# Chapter 10

# **Accessing and Programming the Video Cards**

This chapter explains methods of programming the most popular video cards on the PC market. Even though the video cards mentioned here differ in their capabilities, they are all based on the same basic principle. High level languages such as BASIC, Pascal or C often have their own specific keywords and commands for controlling screen display. However, many of these commands merely call BIOS or DOS functions, which are both slow and inflexible in execution.

# Direct access

Direct access to the video card is the alternative. Applications from Lotus 1-2-3® to dBASE® use direct video access coding, to guarantee both speed and that element of extra control over the video display. The main disadvantage: Programming in assembly language is required, since the communication here occurs at the system level. This chapter examines the programming needed for the best known video cards on the market

- Monochrome Display Adapter (MDA), also called a *monochrome card*
- Color Graphics Adapter (CGA), also called a *color card*
- Hercules Graphic Card (HGC)
- Enhanced Graphic Adapter (EGA)
- Video Graphics Array (VGA)

Most of the graphic cards on the market are compatible with one of the cards mentioned in this chapter, and the descriptions stated here should apply to those cards.

# Video Graphics Array (VGA)

This also applies to the newest generation of video cards, the VGA card. Designed in conjunction with the IBM PS/2 system, the VGA card is now available to the general public as an add-on card. This chapter demonstrates some general features of the EGA and VGA, as well as a few programming techniques.

# What's needed

Before a video card can display a character or graphic pixel on a monitor screen or *CRT* (cathode ray tube), the card must know the following:

- which character or graphic pixel to display
- The color of the character or pixel
- The location on the screen at which it should be displayed.

PC video cards include RAM which collects information about every CRT screen pixel or screen location. This RAM memory is called *video* RAM and interfaces with the PC's RAM, allowing direct access from the microprocessor.

## Speed

Rapid screen changes are important in word processing programs and other PC applications. For example, if you are paging through a word processing document at high speed, a 25-line, SO-column screen requires the transmission of 2,000 characters through the video card at one time. Fast data transfer is even more important for high-resolution graphics. For example, the 200x640-pixel IBM Color Graphics Adapter transmits 12S,OOO pixels of graphic information at a time.

## Display modes

Each type of video card can have more than one display mode. Text and graphics display may be very different from one another. The monitor cannot distinguish between the two modes; it just processes the graphic information sent by the video card (or *video controller).* For the programmer and the video card, the modes require completely different programming techniques.

# Graphic mode and text mode

Graphic mode stores the color of a screen pixel in one or more bits, then transmits the contents of video RAM more or less directly to the screen. Text mode uses a different method. The ASCII code of a character is stored in video RAM for each screen location. When the video controller displays the screen, it obtains the character pattern of the ASCII code from the ROM chip on the video card, then converts the code into a character matrix of pixels. This pattern then passes to the monitor and appears on the screen.

PC text mode uses the 256-character extended character set (see Appendix I). Since these characters are numbered sequentially from 0 to 255, one byte is enough for each screen position to display the character at the proper position.

### Attribute bytes

Every screen position has an *attribute byte* which indicates the color or display attribute of the character (underlined, blinking, inverse video, etc.). This means that two bytes are needed for each position on the screen. Therefore, a total of 4000 bytes are required for a 25-line, SO-column screen. This appears to be a lot of memory at first glance, but is fairly small when compared to the memory requirements for bit-mapped graphic screen. In graphic mode, each dot is represented by one or more bits. A resolution of 64Ox200 pixels requires 12S,OOO bits (16K).

Another advantage of text mode is the simplicity in exchanging one character for another on the screen. The bit-map mode has its own advantages. Besides graphic displays, text can be displayed as individual dots whose pattern is derived from a character table in RAM installed by the user. This means that the user can design his own fonts (character sets).

# 1O. **1 Anatomy of a Video Card**

The figure below shows the individual hardware components of a video card. The starting point for creating the picture is always the video RAM. This video RAM contains information about the characters to be displayed, and their display attributes (color, style, etc.).

#### Getting to the screen

The character generator first accesses video RAM, reading the characters one by one, and uses a character pattern table to construct the bit-map that will later form the character on the screen. The attribute controller also gets information about the display attributes (color, underlining, reverse, etc.) of the character from the video RAM. Both modules prepare this information and send it to the signal controller, which converts it to appropriate signals to be sent to the monitor. The signal controller itself is controlled by the CRT controller, which is the central point of video card operations. Besides the monitor and the video RAM, this CRT controller is one of the most important components of a video system. We will examine all these components in greater detail.



*Block diagram of a video card* 

## The monitor

The monitor is the device on which the video data is displayed. Unlike the video card, the monitor is a "dumb" device. This means it has no memory and cannot be programmed. All monitors used with PCs are *raster-scan devices,* in which the picture is made up of many small dots arranged in a rectangular pattern or raster.

When forming the picture, the electron beam of the picture tube touches each individual dot and illuminates it if it is supposed to be visible on the screen. This is done by switching on the electron beam as it passes over this dot, causing a , phosphor particle on the picture tube to light up.

#### Color monitors

While monochrome monitors need only one electron beam to create a picture, color monitors use three beams which scan the screen simultaneously. Here a screen pixel consists of three phosphor particles in the basic colors of light: red, green, and blue. Each color has a matching electron beam. Any color in the spectrum can be created by combining these three colors and varying their intensities.

But since an ionized phosphor particle emits light for only a very brief period of time, the entire screen must be scanned many times per second to create the illusion of a stationary picture. PC monitors perform this task between SO and 70 times per second. This repeated re-scanning is called the *refresh rate.* One rule of thumb for this rate: The faster the refresh rate, the better quality the picture.

Each new screen image begins in the upper left comer of the screen. From there the electron beam moves to the right along the first raster line. When it reaches the end of this line, the electron beam moves back to the start of the next line down, similar to pressing the <Return> key on a typewriter. The electron beam then scans the second raster line, at the end of which it moves to the start of the next raster line, and so on. Once it reaches the bottom of the screen, the electron beam returns to the upper left comer of the screen and the process starts over again. The illustration below shows the path of the electron beam.

Remember that the movement of the electron beam is controlled by the video card, not by the monitor itself.



*Electron beam scan movement* 

The resolution of the monitor naturally controls the number of raster lines and columns which the electron beam scans when creating a display. Thus, a monitor which has only 200 raster lines of 640 raster columns each clearly cannot handle the high resolutions of an EGA card at 640x350 pixels. The four monitor types used with a PC generally have the following resolutions:



# The CRT controller

The CRT Controller or CRTC is the heart of a video card. It controls the operation of the video card and generates the signals the monitor needs to create the picture. Its tasks also include controlling light pens, generating the cursor and controlling the video RAM.

To inform the monitor of the next raster line, the CRTC sends a display enable signal at the start of each line, which activates the electron beam. While the beam moves from left to right over each raster column of the line, the CRTC controls the individual signals for the electron beam(s) so that the pixels appear on the screen as desired. At the end of the line, the CRTC disables the display enable signal so that the electron beam's return to the next raster line doesn't make a visible line on the screen. The electron beam is directed to the left edge of the following raster line by the output of a horizontal synchronization signal. The display enable signal is again enabled at the start of the next raster line, and the generation of the next line begins.

#### Overscan

Since the time that the electron beam needs to return to the start of the next line is less than the time the CRTC needs to get and prepare new information from the video RAM, there is a short pause. But the electron beam cannot be stopped, so we get something called *overscan,* which is visible as the left and right borders of the actual screen contents. Although this is an undesirable side effect in one sense, it is useful because it prevents the edges of the screen contents from being hidden by the edge of the monitor. If the electron beam is enabled while it is traveling over this border, a color screen border can be created.



*Rasters and overscan on a screen* 

Once the electron beam reaches the end of the last raster line, the display enable signal is disabled, and a vertical synchronization signal is sent. The electron beam returns to the upper left comer of the screen. Again the display enable signal is reenabled and scanning again begins.

## Pause and overscan

As with the horizontal electron beam return, a pause results which is displayed in the fonn of overscan, creating a vertical screen border.

# Signal timing

The timing of individual signals varies from video mode to video mode. For this reason, the CRTC has a number of registers which describe the signal outputs and their timing. The structure of these registers and how they are programmed will be discussed in the remainder of this section. Many of these registers come from the registers of the 6845 video controller from Motorola. This controller is used in the MDA, CGA, and Hercules graphics cards. The EGA and VGA cards use a special VLSI (very large scale integration) chip as a CRTC, and its registers are somewhat more complicated. The techniques described here are intended as general descriptions for all video cards.



These registers, like all of the other registers on the video card, are accessed via I/O ports with the assembly language instructions IN and OUT. The registers of the CRTC are accessed through a special address register, rather than directly from the address space of the processor. The number of the desired CRTC register is written to the port corresponding to this address register. Then the contents of this register can be read into a special data register with the IN assembly language instruction. If a value is to be written to the addressed register, it must be transferred to the data register with the OUT instruction. Then the CRTC automatically places it in the desired register. These two registers are actually found at successive port addresses, but these addresses vary from video card to video card.

We will include tables throughout the chapter to describe the contents of individual CRTC registers under the various video modes. Here's an example which shows how the contents of these registers are calculated and how the individual registers are related to each other. If you try some of these calculations with your calculator or pc, you will notice that some of them do not work out evenly. But since the registers of the CRTC hold only integer values, they will be rounded up or down.





The bandwidths in the figure above specify the number of points which the electron beam scans per second, and is therefore also called the point or dot rate. The vertical scan rate specifies the number of screen refreshes per second, while the horizontal scan rate refers to the number of raster lines which the electron beam scans per second

Starting with these values. let's practice calculating the individual CRTC register values for the 80x2S character text mode on a CGA card.

Dividing the bandwidth by the horizontal scan rate we get the number of pixels (screen dots) per raster line.

> Bandwidth 14.318 MHz Horizontal scan rate 15.570 KHz Pixels per line 919

Since the CRTC registers generally refer to the number of characters rather than pixels. this value must be converted to the number of characters per line. This is done by dividing the number of pixels per line by the width of the character matrix. On the CGA card this is eight pixels.

> Pixels per line 919 <sup>+</sup>Pixels per character 8 Characters per line 114

This value, decremented by one, is placed in the first register of the CRTC and speciftes the total number of characters per line. In the second register we load the number of characters that will actually be displayed per line. The 80x25 character text mode usually offers 80 characters.

The difference between the total and the number of characters actually displayed per line is the number of characters which can be displayed between the horizontal return and the overscan. The difference in this case is 34 characters.

The duration of the horizontal beam return must be entered in the fourth register of the CRTC. This register stores the number of characters which could be displayed during this time. rather than the actual time duration. The monitor specifications deftne this instead of the video card itself. As a rule this number is between *5%* and 15% of the total number of characters per line. A color monitor uses exactly ten characters.

This leaves 24 characters for the overscan (the horizontal screen border). The third CRTC register specifies how these characters are divided between the left and right screen borders. This register specifies the number of character positions which will be scanned before the horizontal beam return occurs. The BIOS specifies the value 90 here. or after ten characters have been displayed for the screen borders. The remaining 14 characters are placed at the start of the next line and form the left screen border.

The calculations for the vertical data. the number of vertical lines. the position of the vertical synchronization signal. etc.. follow a similar scheme. The first calculation is the number of raster lines per screen. This results from the division

of the number of lines displayed per second by the number of screen refreshes per second:



Since the characters in CGA text mode are eight pixels high by eight pixels wide, we again divide by eight to get the number of text lines per screen:



This result must be decremented by one and then loaded into the fifth register of the CRTC. The number of displayed lines is loaded into the seventh register. Since seven fewer lines are displayed than are actually available, these extra lines are used for the vertical beam return and overscan, whereby the vertical beam return begins after the 28th line.

The character height must be decremented by one and loaded into CRTC register nine. The decrement results is 7 in this example. This value also determines the range for the values loaded into register ten and eleven. They specify the first and last raster lines of the screen cursor. The cursor position is determined by the contents of registers 14 and 15. They refer to the distance of the character from the upper left comer of the screen, instead of line and column. This value is calculated by multiplying the cursor line by the number of columns per line and then adding the cursor column. The high byte of the result must be loaded into register 14 and the low byte in register 15.

# The video RAM area

The contents of registers 12 and 13 determine the area of video RAM displayed on the screen. To understand these registers, we first need to know something about the way video RAM is organized.

The third component of the video system determines what will eventually be displayed on the screen. In text mode, the video RAM contains the ASCII codes of the characters to be displayed and their attributes. While the organization of video RAM in this mode is identical for all of the video cards discussed here, the organization for graphic mode varies from card to card. The description of each card discusses the way video RAM organizes graphic modes (more on this later).

As the illustration below shows, each screen position occupies two bytes in video RAM. The ASCII code of the character to be displayed is placed in the first of these two bytes, the one with the even address. By using eight bits per character code, a maximum of 256 different characters can be displayed.



*Normal text mode structure in video RAM* 

After the ASCII code, and always at an odd offset address, follows the attribute byte, which defmes the appearance of the character on the screen. The attribute controller divides it into two nibbles, whereby the upper nibble (bits four to seven) describes the character background, and the lower nibble (bits zero to three) describes the character foreground. This results in two values between zero and fifteen which are interpreted depending on the type of monitor attached. With a color monitor (and a CGA or EGA card) both values select one of 16 possible colors. Each character on the screen can thus have its own foreground and background colors.

A monochrome monitor cannot display colors, regardless of the adapter. Here the attribute controls whether the character is displayed at high or low intensity, inverse, or underlined.

#### Character organization in video RAM

To access video RAM, you must know how the individual characters are organized within this memory. This organization is similar to character display on the screen.

The first character on the screen (the character in the upper left corner) is also the frrst character in video RAM, located at offset position OOOOR. The next character to the right is located at offset position 0002R. All 80 characters of the frrst screen line follow in this manner. Since each screen character takes two bytes of memory, each line occupies 160 bytes of RAM. The first character of the second screen line follows the last character of the frrst line, and so on.

#### Finding character locations in video RAM

You can easily find the starting address of a line within video RAM by multiplying the line number (starting with zero) by 160. To get from the beginning of the line to a character within the line, the distance of the character from the start of the line must be added to this value. Since each character takes two bytes, this is done simply by multiplying the column number (also starting at zero) by two. Adding both products together yields the offset position of the character in the video RAM. These calculations can be combined into a single formula:

```
Offset position (row, column) = row * 160 + column * 2
```
Note: Since only 40 characters per line are displayed in 40-column video modes, the factor 80 must replace the original 160.

The RAM memory of the video card is integrated into the normal RAM of the PC system, so you can use normal memory access commands to access video RAM. You must know the segment address of video RAM, which is used together with the formula above to fInd the offset position. Section 10.7 shows how this can be done easily in assembly language, BASIC, Pascal, and C.

Now that we have discussed the most important similarities between the four video cards, the following four sections describe the capabilities of these cards. In addition, these sections explain how these capabilities can be used for optimal screen output

# **10.2 The IBM Monochrome Card**

The IBM Monochrome Display Adapter, or MDA, is probably the oldest of the video cards. This card is based on the Motorola 6845 video controller, which is an intelligent peripheral chip. The 6845 controller constructs a display by generating the proper signals for the monitor from video RAM.

This card is excellent for text display. This is achieved with a 9x14 character matrix, which pennits high-resolution character display. The format of this matrix is unusual since a character generator containing the bit pattern of each character can only produce characters 8 pixels wide. Characters from the IBM character set may not connect with each other (e.g., using box characters to draw a box). A circuit on the graphics card sidesteps this disadvantage by copying the eighth pixel of the line into the ninth pixel for any characters whose ASCII codes are between BOH and DFH. This allows the horizontal box drawing characters to connect



*Monochrome display adapter-9x14 character matrix* 

The character generator requires one byte for each screen line: one bit per pixel, eight bits per line. Each character requires 14 bytes. The complete character set has a memory requirement of almost 4K, stored in a ROM chip on the card. For some reason the card has an 8K ROM, leaving the second bank of 4K unused.

## Video RAM on the MDA

The video RAM of the card starts at address B000:0000 and extends over 4K (4,096) bytes). Since the screen display only has space for 2,000 characters and requires only 4,000 bytes of memory for those characters, the unused 96 bytes at the end of video RAM are available for other applications.

The following figure shows the meanings of the different values representing the attribute byte:



*Attribute byte valuer-lBM monochrome display adapter* 

Any combination of bits can be loaded into this byte. However, the MDA only accepts the following combinations:



Byte combinations-*IBM* monochrome display adapter

Besides these bit combinations, bits 3 and 7 of the attribute byte can be set or unset. Bit 3 defines the intensity of the foreground display. When this bit is set, the characters appear in higher intensity. Bit 7's purpose varies with the contents of the control registers (more on this later). For now, all you need to know is that bit 7 can either enable blinking characters, or enable an intensity matching the background color.

Monochrome cards have two more registers available: the control register and the status register.



*Control register* 

#### MDA control register

The control register located at port 3B8H controls the monochrome display adapter's different functions. As the figure below shows, only bits 0, 3 and 5 are of importance. Bit 0 controls the resolution on the card. Although the card only importance. Bit 0 controls the resolution on the card. Although the card only supports one resolution  $(80x25$  characters), this bit must be set to 1 during system initialization. Otherwise the computer goes into an infinite wait loop. Bit 3 controls the creation of a visible display on the monitor. If bit 3 is set to 0, the screen is black and the blinking cursor disappears. If bit 3 is set to 1, the display returns to the screen. Bit 5 has a similar function: If bit 7 in the attribute byte of the character is set to 1, it enables blinking characters. If bit 7 contains the value 0, the character appears, unblinking, in front of a light background color. This means that bit 7 of the attribute byte acts as an intensity bit for the background. This register can only be written. This makes it impossible for a program to determine whether the display is turned on or off. The normal value for this register is 29H, meaning that all three relevant bits default to 1.



*Status registers (3BAH)* 

#### MDA status register

Only bits 0 and 3 are used in the status register; all the other bits must contain the value 1. Unlike the control register, programs can read this register, but register contents cannot be changed by program code.

#### Horizontal synchronization

Bit 0 indicates if a horizontal synchronization signal is being sent to the display screen. The video card sends this signal after creating a screen line (not to be confused with a text line, which consists of 14 screen lines) on the screen. This signal informs the electron gun, which "draws" the picture on the screen, that it should return to the left border of the current screen line. In this case the bit has the value 1. Bit 3 contains the value of the pixel where the electron beam is currently located. A 1 signals that the pixel is visible on the screen and 0 means that the screen remains black at this location.

# MDA internal registers

Besides the two registers directly connected to the hardware of the monochrome display adapter, the 6845 video processor contains a series of internal registers. These 18 registers are open to user access through the 6845 index register and data register. The index register is connected to port address 3B4H, the data register at port address 3B5H. You can only write to the 6845 registers—you cannot read data from them.

When you enter a value into one of the 18 registers, the number of the register (0-17) passes first into the index register. Then the value which is transmitted to the register passes into the data register. The 6845 then transmits the indicated value to the proper register. Most of these 18 registers should not be modified, since they contain important data about the screen structure (e.g., synchronization signals) and incorrect values in these registers can damage the monitor. The following table shows the meanings of the individual registers and the values which ensure a correct display.



The following program makes full use of the monochrome display adapter's capabilities. It was written in assembly language. The individual routines are fully documented and require no additional explanation. The demonstration program built into the listing shows practical application of the individual routines.

#### Assembler listing: VMONO.ASM

```
; ••**•••**.***••••••••******••••*** •••• *****••••••••••*····****··*****i 
;* VMONO *; 
;* Task : makes some elementary functions available for *;<br>;* access to the monochrome display screen **
;* access to the monochrome display screen *; 
 ;*-------------------------------------------------------------------*;
;* Info : all functions subdivide the screen * ; 
;* into columns 0 to 79 and lines 0 to 24 * ; 
 ;*-------------------------------------------------------------------*;
;* Author MICHAEL TISCHER * ; 
 ;* Developed on : 8/11/87 * ; 
;* Last Update : 6/14/89 * ; 
 ;*-------------------------------------------------------------------*;
;* assembly : MASK VMONO; *; 
 ;* LINK VMONO; *; 
;*-------------------------------------------------------------------*; 
;* Call : VMONO *; 
; ••••*.*****.** ••**********************.*••••••*** ••••*•••************; 
:= <math>const</math> and <math>...</math>CONTROL REG - 03B8h ;Control register port address 
ADDRESS-6845 - 04B4h ;6845 address register 
DATA 6845 - 03B5h ;6845 data register 
VIO_SEG - OBOOOh ;Segment address of video RAM 
VIO_SEG = 0B000h ; Segment address of video RAM<br>
CUR_START = 10 ; Register \# CRTC: Starting cursor line<br>
CUR_END = 11 ; Register \# CRTC: Ending cursor line<br>
CURPOS_HI = 14 ; Register \# CRTC: Cursor pos. hi byte<br>
C
                                        Register \frac{11}{100} cursor line<br>The cursor line
                                         ; Register \frac{1}{2} CRTC: Cursor pos. hi byte
                                        Register \frac{1}{2} CRTC: Cursor pos. lo byte
DELAY = 20000 ; Counter for delay loop
```
*i-* Stack ------------------------------------- stack segment para stack ;Definition of stack segment dw 256 dup (?) ; 256-word stack stack ends ;End of stack segment ;- Data **--------------------------------------** data segment para 'DATA' ;Define data segment ;== the Data for the Demo-Program ===  $str1$  db  $a$ <sup>m</sup>, 0<br>str2 db <sup>m</sup> >PC  $str2$  db  $*$  >PC SYSTEM PROGRAMMING<  $*$ , 0<br>str3 db  $*$  window 1  $*$ , 0 str3 db " window 1 ", 0<br>str4 db " window 2 ", 0 str4 db  $"$  window 2<br>str5 db  $"$ the program is stopped by  $\bullet$ db **\*** pressing a Key.... initm db 13,10, "VMONO (c) 1987 by Michael Tischer", 13, 10, 13, 10 db "This demonstration program only runs with " db " a monochrome", 13, 10, "display card. If your PC " db "has another type of display card, ", 13, 10 db "please enter <s> to stop the " db " program.", 13, 10, "Otherwise press any " db "key to start ", 13,10 db "the program ...", 13,10, "\$" *i--* Data -===--~---~-=-=-=------=---==------====----------==-------- linen  $dw = 0*160,1*160,2*160$ ; Start addresses of the lines as dw 3\*160,4\*160,5\*160 ;offset addresses in the video RAM dw 6\*160,7\*160,8\*160 dw 9\*160,10\*160,11\*160,12\*160,13\*160,14\*160,15\*160,16\*160 dw 17\*160,18\*160,19\*160,20\*160,21\*160,22\*160,23\*160,24\*16° data ends ;End of data segment *i--* Code ----=-------------==-==---------------------- code segment para 'CODE' ;Definition of the CODE segment assume cs:code, ds:data, es:data, ss:stack ;== this is the Demo-Program ================================== demo proc far mov ax,data ;Get segment address of data segment<br>
mov ds,ax ;and load into DS mov ds, ax ;and load into DS<br>mov es.ax ;as well as ES ;as well as ES :-- Display initial msg./wait for input ----mov ah, 9 ; String output function<br>mov dx.offset initm : Address of initial mes. mov dx, offset initm ;Address of initial message<br>int 21h :Call DOS interrupt 21H ;Call DOS interrupt 21H xor ah,ah ;Get function number for key<br>int 16h ;Call BIOS keyboard interrup int 16h iCall BIOS keyboard interrupt<br>
cmp al, "s" ; was <s> entered? ;was <s> entered? je ende ;YES --> end program<br>  $\text{cmp}$  al, "S" ;was <S> entered? cmp al, "S" ; was <S> entered?<br>jne startdemo ; NO --> start dem jne startdemo *iNO* --> start demo ende: mov ax,4c00h ;Function number for program end<br>int 21h :Call DOS interrupt 21H ;Call DOS interrupt 21H

------------------------------- ;-- Display program logo ;-- Fill window with arrows ----------------------------startdemo label near<br>mov cx,0d00h ;Enable full cursor call cdef<br>call cls :Clear screen ;-- Fill screen with ASCII characters ----------- demo1: derno2: **arrow:**  arrowO: arrow1: xor di,di mov si,offset str1 mov cx,2000 mov al,07h call print inc str1 jne demo2 inc str1 loop demo1 ;Start in upper left corner ;Offset address of string1 ;2,000 characters fit on the screen ;white letters on black background ; Display string ;Increment character in test string ;NUL code suppressed ;Repeat output ;-- Create window 1 and window 2 -------- mov bx,0508h mov dx,1316h mov ah,07h call clear mov bX,3C02h mov dx,4A10h<br>call clear mov bx,0508h call calo mov si,offset str3 ;Offset address string 3<br>mov ah,70h ;Black characters, white mov ah, 70h<br>call print mov bX,3C02h call calo mov si,offset str4 call print xor di,di mov si,offset str5 call print mov bx,lEOCh call calo mov si,offset str2 mov ah,OFOh call print xor ch,ch mov bl, 1<br>push bx mov di,offset str3<br>mov cl,15 sub cl,bl shr cl, 1<br>or cl, cl or cl,cl arrow1  $mov \; al.$ " rep stosb<br>mov cl.bl mov al, \*\*\* rep stosb mov cl,15 sub cI,bl shr cl,l or cl,cl je arrow2 mov **al,· ..**  ;Upper left comer of window 1 ; Lower right corner of window 1 ;White letters, black background ; Clear window 1 ; Upper left comer of window 2 ; Lower right corner window 2 ;Clear window 2 ; Upper left comer of window 1 ;Convert to offset address ;Black characters, white background ;Display string 3 ;Upper left comer of window 2 ;Convert to offset address ;Offset address string 4 ;Display string 4 ;Upper left display corner ;Offset address string 5 ;Display string 5 ;Column 30, line 12 ;Convert offset address ;Offset address string 2 ;Inverse blinking ;Display string 2 ;Hi-byte of the counter to 0 ;Asterisk ;Push BX on the stack ;Draw arrow line in string 3 ;Total of 15 characters in a line ;Calculate number of spaces ;Divide by 2 (for left half) ; YES --> ARROW1 ;Draw blanks in string 3 ;Number of asterisks in counter ;Draw stars in string 3 ;Total of 15 characters in a line ;Calculate number of blanks ;Divide by 2 (for right half) ;No blanks? ;YES --> ARROW2

rep stosb ;Draw blanks in string 3<br>
arrow2: mov bx,0509h ;below the first line of window 1<br>
call calo ;Convert to offset address<br>
mov si,offset str3 ;Offset address string 3 mov ah,07h ;White characters, black background call print ; Display string 3 call print ;Display string 3 mov bx,3CIOh ;into the lowest line of window 2 call calo ;Convert offset address ;Display string 3 ;-- Brief pause -------------------------------------- mov cx, DELAY ; Loop counter<br>loop waitlp : Count loop to waitlp: loop waitlp : Count loop to 0 :-- Scroll window 1 line down ------------------------mov bx,0509h ; Upper left corner of window 1<br>mov dx,1316h ; Lower right corner window 1 ;Lower right corner window 1<br>;Scroll down mov cl,1 ; Scroll do<br>call scrolldn : one line call scrolldn ;-- Scroll window 2 one line up ---------------------- mov bx,3C03h ; Upper left corner window 2<br>mov dx,4A10h ; Lower right corner window 2 %, Iower right corner window 2<br>%Right up call scrollup ;-- Was a key pressed? (end program) ------------------mov ah,1 ;Function number for testing key<br>int 16h ;Call BIOS keyboard interrupt int 16h ;Call BIOS keyboard interrupt<br>jne end it ;Keypress -> goto end of progr ; Keypress -> goto end of program ;-- NO, display next arrow -------------------pop bx ;Pop BX from stack again<br>add bl,2 ;2 more stars in next lip add bl, 2 ; 2 more stars in next line<br>
cmp bl, 17 ; Reached 17 ? cmp bl,17 ; Reached 17 ?<br>jne arrow0 ; NO --> next jne arrowO **;NO --> next arrow**  ;No key --> next arrow ;-- Get ready to end program xor ah,ah ;Get function number for key<br>int 16h ;Call BIOS-keyboard-interrup end it: int 16h ;Call BIOS-keyboard-interrupt<br>mov  $cx,$ 0DOCh ;Restore normal cursor ; Restore normal cursor call cdef call cls **iClear screen**<br>  $\frac{1}{2}$  **iPhone iPhone iCo** to end of ;Go to end of program demo endp i== **Functions** ====--===---============-----==-====-===========-= ;-- SOFF: switches the display off ----------------------- $:-$  Input  $:$  none<br> $:-$  Output  $:$  none ;-- register : AX and DX are changed SOFF proc near mov dx, CONTROL REG ; Address of display control register<br>in al, dx ; read its content in  $a1$ , dx<br>and  $a1$ , 11110111b and al, 11110111b ;bit  $3 = 0$ : display off out  $dx$ , al ;set new value (display ; set new value (display off) ret ;back to caller SOFF endp

;-- SON: switches the display on ------------;-- Input : none<br>;-- Output : none -- register : AX and DX are changed SON proc near mov dx, CONTROL REG ; Address of display control register<br>in al.dx : Read its content in al,dx  $\overline{\phantom{a}}$  ; Read its content<br>or al,8 ; Bit 3 = 1: display on out dx,al ;Set new value (display on)<br>ret ;Back to caller SON endp ;-- CDEF: sets the start and end line of the cursor -----------<br>;-- Input : CL = Start line<br>;-- CH = End line  $CH = End$  line ;-- Output : none ;-- register : AX and DX are changed<br>cdef proc near proc near mov al, CUR\_START ;Register 10: start line<br>mov ah, cl ;Start line to AH mov ah,cl  $\overline{\phantom{0}}$  ; Start line to AH call setvk : Transmit to video call setvk . Transmit to video controller mov al, CUR\_END ; Register 11: end line<br>mov ah.ch ; End line to AH mov ah, ch in the set of the short set when the set of the short control in the short control of jmp short setvk ;Transmit to video controller cdef endp *;***--** SETBLINK: sets the blinking display cursor ------------<br> *;*-- Input : DI = offset address of the cursor<br> *;*-- Output : none :-- register : BX, AX and DX are changed setblink proc **near**  mov bx,di ;Transmit offset to BX<br>mov al,CURPOS\_HI ;Register 15:Hi-byte of cursor offset<br>mov ah,bh ;HI-byte of the offset<br>call setvk ;Transmit to video controller call setvk ;Transmit to video controller mov al,CURPOS\_La ;Register 15:Lo-byte of **cursor** offset mov ah,bl ;Lo-byte of the offset ;-- SETVK is called automatically ---------------------- setblink endp ;-SETVK: sets a byte in one of the registers of the video controller -  $;--$  Input : AL = number of the register<br> $;--$  AH = new content of the register ;-- AH = new content of the register<br>;-- Output : none ;-- register : OX and AL are changed setvk proc near mov dx,ADDRESS\_6845 ;Address of the index register<br>out dx,al ;Send number of the register<br>jmp short \$+2 ;Small I/O pause inc dx ;Address of the index register<br>mov al,ah ;Content to AL mov al,ah ;Content to AL out dx, al ; Set new content<br>ret : Back to caller ; Back to caller setvk endp ;-- GETVK: reads a byte from one register of the video controllers -<br>;-- Input : AL = number of the register

```
;-- SCROLLUP: scrolls a window up by N lines ----------------
;-- Output : AL = content of the register
;-- register : DX and AL are changed
getvk proc near 
          mov dx, ADDRESS 6845
          out 
dx,al 
          jmp 
short $+2 
          inc 
dx 
          in 
al,dx 
          ret 
getvk endp 
;-- Input : BL = line upper left
i-
;-
i-
;-- CL<br>:-- Output : none
                                  ; Address of the index register
                                  ;Send number of the register 
                                  ;Address of the index register 
                                  ;Read content to AL 
                                  ; Back to caller 
              BH = column upper leftOL - line lower right 
               DH = column lower right
              CL = number of lines to scroll 
i-- register : only FLAGS are changed
i-- Info 
scrollup 
proc near 
supl: 
          the display lines released are erased 
          cld 
          push ax 
          push bx 
          push di 
          push si 
          push bx 
          push ex 
          push dx 
          sub dl,bl 
          inc dl 
          sub dl,cl 
          sub dh,bh 
          inc dh 
          call calo 
         mov si,di 
          add bl.cl
          call calo 
         xchg si,di 
          push ds 
         push es 
         mov ax,VIO_SEG 
         mov ds,ax 
         rnov es,ax 
         rnov ax,di 
          mov bX,si 
         rnov cl, dh 
          rep movsw 
         rnov di,ax 
         rnov si,bx 
          add di,160 
         add si,160 
          dec dl 
          jne supl 
          pop es 
         pop ds 
         pop dx 
         pop bx
         rnov bl, dl 
         sub bl,cl 
          inc bl 
         rnov ah,07h 
                                  ;Increment on string instructions 
                                   ;Push all changed registers on the 
                                  ;stack 
                                  iln this case the sequence 
                                  ;must be observed! 
                                  ;These three registers are restored 
                                  ;from the stack before ending 
                                  ;Calculate the number of lines 
                                  ;Deduct number of lines scrolled 
                                  ;Calculate number of columns 
                                ;COnvert upper left in offset 
                                  ;Record Address in SI 
                                  ;First line in scrolled window 
                                 ;Convert first line to offset 
                                ;Exchange SI and DI 
                                 ;Store segment register on 
                                  ;the stack 
                                  ;Segment address of the video RAM 
                                  ito OS 
                                 ; and ES
                                  ;Record DI in AX 
                                  ;Record S1 in BX 
                                  ;Number of column in counter 
                                 ;Move a line 
                                 ;Restore DI from AX 
                                  ;Restore SI from BX 
                                  ; Set next line 
                                  ;Processed all lines? 
                                  iNO --> move another line 
                                  ;Get segment register from 
                                  ;stack 
                                 ;Get lower right corner 
                                ;Read number of lines 
                                ;Get upper left corner 
                                  ;Lower line to BL 
                                  ;Deduct number of lines 
                                  ;Color : black on white
```
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call clear ;Erase lines freed pop si ;CX and DX have already<br>pop di ; been read ;been read pop bx pop ax ret ;Back to caller scrollup endp ;-- SCROLLDN: scrolls a window down N lines ---------------<br>;-- Input : BL - line upper left<br>;-- BH = column upper left **i--** BH - column lower right<br>  $\begin{array}{ll}\n\text{F}-\text{D} & \text{D} & \text{D} & \text{D} \\
\text{F}-\text{D} & \text{D} & \text{D} & \text{D} \\
\text{F}-\text{D} & \text{D} & \text{D} & \text{D} \\
\text{F}-\text{D} & \text{D} & \text{D} & \text{D}\n\end{array}$ ;-- register : only FLAGS are changed<br>;-- Info : display lines released : display lines released are erased scrolldn proc near cld ;Increment on string instructions push ax ;Store all changed registers on the push bx ; stack<br>push di ; In th push di ; In this case the sequence<br>push si : must be observed ! ; must be observed ! push bx ; These three registers are returned<br>push cx ; from the stack before the end push cx ; from the stack before the end<br>push dx : of the routine ;of the routine sub dh,bh ;Calculate the number of the column<br>inc dh mov al, bl ;Record line upper left in AL mov bl, dl ;Line upper right to line upper mov bl,dl ;Line upper right to line upper left<br>call calo ;Convert upper left into offset call calo ;Convert upper left into offset<br>
mov si,di ;Record address in SI<br>
sub bl.cl ;Deduct number of lines to scro sub bl,cl ;Deduct number of lines to scroll<br>call calo ;Convert upper left in offset call calo  $\begin{array}{ll}\n\text{convert upper left in offset} \\
\text{for } \mathbf{N} = \mathbf{N}.\n\end{array}$ xchg si,di ;Exchange SI and OI sub dl,al ;Calculate number of lines<br>inc dl ;Deduct number inc dl ;Oeduct number sub dl,cl ;of lines to be scrolled ; Push segment register onto stack push es<br>mov ax,VIO SEG ; Segment address of video RAM mov ds,ax <sup>-</sup> ;to DS<br>mov es,ax ;and ES<br>mov ax,di ;Move D sdn1: mov ax,di<br>mov bx,si ;Move SI to BX mov bx, si ;Move SI to BX<br>mov cl, dh ;Number column mov cl,dh ;Number column in counter rep movsw ;Scroll one line<br>mov di,ax ;Get DI from AX mov di, ax ;Get DI from AX mov si,bx ;Restore SI from BX<br>sub di,160 ;Set next line ; Set next line sub si,16O dec dl ;All lines processed ? jne sdn1 ;NO --> scroll another line pop es ;Get segment register from<br>pop ds ;stack pop ds ; stack pop dx ;Return lower right corner<br>pop cx ;Return number of lines pop cx ;Return number of lines<br>pop bx ;Return upper left corne pop bx ; Return upper left corner<br>mov dl,bl ; Upper line to DL mav dl,bl ;Upper line to OL ; Add number of lines dec dl mov ah, 07h ;Color : black on white

```
call clear ;Erase lines which were released 
              pop si \begin{array}{ccc} 1 & \text{if } 5 \text{ is a point} \\ \text{if } 5 \text{ is a point} \\ \text{if } 5 \text{ is a point} \end{array}; already returned
              pop bx 
              pop ax 
              ret ;Back to caller
scrolldn endp
;-- CLS: Clear the complete screen --<br>;-- Input : none
; -- Output : none 
;-- register : only FLAGS are changed 
cIs proc near 
              mov 
ah,07h 
              xor 
bx,bx 
              mov 
dx,4Fl8h 
                                                ;Color is white on black 
;Upper left is (0/0) 
                                              ;Lower right is (79/24) 
              i-- Execute Clear 
cls endp 
;-- CLEAR: fills a designated display with space characters ---
;-- Input : AH = Attribute/color<br>;-- BL = line upper left
;-- BH = column upper left<br>;-- DL = line lower right
;-- DL = line lower right<br>;-- DH = column lower rig
                   DH = column lower right
: -- Output : none
: -- register : only FLAGS are changed
clear proc near
              cld ;Increment on string instructions<br>
push cx                    ;Store all registes which
              push cx \begin{array}{ccc} \text{push} & \text{if} \\ \text{push} & \text{if} \\ \text{push} & \text{if} \\ \text; are changed on the stack
              push si 
             push di 
             push es<br>sub dl,bl
                                              ;Calculate number of lines
              inc dl<br>sub dh,bh
                                            ;Calculate number of columns
              inc dh 
             call calo ;Offset address of upper left corner 
                                            ;Segment address of the video RAM<br>;to ES
             moves,cx<br>xorch,ch
             xor ch, ch ; Hi-bytes of the counter to 0<br>mov al, " ; Space character
                                              ;Space character<br>;Move DI to SI
clear1: mov si,di<br>mov cl,dh
              mov cl,dh ;Number of column in counter<br>rep stosw ;Store space character
              rep stosw ; Store space character<br>mov di,si ; Restore DI from SI
              mov di,si ;Restore DI from SI<br>add di,160 ;Set in next line
              add di,160 ;Set in next line 
              dec dl ;All lines processed 
                                              ;NO --> erase another line
              pop es ;Restore registers from 
              pop di  ,stack
              pop si 
              pop dx 
              pop ex 
              ret ;Back to caller
clear endp
;-- PRINT: outputs a string on the Display -------------------
```
 $; --$  Input : AH = Attribute/color *i--* DI - offset address of the first character ;- SI - offset address of the strinq to DS  $i$ -- SI = offset address of the string to DS<br> $i$ -- Output : DI points behind the last character output ;-- register : AL, DI and FLAGS are changed  $;--$  Info : the string must be terminated with a NUL-character.<br> $;--$  other control characters are not recognized **;--** other control characters are not recoqnized print proc near cld ;Increment on string instructions<br>push si ;Store SI, DX and ES on the stack ; Store SI, DX and ES on the stack push es push dx<br>mov dx,VIO\_SEG mov dx,VIO\_SEG ; Segment address of the video RAM<br>mov es,dx ; First to DX and then to ES mov **es,dx** ;First to DX and then to ES<br>jmp print1 ; YES --> Output finished ;YES --> Output finished print0: stosw **;Store attribute and color in V-RAM**<br>print1: lodsb **;Get next character from the string** lodsb ;Get next character from the string<br>or al,al ;Is it NUL or al, al <br>jne print0 ;NO --> out ;NO --> output printe: pop dx ;Get SI, DX and ES back from stack pop es pop si<br>ret ; Back to caller print endp ;- CALO: converts line and column into offset address ----------------<br>;-- Input : BL = line<br>;-- BH = column  $i$ -- Output : DI = the offset address :-- Registers: DI and FLAGS are changed calo **proc near**  push ax ;Store AX on the stack<br>push bx ;Store BX on the stack ; Store BX on the stack  $\begin{array}{ll}\n\text{shl} & \text{bx,1} \\
\text{mov} & \text{al,bh} \\
\text{iv.} & \text{collumn to AL}\n\end{array}$ mov al,bh ;Column to AL xor bh,bh ;Get Hi-byte<br>mov di, [linen+bx] ;Offset addre mov di, [linen+bx] ;Offset address of the line<br>xor ah.ah ;HI-byte for column offset xor ah,ah ;HI-byte for column offset<br>add di.ax ;Add line- and column offse ; Add line- and column offset pop bx ;Get BX from stack again<br>pop ax ;Get AX from stack again pop ax ;Get AX from stack again<br>ret :Back to caller ; Back to caller calo endp **;== End** =========~--========--======---====================~ code ends ;End of the CODE segment<br>end demo ;Start program execution ; Start program execution w/ demo

# 10.3 The Hercules Graphic Card

The Hercules display adapter displays text in both text mode and graphics mode, with a graphic resolution of 72Ox348 pixels. This card contains enough RAM for two display pages. Each display page is 32K, so video RAM can accept a 4K text page and a graphic page. The frrst display page extends from address BOOO:OOOO to BOOO:7FFF. The second screen page goes from BOOO:8000 to BOOO:FFFF.

# Hercules video RAM

The Hercules card's video RAM in text mode has the same cursor character and port addresses as the IBM monochrome display adapter. With the graphic capabilities, only a few bits in the status and control register are different from the monochrome card. An additional configuration register can be addressed from 3BFH. You can write to this register only. Only bits 0 and 1 are of interest to the programmer. The former indicates whether the graphic mode can be switched on (1) or not (0). Bit 1 determines whether the second display page can be used. Bit 1 contains the value 1 if the second page is usable.

To avoid conflicts with other video cards (especially color cards), both bits are set to 0 at the start of the system so that neither graphic mode nor the second display page are accessible at first. Application programs must configure the Hercules display adapter through the configuration register if the programs require graphic mode or the second screen page.

The control register of the Hercules graphic card has some differences from that of the MDA discussed in the preceding section.



*The Hercules control register (3B8H)* 

Unlike the IBM monochrome display adapter, bit 0 is unused and doesn't have to be set to 1 during the system boot Bit 1 determines text or graphic mode: a 0 in bit 1 enables text mode, while a 1 in bit 1 enables graphic mode. *As* you shall see in the following examples, changing these bits isn't enough to switch between text and graphic modes. The internal registers of the 6845 must be reset as well. During this process, the screen display must be switched off to prevent the 6845 from creating gatbage during its reprogramming.

The Hercules card has a seventh bit in this register. Its contents determine which of the two screen pages appear on the monitor screen. If this bit is 0, the first screen page appears; a 1 calls the second screen page on the screen. Independent of each other, the user can write to or read from either page at any time. You can only write to this register; attempts to read this register return the value FFH. Because of this, it is impossible to switch off the display simply by reading the contents of the status register and erasing bit 3, regardless of the display mode and the screen page selected.



*Hercules status register (3BAH)* 

Only the significance of bit 7 makes this register different from the IBM monochrome card. It's always set to 0 when the 6845 sends a vertical synchronization signal to the display. This signal is always sent when the last screen line has been constructed. The electron beam, which constructs the display, then jumps to the first line of the screen to start constructing a new screen.

Since the Hercules card uses the same processor as the IBM card, the internal registers of the 6845 and their meaning are identical to the IBM card. The index register and data register are also located at the same address. The following values must be assigned to the various registers in the text and graphic modes respectively:



As mentioned earlier, the Hercules card in graphic mode provides 348x720 resolution. Every pixel on the screen corresponds to one bit in the video RAM. If the corresponding bit contains the value 1, the dot is visible on the display, otherwise it remains dark. The following figure shows the construction of the video RAM in the graphic mode.



*Video RAM* and *the screen under construction* 

The bit patterns of the individual lines in the video RAM aren't arranged sequentially, as you might have assumed. The 32K of video RAM is divided into four 8K blocks. The first block contains the bit pattern for any lines divisible by 4 (0,4,8, 12, etc.). The second block contains the bit patterns for lines 1,5,9, 13 etc. The third block contains the bit patterns for lines 2, 6, 10, 14, etc., while the last block contains lines 3, 7, 11, 15 etc. When the 6845 generates a display, it obtains information for screen line zero from the fIrst data block, screen line one from the second data block, etc. Mter it has obtained the contents of the third screen line from the fourth data block, it accesses the first data block again for the structure of the fourth line. Each line requires 90 bytes within the individual data blocks-every pixel requires a bit, and 720 pixels divided by 8 bits (per byte) equals 90. The fIrst 90 bytes in the first memory area provide the bit pattern for screen line zero, and the 90 bytes following provide the bit pattern for the fourth screen line. The zero byte of one of these 90-byte sets represents the first eight columns of a screen line (columns 0-8). The first byte represents columns 8-15,

etc. Within one of these bytes, bit 7 corresponds to the left screen pixel and bit 0 corresponds to the right screen pixel.



#### *Relationship between 9O-line bytes and screen display*

If the screen pixels of a line (0 to 719) and the screen pixels of a column (0 to 347) are sequentially numbered, an equation indicates the address of the bytes relative to the beginning of the screen page. This address contains the information for a pixel with the coordinates X/Y.

To determine the bit within the byte which represents the pixel, the following formula can be used:

Address = 2000H \* (Y mod 4) + 90 \* int(Y/4) + int(X/8)

The following program demonstrates the abilities of the Hercules display adapter. The individual routines within this program have some differences from the routines shown in the monochrome display adapter demo program from the previous section. The routines here enable access to both screen pages, and support the Hercules graphic mode.

#### Assembler listing: VHERC.ASM



;\* last update : 6/15/89 \*; **;\*---***----------\*i*  ;\* assembly : MASM VHERC; \*; ;\* LINK VHERC: \*; ,call : VHERC \*; *i\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*·\*\*\*\*·\*····\*\*\*\*\*\*\** **\*\*\*\*\*\*••\*\*\*\*•••\*: ;\*--***---------\*i*   $:=$  Constants  $==$ CONTROL REG - 03B8h ;Control register port address  $ADDRESS-6845 = 03B4h$  ;6845 address register<br> $DATA 6845 = 03B5h$  ;6845 data register  $DATA 6845 = 03B5h$  ;6845 data register<br>CONFIGREG = 03BFh ;Configuration regis CONFIG REG = 03BFh ;Configuration register<br>VIO SEG = 0B000h ;Video RAM segment addr VIO SEG OBOOOh ;Video RAM seqment address CUR\_START = 10 ;Reg.  $\#$  for CRTC: Start cursor line<br>
CUR\_END = 11 ;Reg.  $\#$  for CRTC: End cursor line<br>  $\frac{1}{2}$ CUR END = 11 ;Reg.  $\#$  for CRTC: End cursor line<br>
cURFOS HI = 14 ;Reg.  $\#$  for CRTC: Cursor pos hi b CURFOS HI = 14 ;Reg.  $\#$  for CRTC: Cursor pos hi byte<br>CURPOS LO = 15 ;Reg.  $\#$  for CRTC: Cursor pos lo byte ; Reg. # for CRTC: Cursor pos lo byte DELAY = 20000 ;Count for delay loop ;== **Macros** =====-========\_\_\_\_\_=-=-========-========\_\_\_ss== setmode macro modus ;Set control register mov dx, CONTROL\_REG ; Screen control register address<br>mov al, modus ; Put new mode in AL register mov al, modus  $\overline{\phantom{a}}$  ;Put new mode in AL register<br>out dx, al ;Send mode to control regist ; Send mode to control register endm setvk macro **;Write value to CRTC registers** ;Input: AL - register number  $\cdot$ AH = Value for register mov dx,ADDRESS\_6845 ;Index register address ;Display register number and new value endm  $i ==$  Stack ====== stack segment para stack ;Definition of stack segment dw 256 dup (?) ;Stack is 256 words in size stack ends ;End of stack segment **;-- Data** -====-=-~-=-========--==---=------=---------------== data segment para 'DATA' ;Define data segment ; == Data needed for demo program ============================= initm db 13,10, "VHERC (c) 1987 by Michael Tischer", 13,10,13,10 db "This demonstration program runs only with • db • a HERCULES",13,10,"graphics card. If your PC " db "has another type of display card, ", 13,10 db "please input an >s< to stop the " db " program.", 13, 10, "Otherwise please press any " db "key to start the ", 13, 10 db "program ...", 13, 10, "\$" strl db 1, 17, 16, 2, 7, 0<br>str2 db 2, 16, 17, 1, 7, 0 db 2,16,17,1,7,0 domes db 13,10 db "This program creates a short graphic demo ", 13,10 db "and a text demo. Pressing a key during the", 13,10

db "demo ends the program.", 13,10 db "Press a key to start the program...", 13, 10, "\$" :== Table of line offset addresses ======== lines dw  $0*160,1*160,2*160$ ; Beginning addresses of the lines as dw 3\*160,4\*160,5\*160 ;offset addresses in video RAM dw 6\*160,7\*160,8\*160 dw 9\*160,10\*160,11\*160,12\*160,13\*160,14\*160,15\*160,16\*160 dw 17\*160,18\*160,19\*160,20\*160,21\*160,22\*160,23\*160,24\*160 grafikt db 3Sh, 2Dh, 2Eh, 07h, SBh, 02h ;Reqister values for the db S7h, S7h, 02h, 03h, OOh, OOh ;graphic mode textt db 61h, SOh, S2h, OFh, 19h, 06h ;Reqister values for the db 19h, 19h, 02h, ODh, OBh, Och ;text mode data ends ;End of data segment ;== Code segment ============ code segment para 'CODE' ;Definition of the code segment  $\alpha_{\mathbf{q}}^{\mathbf{k}}$  100h assume cs:code, ds:data, es:data, ss:stack ;== this is only the Demo-Program ========== demo proc far mov ax, data ;Get segment address of data segment mov **ds,ax** ;Load into OS mov **es,ax** ;and ES **i-- Opening** *msq.,* **wait for input ------------------** mov ah,9 ;Output function number for string<br>mov dx,offset initm ;address of the message<br>int 21h :Call DOS interrupt ;Call DOS interrupt xor ah,ah ;Get function number for key<br>int 16h :Call BIOS keyboard interrup int 16h ;Call BIOS keyboard interrupt<br>
cmp al, "s" :Was <s> entered? cmp **al,<sup>\*</sup>s<sup>\*</sup> fWas** <s> entered?<br>de ende :YES--> End program je ende ; YES--> End program<br>
cmp al, "S" ; Was <S> entered? cmp **al,<sup>"</sup>S"** ;Was <S> entered?<br>ine startdemo :NO --> Start dem ;NO --> Start demo ende: mov ax,4COOh ; Function number - end program<br>int 21h : Call DOS interrupt 21H ;Call DOS interrupt 21H startdemo label near<br>mov ah, 9 mov ah,9 ;Output function number for string<br>mov dx,offset domes ;address of the message<br>int 21h :Call DOS interrupt ;Call DOS interrupt xor ah,ah ;Get function number for key<br>int 16h :Call BIOS keyboard interrup ;Call BIOS keyboard interrupt  $; --$  Initialize graphic mode  $---$ mov al, 11b ;Graphic and page 2 possible<br>call config ;Configure xor bp, bp ;Access display page 0<br>call grafik ;Switch to graphic mod call grafik ;switch to graphic mode xor al,al call cgr ;Erase graphic page 0<br>
xor bx,bx ;Begin in the upper left<br>
xor dx,dx ;Display corner<br>
mov ax,347 ;Vertical pixels



mov cx, DELAY ; Load counter<br>loop pause ; Count to 65, pause: loop pause ;Count to 65,536 setmode 00001000b ;Display page 0 ;-- short pause --------<br>mov cx, DELAY mov cx, DELAY ;Load counter<br>loop pausel ;Count to 65,5 pausel: loop pausel ;Count to 65,536 mov ah,1 ;Test function nr. for key<br>int 16h ;Call BIOS-keyboard-Interry int 16h ;Call BIOS-keyboard-Interrupt ;No key --> continue xor ah,ah ;Get function number for key int 16h ;Call BIOS-keyboard-Interrupt mov bp,O ;Display page 1 call cIs **iClear screen**  mov cX,ODOch ;Restore normal **cursor**  mov cx,0D0ch<br>call cdef<br>call cls call cIs ;Clear screen ; End program demo endp ;== The actual functions follow ==----=~=====-===-----==--= ;-- CONFIG: configures the HERCULES card ----------------------------- ;-- Input : AL : bit 0 - 0 Only text presentation possible  $;--$  1 : also graphic presentation possible<br> $;--$  bit  $1 = 0$  : RAM for display page 2 off  $j--$  bit  $1 = 0$ : RAM for display page 2 off<br> $j--$  1: RAM for display page 2 on 1 : RAM for display page 2 on ;-- Output : none ;-- Register : AX and DX are changed config **proc near**  mov dx,CONFIG<sub>\_</sub>REG ;Address of configuration register<br>out dx,al ;Set new value<br>ret .Back to caller ; Back to caller config endp ;-- TEXT: switches the text presentation on -------------------------- ;-- Input : none ;-- Output : none ;-- Register : AX and DX are changed text proc near mov si, offset textt ;Offset address of the register-table mov bl,OOlOOOOOb ;Display page O,text mode,blinking jmp short vcprog ;Program video-controller again text endp ;-- GRAFIK: switches on the graphic mode ------- --------------------- **i-- Input : none**  ;-- Output : none ;-- Register : AX and OX are changed grafik **proc near**  mov si,offset grafikt ;Offset address of the register-table mav bl,OOOOOOlOb ;Oisplay page 0, graphic mode grafik endp ;-- VCPROG: programs the video controller ---------------------------- ;-- Input SI - address of a register-table

```
;-- BL = value for display-control-register<br>;-- Output : none
;-- register : AX, SI, BH, DX and FLAGS are changed
vcproq 	 proc near 
               setmode bl ;Bit 3 = 0: display aus
              mov cx,12 ;12 registers are set<br>
xor bh,bh ;Start with register 0<br>
lodsb :Get register value from
vcp1: lodsb ;Get register value from the table<br>mov ah,al ;Register value to AH
               mov ah,al ;<br>mov al,bh ;Number of the register to AL
              setvk in the setup of the register to AL<br>setvk for the controller<br>inc bh faddress next register
              inc bh ;Address next register 
                                                 ; Set additional registers
              or bl, 8 ;Bit 3 = 1: display on setmode bl \begin{array}{ccc} ;\text{Set new mode} \ \text{ret} & ;\text{Back to caller} \end{array}; Back to caller
vcprog endp
;-- cOEF: sets the start and end line of the cursor-------------------
;-- Input : cL = start line<br>;-- cH = end line
;-- \text{CH} = \text{end line}<br>;-- Output : none
;-- register : AX and DX are changed
cdef proc near
              mov al, CUR_START ;Register 10: start line<br>
mov ah, cl ;Start line to AH<br>
setvk :Transmit to video-control
              setvk ;Transmit to video-controller<br>mov al,CUR_END ;Register 11: Endline
              mov al, CUR_END ;Register 11: Endline<br>mov ah, ch ;End line to AH<br>setyk ;Transmit to video-com
                                                  ;Transmit to video-controller
              ret 
cdef endp
;-- SETB1INK sets the blinking display cursor ---------------------- i-- Input 01 = offset address of the cursor 
;-- Output none 
;-- register : BX, AX and DX are changed
setblink proc near
              mov bx,di ;Transmit offset to BX<br>mov al,CURPOS_HI ;Register 15:Hi Byte of cursor offset<br>mov ah,bh ;HI byte of the offset<br>setvk :Transmit to video-controller
                                                  ;Transmit to video-controller
              mov al, CURPOS IO ;Register 15: Io-Byte of cursor offset<br>mov ah,bl : ;Io byte of the offset<br>setvk :Transmit to CRTC
                                                  ; Transmit to CRTC
              ret 
setblink endp
;-- GETVK : reads a byte from one register of the video-controller -<br>
;-- Output : AL = number of the register<br>
;-- output : DX and AL are changed<br>
;-- register : DX and AL are changed
getvk 	 proc near 
               mov dx,ADDRESS_6845 ;Address of the index register<br>out dx,al                  ;Send number of the register
                out dx, al . Send number of the register
               jmp $+2 ;Short io pause<br>inc dx ;Address of the
                                                  ;Address of the index register
```
in al,dx ;Read content to AL ret in Back to caller ; Back to caller getvk endp ;-- SCROLLUp: scrolls a window by N lines upward --------------------- ;-- Input BL - line upper left **;--** BH - column upper left **;--** DL - line lower right **;--** DH - column lower right **;--** CL - number of the lines to be scrolled **;--** BF - number of the display page (0 or 1) ;-- OUtput **none**  ;-- Info : the display lines released are erased scrollup proc near cld push ax push bx push di push si push bx push cx push dx sub dl,bl inc dl sub dl,cl sub dh,bh inc dh call calo mov si,di add bl,cl call calo xchg si,di push ds push es mov ax, VIO SEG mov **ds,ax**  mov **es,ax**  supl: mov ax,di mov bX,si mov cl,dh **rep movsw**  mov di,ax mov si,bx add di,160 add si,160 dec dl jne sup1 pop es pop ds pop dx pop cx pop bx mov bl,dl sub bl, cl<br>inc bl mov ah,07h call clear pop si pop di pop ax ret ;Increment for string instructions ;Store all changed registers ; on the stack ;In this case the sequence ; must be followed ! ;These three registers are returned ;from the stack before ;the end of the routine ;Calculate number of lines ;Deduct number ;of lines to be scrolled ;Calculate number of columns ;Convert upper left in offset ;Note address in SI ;First line in scrolled window ;Convert first line in offset ;Exchange S1 and D1 ;Store segment register ; on the stack ;Segment address of the video RAM to DS ; and ES ;Note D1 in AX ; Note SI in BX ;Number of columns in counter ;Move a line ;Restore D1 from AX ;Restore S1 from BX ; Set next line ;Processed all lines ? ;NO --> move another line ;Get segment register from ; stack ;Get lower right corner ;Get number of lines ;Get upper left corner ;Lower line to BL ;Deduct number of lines ;Color : black on white ;Erase liberated lines ;CX and DX have been brought back ; already ;Back to caller
$\dot{f}$ 

scrollup endp **;--** SCROLLDN: scroll a Window by N lines upwards --------------------- **i--** Input BL - line upper left *i--* BH - column upper left **i--** DL - line lower riqht *i--* DH - column lower riqht ;-- : BP = number of the display page (0 or 1) ;-- Output : none ;-- register : only FLAGS are changed<br>;-- Info : released lines are dele : released lines are deleted scrolldn proc near cld :Increment on string instructions \ push ax ;Secure all chanqed reqisters on the push bx ; stack<br>push di ; In thi push di ;In this case the sequence must ; be followed! push bx ;These three registers are<br>push cx ;These three registers are push cx ; push cx ; puturned from the stack before the push dx  $\cdot$  : end of the routine ; end of the routine sub dh, bh ;Calculate number of columns inc dh<br>mov al,bl mov al, bl ;Record line upper left in AL<br>mov bl, dl ;Line lower right top lower left mov bl,dl ;Line lower right top lower left<br>call calo ;Convert upper left in offset call calo : convert upper left in offset<br>
mov si,di ;Note address in SI mov si, di ;Note address in SI<br>sub bl,cl ;Deduct number of chars to scroll<br>call calo ;Convert upper left in offset call calo  $\begin{array}{ll}\n\text{convert upper left in offset} \\
\text{for } \text{set } \text{in} \\
\text$ xchq si,di ;Exchange SI and DI<br>sub dl,al ;Calculate number o ;Calculate number of lines inc dl<br>sub dl,cl sub dl,cl ;Deduct number of lines to scroll<br>push ds :Store segment register on the push ds ;Store segment register on the push es :stack push es ; stack<br>mov ax, VIO SEG ; Segment ;Segment address of the video RAM<br>;to DS **rnov** ds, ax **ito** DS<br> **rnov** es, ax **i** and ES<br> **rnov** ax, di **i** Record DI in AX sdnl: mov ax,di ;Record DI in AX<br>mov bx,si ;Record SI in BX<br>mov cl,dh ;Number of column mov cl,dh ;Number of columns in counter<br>rep movsw ;Move a line rep move di, ax ; Restore DI from AX<br>move si, bx ;Restore SI from BX mov si,bx ;Restore SI from BX<br>sub di,160 :Set next line ; Set next line sub si,160<br>dec dl dec dl ;All lines processed jne sdn! ;NO --> move another line pop es ;Get segment register from<br>pop ds ;stack pop ds ; stack pop cx ;Get number of lines<br>pop bx ;Get upper left corne pop bx **j**Get upper left corner<br>
mov dl,bl **j**Upper line to DL mov dl,bl ; Upper line to DL<br>add dl,cl ;Add number of li ; Add number of lines dec dl<br>mov ah, 07h mov ah, 07h ; Color : black on white<br>
call clear : Erase liberated lines ;Erase liberated lines pop si  $\bigcup_{\text{p} \text{ open}}$  cX and DX have already pop di ; been read pop bx pop ax ret ;Back to caller

```
scrolldn endp 
;- cLS: clear the whole screen ------------------------------------- ;-- Input BP - number of the display page (0 or 1) 
i-- OUtput none 
;-- register : only FLAGS are changed
cIs 	 proc near 
            mov ah, 07h ;Color is white on black<br>xor bx, bx ;Upper left is (0/0)
            xor bx,bx ; Upper left is (0/0)<br>mov dx,4F18h ; Lower right is (79/
                                        ; Lower right is (79/24):-- perform clear ---
cls endp
;-- CLEAR: fills a designated display area with space character ------
;-- Input : AH = Attribute/color<br>;-- BL - line upper left<br>;-- BH - column upper left<br>;-- DL - line lower right
;-- DH = column lower right<br>;-- BP = number of the display page (0 or 1)
;-- Output none 
;-- register : only FLAGS are changed
clear proc near
            cld \begin{array}{ccc} \text{cld} \\ \text{push cx} \end{array} ; Secure all changed
            push cx ; Secure all changed<br>push dx ; registers on the st
                                         ; registers on the stack
            push si 
            push di 
            push es<br>sub dl,bl
                                        ; Calculate number of lines
            inc dl<br>sub dh,bh
                                        ;Calculate number of columns
            inc dh 
            call calo ;Offset address of upper left corner 
            mov cx,VIO_SEG ;Segment address of the video RAM<br>mov es,cx ;to ES
            mov es,cx Ito ES xor ch,ch ;Hi byte of the counter to 0 
            mov al," b<br>"
nov si,di ;Note DI in SI
clearl: mov si,di ;Note DI in SI<br>mov cl,dh ;Number of colu
                                      ;Number of columns in counter
            rep stosw ;Store space character
            mov di,si ;Restore DI from SI<br>add di,160 ;Set next line
            add di,160 ; Set next line 
            dec dl ;All lines processed 
                                        ;NO --> erase another line
            pop es ;Get secured registers 
            pop di ; from the stack 
            pop si 
            pop dx 
            pop cx 
            ret ; Back to caller
clear 	 endp 
;-- PRINT: outputs a string on the display -----------<br>;-- Input : AH = attribute/color<br>;-- DI = offset address of the first chara
;-- DI = offset address of the first character<br>;-- SI = offset address of the strings to DS
;-- SI = offset address of the strings to DS<br>;-- BP = number of the display page (0 or 1)
                BP = number of the display page (0 or 1);-- Output : DI points behind the last character to be output
;-- register : AL, DI and FLAGS are changed
;-- Info : the string must ne terminated with NUL-character.
```


**i--** other control characters are not recognized print **proc** near cld ;Increment on string instructions<br>push si :SI. DX and ES to the stack :SI, DX and ES to the stack push es push dx<br>mov dx, VIO SEG mov dx,VIO\_SEG ;First segment address of video RAM<br>
mov es,dx ;to DX and then to ES<br>  $\text{Jmp}$  print1 ;Get first character from string jmp print1 ;Get first character from string<br>stosw :Store attribute and color in V-1 print0: stosw ;<br>print1: lodsb ;Store attribute and color in V-RAM<br>contracter from the string; ;Get next character from the string or al, al  $\begin{array}{ccc} ;1s & \text{it NUL} \\ \text{the print0} & ;N0 & \text{--> ou} \end{array}$ ;NO --> output printe: pop dx ;Get SI, DX and ES from stack again pop es pop si<br>ret : Back to caller print endp ;-- cALO: converts line and column into offset address ---------------<br>;-- Input : BL = line<br>;-- BH = column **i--** Bp = number of the display page (0 or 1) <br> **;--** Output : DI = offset address<br> **;--** register : DI and FLAGS are changed calo proc near push ax ;Record AX on the stack<br>push bx ;Record BX on the stack ; Record BX on the stack shl bx, 1 ;Column and line times 2<br>mov al, bh ;Column to AL ;Column to AL<br>;Hi byte xor bh,bh<br>mov di, [lines+bx] mov di, [lines+bx] ;Get offset address of the line<br>xor ah,ah ;Hi byte for column offset<br>add di.ax ;Add lines- and column offset add di,ax ;Add lines- and column offset<br>or bp,bp ;Display page 0? or bp,bp ;Oisplay page 01 ;YES --> address ok add di,8000h ;Add 32 KB for display page 1 caloe: **pop bx** ;Get BX from stack again<br>
pop ax ;Get AX from the stack again<br>
ret :Back to caller : Back to caller calo endp **i--** CGR: clear the complete graphic screen --------------------------- **;--** Input BP - number of the display page (0 or 1) **;--** AL - OOH erase all pixels *i* -- Output : none  $:=$  register : AH, BX, cX, DI and FLAGS are changed cgr proc **near**  push es **iRecord ES** on the stack<br>cbw **iPs**<br>**Expand AL** to AH xor di,di ;Offset address in video RAM<br>mov bx,VIO SEG ;Segment address display page mov bx, VIO\_SEG ; Segment address display page 0<br>or bp, bp ; Erase page 1? or bp,bp ;Erase page 11 ;NO --> erase page 0 add bx,0800h ;Segment address display page 1

```
cgr1: 
cgr 
;-- SPIX: sets a pixel in the graphic display ----------------------------------<br>;-- Input : BP = number of the display page (0 or 1)
i-
i-
;-- DX =<br>
;-- Output : none
             mav es,bx 
             mov cX,4000h 
             rep stosw 
             pop es 
             ret 
             endp 
                                            ;Segment address to segment register 
                                            ;A page is 16K-words 
                                           ;Fill page 
                                           ;Get ES from stack 
                                            ; Back to caller 
                    BP = number of the display page (0 or 1)BX - column (0 to 719) 

                  DX = line (0 to 347);-- register : AX, DI and FLAGS are changed
spix 
spixl: 
spix 
             proc near 
             push es 
             push bx 
             push ex 
             push dx 
             xor di,di 
             mov cx, VIO_SEG<br>or bp, bp
             je spixl 
             mov cX,OBOOh 
             mov es,cx 
             mov aX,dx 
             shr aX,1 
             shr ax,l 
             mov cl,90 
             mul cl 
             and dx,1lb 
             mav el,3 
             ror dx,cl 
              mov di,bx mov cl,3 
              shr di,cl<br>
add di, dx<br>
add di, dx<br>
mov cl, 7<br>
and bx, 7<br>
sub cl, bl
             mov ah,l 
             shl ah,cl 
              mov al,es:[di]<br>or al,ah<br>mov es:[di],al
             pop dx 
             pop ex 
             pop bx 
             pop es 
             ret 
             endp 
                                          ;Store ES on the stack 
                                          ; Store BX on the stack
                                              ; Store eX on the stack 
;Store DX on the stack 
                                              ;Offset address in video RAM<br>;Segment address display page 0
                                              ;Access page 1 ? 

;NO --> access page 0 
                                          ;Segment address display page 1 
                                              ;Segment address in segment register 
;Move line to AX 
;Shift line right 2 times 
                                              ,This divides by four 
;The factor is 90 
;Multiply line by 90 
;AND all bits except for 
0 and 1 
                                          ;3 shifts 
                                          ;Rotate right (* 2000H) 
                                              ;Column to DI 
;3 shifts 
                                              ;divide by B 
;+ 90 * int(line/4) 
;+ 2000H * (line mod 4) 
;Maximum of 7 moves 
;Column mod B 
;7 - column mod B 
                                           ;Determine bit value of the pixels 
                                              ; Get 8 pixels 
                                              ; Set pixel 
                                           ;Write B pixels 
                                          ;Get DX from stack 
                                           ;Get eX from stack 
                                            ;Get BX from stack
                                           ;Get ES from stack 
                                           ; Back to caller 
;== End ===================-=-=====================----========-======= 
code ends ;End of the code segmentend demo
```
# **10.4 The IBM Color Card**

The IBM Color/Graphics Adapter (CGA) supports two text modes and three different graphic modes. Like the other two cards, the CGA is based on a 6845 video processor and is equipped with 16K of video RAM which begins at address B800:0000.

# Text modes

Besides the normal text mode of 25 lines and 80 columns, the CGA also has a text mode consisting of 25 lines and 40 columns. This 40-column mode displays characters twice as wide as normal 8O-column mode. CGA characters are displayed in an 8x8 matrix, which results in a less distinct display than monochrome display adapter text. The CGA's video RAM assignment is almost identical to that of the monochrome card. The attribute byte is different from that of the monochrome display adapter.



*Color/Graphics Adapter attribute byte* 

The lower four bits of the attribute byte indicate one of the 16 available colors. The meanings of the upper four bits depend on whether blinking is active. If it is active, bits 4 to 6 indicate the background color (taken from one of the first eight colors of the color palette), while bit 7 determines whether or not the characters blink. If blinking is disabled, bits 4 to 7 indicate the background color (taken from one of the 16 available colors).



#### *Color/Graphics Adapter color palette*

Each 80x25 text page requires 4,000 bytes of video RAM. 16K allows a total of four text pages. The first display page starts at address B800:0000, the second at B800:1000, the third at B800:2000 and the last at B800:3000. The 4Ox25 mode allows storage of eight display pages, because each display page only requires 2,000 bytes in this mode. The first display page starts at address B800:0000, the second at B800:0800, the third at B800:1000, etc.

# **Graphic** modes

The CGA supports three different graphic modes, of which only two are usually used. The *color-suppressed* mode displays 160xl00 pixels with 16 colors. The 6845 supports this resolution, but the rest of the hardware doesn't offer colorsuppressed mode support. The remaining two graphic modes have resolutions of 32Ox200 and 640x200 respectively. The 32Ox200 resolution permits four-color graphics, while 640x200 resolution only allows two colors.

# **320x200 resolution**

The CGA uses up all 16K of its video RAM for displaying a graphic in  $320x200$ resolution with four colors. This limits the user to one graphic page at a time. Of the four colors permitted, the background can be selected from the 16 available colors. The other three colors originate from one of the two user-selected color palettes, which contain three colors each.



Since a total of four colors are available, each screen pixel requires two bits. Four bits can represent the color numbers (0 to 3). The following values correspond to the various colors:



 $11(b) = \text{color 3 of the selected palette}$ 

The video RAM assignment in this mode is similar to that of the Hercules card during graphic display. The individual graphic lines are stored in two different blocks of memory. The frrst block, which begins at address B800:0000, contains the even lines  $(0, 2, 4...)$ ; the second block, which begins at B800:2000, contains odd lines (1,3,5).



#### *Video RAM assignment in graphic mode (blocking)*

Each graphic line within the two blocks requires 80 bytes, since the 320 pixels in a line are coded into four pixels to a byte. The first byte in a graphic line (an 80 byte series) corresponds to the frrst four dots of the graphic on the screen. Bits 7 and 8 contain the color information for the leftmost pixel, while bits 0 and 1 contain the color information for the rightmost pixel of the byte.



*Graphic line coding in 320x200 resolution* 

A formula can be derived with the help of this information to determine the byte in video RAM, similar to the Hercules card. This byte is relative to the starting address of the screen page, which contains the color information for a pixel. The screen column  $(0-319)$  is designated as X and the screen line  $(0-199)$  as Y:

Address = 2000H \* (Y mod 2) + 80 \* int(Y/2) + int(X/4)

To detennine the number of the two bits within this byte which represents the pixel, use the following fonnula:

Bit number =  $6 - 2 * (X \mod 4)$ 

For example, if this formula returns 4, this means that the color information for the dot is coded into bits 4 and 5.



*Graphic line coding in 640x200 resolution* 

# 640x200 resolution

High-resolution mode with a resolution of 64Ox200 dots only allows the use of two colors. The video RAM assignment in this mode is similar to 320x200 mode. Each line displays twice as many pixels, with one bit encoding the line instead of 2 bits. Because of this, one screen line requires 880 bytes. Therefore the formulas for access to a screen pixel are similar.

```
Address = 2000H * (Y mod 2) + 80 * int(Y/2) + int(X/8)
Bit number = 7 - (X \mod 8)
```
# CGA registers

The CGA has a mode selection register at address 3D8H which is comparable with the control register of the monochrome display adapter. You can write to this register but not read it.





#### Bit layout

Bit 0 of this register determines the text mode display of 80 or 40 columns per line. A 1 in bit 0 displays 80 columns, while a 0 in bit 0 displays 40 columns.

The status of bit 1 switches the CGA from text mode to the  $320x200$  bit-mapped graphic mode. A 1 in this register selects graphic mode, while a 0 selects text mode.

Bit 2 should be of interest to any users who want to operate their CGA with a monochrome monitor. If this bit contains the value 1, the 6845 suppresses the color signal, displaying monochrome mode only.

Bit 3 is responsible for creating screens. If it contains the value 0, the screen remains black. This suppression is useful when changing between display modes; it prevents sudden signals from reaching the monitor which could cause damage.

Bit 4 enables and disables 640x200 bitmapped graphic mode. A 1 in bit 4 enables this mode, while a  $0$  disables it.

Bit 5 has the same significance as in the monochrome card. If it contains a 0, blinking stops and bit 7 returns one of the 16 available background colors. This bit contains a default value of 1, which causes blinking characters.

The various text or graphic modes and the color or monochrome display can be selected in these modes with this register. Bits 0, 1, 2 and 4 are used for this. The following table shows how these bits must be programmed to obtain certain modes:



The CGA also has a status register similar to the status register in the monochrome display adapter. The following figure shows the construction of this register, which can be found at address 3DAH. It is a read-only register.



*Status register structure* 

Bit 0 of this register always contains the value 1 when the 6845 sends a horizontal synchronization signal to the monitor. This signal is transmitted when the creation of a line ends and the CRTs electron beam reaches the end of the screen line. The electron beam then jumps back to the left comer of the screen line. The bit gets its significance from the condition that the CGA doesn't always allow data reading or writing within video RAM.

#### Flickering and the CGA

This problem occurs because the 6845 must continuously access video RAM to read its contents for screen display. If a program tries to transmit data to video RAM, problems can arise when the 6845 accesses video RAM at the same time. The result of this memory collision is an occasional flickering on the screen.

To avoid this problem, you should only access video RAM when the 6845 is not accessing it. This only occurs when a horizontal synchronization signal travels to the screen, because it requires a moment of time until the electron beam has carried out this instruction. For this reason, the status register must be read before every video RAM access on a CGA. This process must be repeated until bit 0 contains the value 1. When this happens, a maximum of two bytes can then be transmitted to video RAM.

#### Demonstration program

The program at the end of this section demonstrates how this process functions. This delay in video RAM access doesn't occur with monochrome cards because they are equipped with special hardware logic and fast RAM chips. This is also true of most of the newer model color cards. Before waiting for the horizontal synchronization signal, which results in an enormous delay of the display output, the user should try direct access to video RAM to test his color card's reaction time.

If many accesses to video RAM occur within a short period of time (e.g., scrolling the screen), the electron beam doesn't respond fast enough. The screen should be switched off using bit 3 of the mode selection register. This prevents the 6845 from accessing video RAM, permitting unlimited user access to video RAM. When data transfer ends, the screen can be switched on again. BIOS uses this method during scrolling. which results in the flickering "silent movie effect."

# Color selection register

The color selection register is located at address 3D9H. This register is write-only (cannot be read).



#### *Color selection register*

The meanings of individual bits in this register depend on the display mode. Text mode uses the lowest four bits for assigning the background color from the 16 available colors. In 320x200 graphic mode, these four bits indicate the color of all pixels represented by the bit combination 00{b) (background color).

Bit 5 selects the color palette for 320x200 mode. If this bit contains the value I, the first color palette (cyan, violet, white) is selected. A value of 0 selects the second color palette (green, yellow, red).

#### Internal registers

The 18 internal registers of the 6845 on this card are accessed exactly like the monochrome card. The only difference is that the index and the data register are located at 3D4H and 3D5H. The following table shows the contents which the register must have for various display modes.



These registers are of interest to the user since they define the position and appearance of the cursor on the screen. Section 10.1 described programming these registers. The CGA adds registers 12 and  $\Delta$ 3. They indicate the start of the video page which must be displayed on the screen, as offset of the beginning of the 16K RAM on the card (B800:0000), divided by 2. Register 12 contains the most significant 8 bits of this offset, while register  $13$  contains the least significant 8 bits. Normally both registers contain the value 0, displaying the frrst screen page (beginning at the address B800:0000) on the screen. For display of the first screen page, which begins at location B800:1000 in the 8Ox25 text mode, the value l000H divided by 2 (8ooH) must be entered in both registers.

The last of the three programs in this chapter accesses the color/graphics adapter. The only significant difference between the two preceding programs lies in the fact that the video controller can synchronize video RAM access and screen construction. This is necessary on all video cards where direct access to video RAM causes a flickering on the screen. The WAIT constant, defmed directly after the program header, switches synchronization on or off. Its contents decide during the assembly of the program, whether to assemble the program lines for synchronization listed in the source listing. These lines would slow down the screen considerably, and should only be included if it is absolutely necessary.

#### Assembler listing: VCOL.ASM

*i··\*\*\*\*\*\*\*\*\*\*·\*\*\*\*\*\*\*··\*\*···\*\*·········\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*······\*\*\*\*\*\*\*\*i*   $\mathbf{v} \in \mathbb{R}^*$  , where  $\mathbf{v} \in \mathbb{R}$  , we have  $\mathbf{v}$  and  $\mathbf{v}$ :\*------------ --\*: ;\* Task : Makes some basic functions available for \*; ;\* access to the Color Graphics Adapter (CGA) \*; %/\* Info : All functions subdivide the screen  $\begin{array}{lll} \star \star & \text{info} & \text{ 1} \star \star \\ \star \star & \text{info} & \text{columns} \circ \text{to} & \text{?9} \text{ and lines} \circ \text{to} & \text{?4} \end{array}$ ;\* into columns 0 to 79 and lines 0 to 24 \*;<br>;\* in text mode and into columns 0 to 719 and \*; ;\* in text mode and into columns 0 to 719 and \*;<br>;\* the lines 0 to 347 in graphic mode. \*; ;\* the lines 0 to 347 in graphic mode. \*;<br>;\* the 40 column text mode is not supported ! \*; ;\* The 40 column text mode is not supported !<br>I \* A high resolution graphic screen should ap ;\* The a high resolution graphic screen should appear\*;<br>"
first, followed by a text screen. If the high \*; ;\* first, followed by a text screen. If the high \*;<br>"
res screen doesn't appear, try running the \*; ;\* res screen doesn't appear, try running the \*; ;\* program a few times in succession. \*; *i\*---*----------\*: ;\* Author : MICHAEL TISCHER  $\qquad \qquad \qquad \rightarrow ;$ <br>;\* Developed on : 8/13/87  $\qquad \qquad \rightarrow ;$ ;" Developed on *: 8/13/87* "; ;\* Last update : *6/16/89* "; ;\*---\*; ;" assembly MASH VCOL (program will assemble with one "; ;" warning - it WILL link & run) "; ;\* LINK VeaL; \*; ;\*--*-----------\*i*   $; *$  Call : VCOL  $*;$ *i\*·\*i*   $:=$  Constants  $:$ CONTROL REG - 03D8h ;Control register port address CCHOICE\_REG = 03D9h ;Color select register port address<br>ADDRESS 6845 = 03D4h ;6845 address register  $ADDESS = 6845 = 03D4h$ <br> $26845 = 03D5h$  ;6845 address register<br> $26845 = 03D5h$  ;6845 data register  $DATA_6845 = 03D5h$  ;6845 data register<br>VIO SEG = 0B800h :Video RAM secment a VIO SEG = 0B800h ; Video RAM segment address<br>
CUR START = 10 ; Reg  $\frac{1}{2}$  for CRTC: Cursor st CUR\_START =  $10$  ;Reg  $\frac{1}{2}$  for CRTC: Cursor start line<br>  $CUR$  END =  $11$  :Reg  $\frac{1}{2}$  for CTRC: Cursor end line  $CUR \subseteq \text{END}$  = 11 ;Reg  $\#$  for CTRC: cursor end line<br>  $CUR \subseteq \text{NIP}$  = 12 ;Page address (high byte) CURPG\_HI = 12 ;Page address (high byte)<br>
CURPG\_LO = 13 ;Page address (low byte)<br>
CURPOS HI = 14 :Req  $\#$  for CRTC: Cursor p CURPOS\_HI = 14 ;Reg  $\#$  for CRTC: Cursor pos high byte<br>
CURPOS\_LO = 15 ;Reg  $\#$  for CRTC: Cursor pos low byte CURPOS\_LO = 15 ;Reg  $\#$  for CRTC: Cursor pos low byte<br>DELAY = 20000 :Counter for delay loop : Counter for delay loop i-= Macros -===--===-===---==-==--~---=- ;-- SETMODE : Macro for configuring screen control register ------- setmode macro modus mov dx,CONTROL\_REG ;Address of the display control register<br>mov al,modus ;New mode into the AL register mov al, modus ;New mode into the AL register<br>out dx, al ;Send mode to control register ; Send mode to control register endm ;-- WAITRET: waits until display is completed waitret macro<br>local wrl : Local label mov dx,3DAh ;Address of the display status register wrl: in al,dx ;Get content

local wr1 ; Local label mov dx,3DAh ;Address of the display status register<br>in al,dx ;Get content wr1: in al,dx ;Get content<br>test al,8 ;Vertical retrace?<br>de wr1 :NO --> wait ;NO --> wait **;- Stack ---------------** endm stack segment para stack ;Definition of stack segment dw 256 dup (?) ;256-word stack stack ends ;End of stack segment **;- Data ---=----------------=-----** data segment para 'DATA' ;Definition of data segment ;== Data required for demo program ============== initm  $db 13,10$ db "VCOL (c) 1988, 1989 by Michael Tischer " db 13,10,13,10 db "This demo program only runs with a Color/Graphics",13,10 db "Adapter ( CGA). If your PC uses another type of", 13, 10 db "video card press the <s> key to stop the program.",13,10 db "Press any other key to start the program...", 13, 10, "\$"  $str1$  db  $1,0$  $;==$  Table of offset addresses of line beginnings  $===========1$  lines dw  $0*160. 1*160. 2*160$  :start addresses of the line dw  $0*160$ , 1\*160, 2\*160 ;start addresses of the lines as<br>dw 3\*160, 4\*160, 5\*160 ;offset addresses in the video RAM dw 6\*160, 7\*160, 8\*160 dw 9\*160,10\*160,11\*160,12\*160,13\*160,14\*160,15\*160,16\*160 dw 17\*160,18\*160,19\*160,20\*160,21\*160,22\*160,23\*160,24\*160 graphict db 38h, 28h, 2Dh, 0Ah, 7Fh, 06h ; register values for the db 64h, 70h, 02h, 01h, 06h, 07h ; graphic-modes textt db ?lh, SOh, SAh, OAh, 1Fh, 06h ; register-values for the db 19h, 1Ch, 02h, 07h, 06h, 07h ;graphic-modes wait db 0  $;$  ;TRUE (<>0) when caller uses the ;/F switch data ends ;End of data segment  $:=$  Code  $=$ code segment para 'COOE' ;Definition of the COOK segment assume cs:code, ds:data, es:data, ss:stack ;== This 1s only the Demo-Program =-==-====-===---===--~-------=== demo proc far ;-- Look for *IF* from DOS prompt ---------------------- mov cl,ds:128 ;Get number of bytes from prompt<br>or cl,cl :No parameters given? or cl,cl ;No parameters given?<br>je switchl ;NO --> Ignore mov bx, 129 ;BX points to first byte in prompt<br>
mov ch, bh ;Set loop high byte to 0 ; Set loop high byte to 0 switch: cmp [bx], "F/" ;Switch in this position?

je switchl cmp [bx], *"fI"*  je switchl inc hl loop switch switchl: mov ax.data mov **ds,ax**  mov **eS,ax**  mov wait,cl ;YES --> switch found ;Switch in this position? ;YES --> Switch found ;Set BX to next character ;Check next character ;Get segment addr. of data segment ;and load into OS ;and ES ; Set WAIT flag ;-- Display init message and wait for input ----------- mov ah,9 mov dX,offset int 21h xor ah,ah int 16h cmp al, "s" je ende cmp **al/"S"**  jne startdemo ende: mov ax, 4C00h int 21h startdemo label near call grafhi xor al,al call cgr xor bX,bx xor dX,dx mov aX,199 mov cx,639 grl: push cx mov cx, ax<br>push ax mov al,l gr2: call pixhi inc dx loop gr2 pop ax sub ax, 3 pop cx push cx push ax mov al,l gr3: call pixhi inc bx loop gr3 pop ax pop cx sub ex, 6 push cx mov **ex,ax**  push ax mov al,l gr4: call pixhi dec dx loop gr4 pop ax sub **ax,3**  pop cx push cx push ax mov al,l gr5: call pixhi ;Function number for string display ; Address of intial message ;Call DOS interrupt 21H ;Function number: get key ;Call BIOS keyboard interrupt ;<s> key pressed? ;YES --> End program ;<S> key pressed? ;NO --> Start demo ;Function number: End program ;Call DOS interrupt 21H ;switch on 320\*200 pixel graphic ;Clear graphic display ;Column 0 ;Line 0 ; Pixels-vertical ; Pixels-horizontal ;Record horizontal pixels <sub>.</sub><br>Necord vertical pixels on the stack;<br>Record vertical pixels on the stack; ; Set pixel ; Increment line .<br>;Draw line<br>;Get vertical pixels from the stack ;Next line 3 pixels less ;Get horizontal pixels from the stack ;Record horizontal pixels ;Record vertical pixels on the stack ;Set pixel ;Increment column ;Draw line ;Get vertical pixels from stack ;Get horizontal pixels from stack ;Next line 6 pixels less ;Record horizontal pixels ;Vertical pixels to counter ;Record vertical pixels on the stack ;Set pixel ; Decrement line ;Draw line ;Get vertical pixels from stack ;Next line 3 pixels less ;Get horizontal pixels from stack ;Record horizontal pixels ;Record vertical pixels on the stack ;Set pixel

demol: demo2: demo dec bx loop grS pop ax pop ex sub ex, 6 cmp ax,S ja grl xor ah,ah int l6h call text xor bp,bp mov al,30h or ax,bp mov strl,al<br>call setcol call setcol call setpage call cIs xor bx,bx call calo mov cx,2000 xor ah,ah xor ah,ah<br>mov si,offset strl inc ah call print loop demo2 xor ah,ah int l6h inc bp cmp bp,4 jne demol xor bp,bp call setpage jmP ende endp ;== The actual functions follow ============================= ;Increment column ;Draw line ;Get vertical pixels from the stack ;Get horizontal pixels from the stack ;Next line 6 pixels less ;Is the vertical line longer than S ;YES--> continue ;Wait for function number of key wait ;Call BIOS keyboard interrupt ;Switch on 80x25 character text mode ;Process screen page 0 first<br>;ASCII code "0" ;Convert page number to ASCII ;Store in string ;Set color ;Activate screen page in BP ;Clear screen page ;Begin in the upper left ;Screen corner with output ;A page contains 2,000 characters ;Start with color code 0 ;Start with color code 0<br>;Offset address of string 1 ;Increment color value ;Output string 1 ;Repeat until screen is full ;Wait for key ;Call BIOS-Keyboard-Interrupt ;Increment page number ;All 4 pages processed ? ;NO --> then next page ;Activate page 0 again ;Goto program end  $;--$  TEXT: switches the text display on -------<br> $;--$  Input : none ;-- Output none ;-- Register : AX, SI, BH, OX and FLAGS are changed text proc near mov si,offset textt ;Offset address of the register-table mov bl,00100001b ;80x25 text mode, blinking<br>jmp short vcprog ;Program video controller again text endp ;-- GRAFHI: switches the 640\*200 pixel graphic mode on ----------------<br>;-- Input : none ; -- Output : none ;-- Register : AX, SI, BH, OX and FLAGS are changed grathi proc near mov bl,OOOlOOlOb ;Graphic mode with 640"200 pixels jmP short graphic ;Program video controller again grafhi endp ;-- GRAFIO: switches the 320\*200 pixel graphic mode on ----------<br>;-- Input : none ;-- Output : none ;-- Register: AX, SI, BH, OX and FLAGS are changed

```
graflo proc near
             mov bl,00100010b ;Graphic mode with 320*200 pixels 
graphic: mov si, offset graphict ; Offset address of the register table
graflo endp
;-- VCPROG: programs the video controller -----------------------------<br>;-- Input     : SI = Address of a register table
;- BL - Value for display control register ;-- OUtput none 
;-- Output : none<br>;-- Register : AX, SI, BH, DX and FLAGS are changed
veprog proc near
             setmode bl :Bit 3 = 0: screen off
             mov cx, 12 ;12 registers are set<br>xor bh, bh ;Start with register
              xor bh,bh ;Start with register 0<br>lodsb :Get register value fr
vcp1: lodsb ;Get register value from table<br>mov ah,al ;Register value to AH
              mov ah,al ;Register value to AH<br>mov al,bh ;Number of the registe
              mov al, bh ;Number of the register to AL<br>call setvk ;Transmit value to controller
              call setvk ;Transmit value to controller<br>inc bh :Address next reqister
              inc bh ; Address next register<br>loop vcpl ; Set additional regist
                                              ;Set additional registers
              or bl,8 ;Bit 3 = 1: screen on<br>setmode bl ;Set new mode
              ret ;Back to caller
vcprog endp
;-- SETCOL : Sets the color of the display frame and Background ----
 ;-- Input : AL = color value<br>;-- Output : none
;-- register : AX and DX are changed<br>;-- Info : in text mode the lowe
;-- Info in text mode the lowest 4 bits indicate the frame color ;- in graphic mode the lowest 4 bits indicate the frame ;-- and background color, bit 5 selects the color palette 
setcol proc near
              mov dx,CCHOICE_REG ;Address of the color selection register<br>out dx,al :Output color value<br>ret :Back to caller
                                               ; Back to caller
setcol endp
j \rightarrow CDEF : sets the start and end line of the cursor ---------------<br>j \rightarrow Input : CL = start line j \rightarrow<br>j \rightarrow Output i none ii end line ii and i in the ii and i and i and i and i and i and i and 
;-- register : AX and DX are changed
cdef 	 proc near 
              mov al, CUR_START ;Register 10: start line<br>mov ah, cl ;Start line to AH
              mov ah,cl \overline{\phantom{0}} call setvk
              call setvk ;Transmit to video controller<br>mov al,CUR END ;Register 11: end line
              mov aI, CUR_END ;Register 11: end line mov ah,ch ;End line to AH 
                                             ;Transmit to video controller
 cdef endp
 := - SETPAGE : sets the screen page --
  ;- Input BP - Number of the screen page (0 to 3) 
 i-- Output none 
 :- register : BX, AX, CX and DX are changed
```
 $;--$  Info : in the Graphic modes the first screen page has the  $;--$  number 0, the second the number 2 number 0, the second the number 2 setpage **proc near**  mov bx, bp ; Screen page to BX<br>mov cl, 5 ; Multiply by 2,048 ;Multiply by 2,048 **ror bx,cl**  mov al,CURPG\_HI ;Register 12: Hi byte page address<br>mov ah,bh : ;Hi byte of the screen page to AH<br>call setvk ;Transmit to video controller call setvk ;Transmit to video controller<br>mov al,CURPG\_LO ;Register 13: Lo byte page address mov al, CURPG LO ;<br>mov ah,bl : lo byte of the screen page to AH<br>jmp short setvk ; Transmit to video controller ;Transmit to video controller setpage endp **;--** SETBLINK sets the blinking cursor ------------------------------ **i--** Input 01 = Offset address of the cursor **i--** Output **none**   $:-$  register : BX, AX and DX are changed setblink proc near mov bx,di ;Move offset to BX<br>mov al,CURPOS\_HI ;Hi byte of the cursor offset<br>mov ah,bh - ;HI byte of the offset<br>call setvk ;Transmit to video controller call setvk ; Transmit to video controller<br>mov al, CURPOS LO ; Lo byte of the cursor offset mov al, CURPOS<sub>\_</sub>LO ;Lo byte of the cursor offset<br>mov ah,bl :Lo byte of the offset ;-- SETVK is called automatically ------------------------- setblink endp  $;--$  SETVK : sets a byte in one register of the video controller ----<br> $;--$  Input : AL = Number of the register ;-- **Input AH** = new content of the register ;-- Output **none**  ;-- register : DX and AL are changed setvk **proc near**  mov dx, ADDRESS\_6845 ; Address of the index register out dx, al  $\begin{array}{ccc} 1 & 1 & 1 \end{array}$  ; Send number of the register<br>  $\begin{array}{ccc} \text{Imp} & \text{short} & \text{ $5+2$} \end{array}$  ; Short I/O pause jmp short \$+2 ;Short *1/0* pause inc dx **;Address of the index register** mov **al,ah ;Content to AL** out dx,al **;** Set new content ret ; Back to caller setvk endp *j*-- GETVK : gets a byte from one register of the video controller -<br>*j*-- Input : AL = Number of the register : AL = Number of the register  $i$ -- Output : AL = Contents of register  $:=$  register : DX and AL are changed getvk proc **near**  mov dx,ADORESS\_6845 ;Address of the index register out dx, al  $\overline{\phantom{a}}$  ; Send number of the register<br>inc dx  $\overline{\phantom{a}}$ ; Index register address inc dx ;Index register address<br>imp short \$+2 ;Short io pause jmp short \$+2 ; Short io pause<br>in al,dx ; Set new content in al,dx **in the set of set of the set of the** ; Back to caller getvk endp ;-- SCROLLUP: scrolls a window N lines upward --------

**i--** Input **;-**  $; --$ **;- ;- ;- ;--** OUtput **none**  : BL = line upper left BH - column upper left  $DL = line below right$  $DH = column$  below right  $CL =$  Number of lines, to be scrolled BP - Number of the screen paqe (0 to 3) **;--** register : only FLAGS are changed<br>;-- Info : the display lines liberated are cleared scrollup proc near cld push ax push bx push di push si push bx push ex push dx sub dl,bl inc dl sub dl,cl sub bh,dh inc dh call calo mov si,di add bl,cl call calo xchq si,di anp wait, 0 je supO waitret setmode OOlOOlQlb sup0: push ds push es mov ax,VIO\_SEG mov **ds,ax**  mov **es,ax**  supl: mov ax,di mov bx,si mov cl,dh **rep movsw**  mov di,ax mov si,bx add di,160 add si,160 dec dl jne sup1 pop es pop ds anp wait,O je sup2 setmode 00101101b sup2: pop dx pop ex pop bx mov bl,dl sub bl,cl inc bl iOn strinq commands count up ;All chanqed reqisters to the ;Secure stack ;In this case the sequence ; must be observed ! ;These three reqisters are returned ;before the end of the routine ; From t he stack ;Calculate the number of lines ;Subtract number of lines to be scrolled ;Calculate number of columns ;Convert upper left in offset ;Record address in SI ;First line in scrolled window ;Convert first line in offset ;Exchanqe SI and DI ;Flicker suppressed? ; NO --> SUPO ;YES -->Wait for retrace ;Disable screen ;Store segment reqister ; On the stack ;Segment address of the video RAM ;To DS ;And ES ;Record DI in AX ; Record SI in BX ;Number of columns in counter ;Move a line ;Restore DI from AX ;Restore SI from BX ; Set next 11ne ;processed all lines ? ;NO --> move another line ;Get segment reqister from ; Stack ;Flickerinq suppressed? ;NO --> SUP2 ;YES --> Enable screen ;Get lower riqht corner back ;Return number of lines ;Return upper left corner ; Lower line to BL ;Subtract number of lines

mav ah,07h call clear pop si pop di pop bx pop ax ret scrollup endp ;-- SCROLLDN: scrolls a window N lines down --------------------------;Color : black on white ; Clear lines ;CX and DX have already been **jRestored**  ;Back to caller  $;--$  Input : BL = line upper left<br> $;--$  BH = column upper leg ;-- BH = column upper left<br>;-- DL = line below right  $; - DL = line$  below right<br> $; - DH = column$  below right  $; --$  DH = column below right<br> $; --$  CL = number of lines to  $;--$  CL = number of lines to be scrolled<br> $;--$  : BP = number of the screen page (0 to : BP = number of the screen page (0 to 3) ;-- Output **none**   $;--$  register : only FLAGS are changed<br> $;--$  Info : the display lines libe : the display lines liberated are cleared scrolldn proc near cld push ax push bx push di push si push bx push ex push dx sub dh,bh inc dh mov al, bl mov bl,dl call calo mov si,di sub bl,cl call calo xchg si,di sub dl,al inc dl sub dl,cl crnp wait,O je sdnO waitret setmode 00100l0lb sdn0: push ds<br>push es mov ax, VIO SEG mov **ds,ax**  mov **es,ax**  sdnl: mov ax,di mov bx, si mav cl,dh **rep movsw**  mov di,ax mov si,bx sub di,160 sub si,160 dec dl : On string commands count up ;Record all changed registers ; On the stack ;In this case the sequence ;Must be observed ;These three registers are returned ;From the stack before the end ;Of the routine ;Calculate the number of columns ;Record line upper left in AL ;Line below right to line below left ;Convert upper left in offset ;Record address in 51 ;Subtract number of characters to scroll ; Convert upper left in offset ;Exchange 51 and DI ;Calculate number of lines ; Subtract number of lines to be scrolled ;Flicker suppressed? ;NO --> SDNO ;YES --> Wait for retrace **iDisable screen**  ;Store segment register on the **;Stack**  ;Segment address of the video RAM ;To DS ; and ES ;Record DI in AX ;Record 51 in BX ;Number of columns in counter ;Move a line ;Restore Dr from AX ; Restore SI from BX ;set into next line ;processed all lines

```
jne sdn1 ;NO --> move another line
             pop es ;Return segment register from<br>pop ds ;Stack
                                           ; Stack
             cmp wait,0 ;Flicker suppressed?<br>ie sdn2 :NO --> SDN2
                                           ;NO --> SDN2
             setmode 00101101b ; YES --> Enable screen
sdn2: pop dx ;Get lower right corner<br>pop cx ;Return number of lines<br>pop bx ;Return upper left corner
             pop bx ; Return upper left corner<br>mov dl,bl ; upper line to DL
             mov dl,bl ;upper line to DL<br>add dl,cl ;Add number of lin
                                           ;Add number of lines
             dec dl<br>mov ah, 07h
             mov ah, 07h ;Color : black on white<br>call clear ;Erase liberated lines
                                           ; Erase liberated lines
             pop si ;CX and DX have already been<br>pop di :Returned
                                           ; Returned
             pop bx 
             pop ax 
             ret ;Back to caller
scrolldn endp
;-- CLS: Clear the screen completely -------
 \zeta = \zeta - \zeta . The street of the screen page (0 or 1)<br>\zeta = -\zeta - \zeta output : none
;-- register : only FLAGS are changed 
cls 	 proc near 
             mov ah,07h ;Color is white on black<br>xor bx,bx ;upper left is (0/0)
             xor bx,bx ;upper left is (0/0)<br>mov dx, 4F18h ;Lower right is (79/;Lower right is (79/24)
             ;-- Execute Clear ------------------------------------------
cls endp
;-- CLEAR: fills a designated display area with space characters -----
;-- Input : AH = attribute/color<br>;-- BL = line upper left
;-- BL = line upper left<br>;-- BH = column upper le
;-- BH = column upper left<br>;-- DL = line below right
;-- DL = line below right<br>;-- DH = column below right
;-- DH = column below right<br>;-- BP = number of the scre
                   BP = number of the screen page (0 to 3):- Output : none
:= register : only FLAGS are changed
clear 	 proc near 
            cld \begin{array}{ccc} \text{cld} & \text{...} & \text{...} \\ \text{push cx} & \text{...} & \text{...} \\ \text{else} & \text{...} & \text{...} \\ \end{array}push cx \qquad \qquad ; Store all register which are push dx \qquad \qquad ; Changed on the stack
                                           ; Changed on the stack
            push si 
             push di 
            push es<br>sub dl,bl
                                          ;Calculate number of lines
             inc dl 
                                           ; Calculate number of columns
            inc dh 
            call calo \frac{1}{10}; Offset address of the upper left corner<br>mov cx, VIO SEG ; Segment address of the video RAM
                                           ; Segment address of the video RAM
            mov es, cx ;To ES<br>xor ch, ch ;Hi by
                                           ;Hi bytes of the counter to 0
```
mov al.<sup>\*</sup> \* **;Space character** cmp wait,0 je ciearl ;Flickering suppressed? ;NO --> CLEAR! push dx waitret setmode OOIOOIOlb pop dx ;Store DX on the stack ;Retrace wait ;Switch screen off ;Return DX from the stack clearl: mov si,di mov cl,dh rep stosw mov di,si add di,160 dec dl jne ciearl ;Record DI in SI ;Number columns in counter ;Store space character ;Return 01 from SI ;Set in next line ;AII lines processed? ;NO --> erase another line c::mp wait,O je clear2 ;Flicker suppressed? ;NO --> CLEAR2 setmode 00101101b ;Enable screen clear2: pop di pop si pop dx pop ex ret pop es ;Get registers from ; Stack again ; Back to caller clear endp ;-- PRINT: outputs a string on the screen -- $;--$  Input : AH = attribute/color<br> $;--$  DI = offset address of  $; - DI = \text{offset}$  address of the first character<br> $; - SI = \text{offset}$  address of the strings to DS ;-- SI = offset address of the strings to DS<br>;-- BP = number of the screen page (0 to 3)  $BP$  = number of the screen page (0 to 3) ;-- Output : DI points behind the last character output  $;--$  register : AL, DI and FLAGS are changed<br> $;--$  Info : the string must be terminated : the string must be terminated by a NUL-character. ;-- other control characters are not recognized print proc near cld  $\begin{array}{ccc} 1 & \text{otherwise} \\ \text{cyl} & \text{otherwise} \end{array}$  ; Store SI, DX and ES on the ; Store SI, DX and ES on the stack push es push ex push dx<br>mov dx, VIO\_SEG mov dx,VIO\_SEG ; Segment address of the video RAM<br>mov cl,wait ; Get WAIT flag mov cl, wait ; Get WAIT flag<br>mov es, dx ; First to DX at ;First to DX and then to ES jmp short print3 ;Get character and display it printl label near or cl,cl ;Flicker suppressed? je print2 ; NO --> PRINT2 push ax ;Record characters and color<br>mov dx,3DAh ;Address of the display-state mov dx,3DAh ;Address of the display-status-register<br>in al,dx ;Get content hrl: in al,dx <br>test al,1 ;Horizontal ; test al,1 ;Horizontal retrace?<br>ine hri :NO --> wait jne hri ;NO --> wait cli ;permit no further interrupts hr2: in al,dx ; Get content<br>test al,1 ;Horizontal : test al,1 ;Horizontal retrace? je hr2 ;YES --> wait<br>pop ax ;Restore char ; Restore characters and color

sti ;Do not suppress Interrupts any more print2: stosw ;Store attribute and color in V-RAM<br>print3: lodsb ;Get next character from the string lodsb ;Get next character from the string<br>or al,al ;Is it NUL or al, al  $\begin{array}{ccc} ;1s & \text{it NUL} \\ \text{ine print1} & ;N0 & \text{---} > \text{out} \end{array}$ ;NO --> output printe: pop dx ;Get SI, DX, CX and ES from stack pop cx pop es pop si<br>ret ; Back to caller print endp ;-- CALO: Converts line and column into offset address --------------- ;--<br>i-- BH = column **BL** - number of the screen page (0 to 3)  $:-$  Output : DI = the offset address ;-- register : DI and FLAGS are changed calo proc near push ax ; Secure AX on the stack<br>push bx : Secure BX on the stack ; Secure BX on the stack shl bx,1 ;Column and line times 2<br>mov al,bh ;Column to AL mov al, bh ;Column to AL<br>xor bh, bh ;Hi byte mov di, [lines+bx] ;Get offset address of the line<br>xor ah,ah ;HI byte for column offset xor ah,ah ;HI byte for column offset<br>add di,ax ;Add line and column offset add di, ax ;Add line and column offset<br>mov bx, bp ;Screen page to BX mov bx, bp ; Screen page to BX<br>mov cl, 4 ; Multiply by 4,096 ;Multiply by 4,096 ror bx, cl<br>add di, bx add di,bx ;Add beginning of screen page to offset<br>pop bx ;Restore BX from stack pop bx ;Restore BX from stack<br>pop ax ;Restore AX from stack pop ax ; Restore AX from stack<br>ret ; Back to caller ; Back to caller calo endp ;-- CGR: Erase the complete Graphic display -----<br>;-- Input : AL = OOH : erase all pixels<br>;-- FFH : set all pixels FFH : set all pixels ;-- Output **none**  ;-- register : AH, BX, CX, DI and FLAGS are changed ;-- Info : this Function erases the Graphic display in both<br>;-- Graphic modes Graphic modes cgr proc near push es ;Store ES on the stack cbw ; Expand AL to AH<br>xor di,di ;Offset address i xor di,di ;Offset address in video RAM<br>mov bx,VIO SEG ;Segment address screen page mov bx, VIO\_SEG ; Segment address screen page<br>mov es, bx ; Segment address into segment mov es,bx <sup>-</sup> ;Segment address into segment register<br>mov cx,2000h :One page is 8KB words ;One page is 8KB words<br>;Fill page rep stosw<br>pop es pop es ;<br>Return ES from stack<br>Return ES from stack<br>Return ES from stack ; Back to caller cgr endp ;-- PIXLO: sets a pixel in the 320\*200 pixel graphic mode  $;--$  Input  $:BP$  = number of the screen page (0 or 1)  $; -$  BX = column (0 to 319)<br> $; -$  DX = line (0 to 199)  $;--$  DX = line (0 to 199)<br> $;--$  AL = color of the pix ;--  $AL = color of the pixels (0 to 3)$ 

```
:-- Output : none
;-- register : AX, DI and FLAGS are chanqed 
pixlo proc near 
             push ax ; Secure AX on the stack<br>push bx ; Note BX on the stack
             push bx ;Note BX on the stack<br>push cx ;Store CX on the stack
                                             ; Store CX on the stack
             mov cl, 7<br>mov ah, bl
             mov ah,bl ;Transmit column to AH 
             and ah, 11b ; Column mod 4<br>shl ah, 1 ; Column * 2
             \begin{array}{ll}\n\text{shl} & \text{ah,1} \\
\text{sub} & \text{cl,ah} \\
\text{sub} & \text{cl,ah}\n\end{array}sub cl,ah ;7 - 2 • (column mod 4) 
mov ah,ll ;Bit value 
             mov ah, 11 <br>shl ax, cl <br>not ah ;Nove to pixel position<br>rot ah ;Reverse AH
             not ah iReverse AH<br>shr bx,1 iDivide BX
             shr bx,1 ;Divide BX by 4 by shifting<br>shr bx,1 ;Right twice
                                       ; Right twice<br>; Set pixel
             jmp short spix
pixlo endp 
;-- PIXHI: sets a pixel in the 640*200 pixel qraphic mode 

;-- Input : BP = number of the screen page (0 or 1)i-- BX = column (0 to 639)<br>
i-- DX = line (0 to 199)
; -- DX = line (0 to 199)<br>; -- AL = color of the pix

i-- AL - color of the pixels (0 or 1) 
;-- Output : none
 ;-- register : AX, DI and FLAGS are changed
pixhi proc near 
             push ax ;Store AX on the stack<br>push bx ;Note BX on the stack
             push bx induce i
                                             ;Note CX on the stack
             mov cl, 7<br>mov ah, bl
             mov ah,bl ;Transmit column to AH 
              and ah, 111b ; Column mod 8<br>sub cl, ah ; 7 - column mod 8
             sub cl, ah <br>mov ah, 1 ;Bit value<br>shl ax, cl ;Move pixe
              shl ax,cl ;Move pixel position<br>not ah ;Reverse AH
             not ah ;Reverse AH 
             mov cl, 3 ;3 shifts<br>shr bx, cl                        ;Divide B
                                             ;Divide BX by 8
              ; -- set pixel ----pixhi endp 
;-- SPIX: sets a pixel in the graphic display ----------------------- ;-- Input BX = column offset 
;-- DX = line (0 to 199)<br>;-- AH = Value to cancel
;-- AH = Value to cancel old Bits 
                   AL = new Bit valueOutput none 
i-- register : AX, DI and FLAGS are changed
spix proc near 
              push es ;Secure ES on the stack 
              push dx \begin{array}{ccc} \bullet \end{array} ; Secure DX on the stack<br>push ax \begin{array}{ccc} \bullet \end{array} ; Secure AX on the stack
                                             ; Secure AX on the stack
              xor di,di ;Offset address in video RAM<br>mov cx,VIO_SEG ;Segment address screen page
              mov cx, VIO_SEG ; Segment address screen page<br>mov es, cx ; Segment address into segment
              mov es, cx <sup>-</sup>;Segment address into segment register<br>mov ax, dx -;Move line to AX
              mov ax,dx ;Move line to AX<br>shr ax,1 ;Divide line by:
              shr ax,1<br>mov cl,80 ;The factor is 90<br>mul cl :Multiply line by
                                             ;Multiply line by 80
```


# **10.5 EGA and VGA Cards**

The EGA and VGA cards far exceed their predecessors in both graphics and in text display capabilities. Other computers have had EGA and VGA capabilities for some time (e.g., work stations, CAD/CAM applications), but these video cards are now at prices where many home systems will soon have them.

The range of power of this new generation of video cards can be seen in their very sharp resolutions and their ability to display almost any number of lines on the screen. The EGA and VGA cards' greatest feature lies in their ability to emulate other video cards.

These capabilities come with a price-more complicated hardware and programming are required. One result of this is that the features of an EGA card or a VGA card can no longer be realized with the traditional PC video controller (the Motorola 6845). Instead, most EGA and VGA cards contain a VLSI chip developed especially for use on an EGA card. At the heart of this component is a video controller that controls the video signal generation. Its basic task is similar to that of the 6845, but its registers differ from those of the 6845, both in number and interaction between registers. Comparing the 6845 and VSLI is like comparing BASIC and assembly language, where the increase of power is in proportion to the degree of language complexity.

We recommend that you avoid programming the hardware registers directly unless you absolutely must do so. Many tasks can be delegated to the BIOS without wasting much time. Not only will this keep your program code more compact and easier to read, it will greatly improve the compaubility of your code with other video cards. Among the tasks which the various functions of the BIOS video interrupt can perform are:

- Initialization of the video mode
- Selection of the display page
- Cursor positioning
- Defining the starting and ending line of the cursor
- Palette and border color selection
- Setting the size of the character matrix, and thereby the number of text lines which can be displayed on the screen
- Loading user-defined character sets
- Reading configuration data

Detailed information about traditional BIOS video functions and the new functions of the EGA/VGA BIOS can be found in Sections 7.4.

If you need speed and maximum control over the screen, you should still perform time-critical actions (e.g., manipulating video RAM) "by hand."

# EGAlVGA and text mode

There is no difference between the EGA and MDA or CGA card in text mode. The video RAM and attribute byte are organized the same way for the EGA card as for the other two cards-even the location of the video RAM is the same. But since an EGA card can emulate either a CGA card or an MDA card, depending on the monitor to which it is connected, you should first determine what kind monitor is in use. From this the EGA can determine which of the two systems to emulate (routines presented in Section 10.7 show how this is done). The type of card being emulated determines where the video RAM can be found in memory, how the bits of the character attribute byte are interpreted, and how many screen pages are available.

Remember that the EGA or VGA card does not contain a 6845 CRTC, despite the fact that it can perfectly emulate its video predecessors. This means that the status and control registers of the MDA and CGA cards are unavailable. However, since the settings that are normally made with these registers can also be performed with the BIOS, we don't really need these registers. You should also remember that there are no restrictions to accessing the video RAM of an EGA card or a VGA card when it is in CGA emulation. It is unnecessary to synchronize screen access with the activity of the CRTC by reading the status register.

The parallels between the organization of the video RAM in the CGA and MDA cards also apply when the text mode is switched to 43 lines (which is impossible in CGA emulation). As with any other number of displayed lines, this does not change the basic structure of the video RAM at all. It is larger, but the formulas for calculating the offset position of a character and its attribute byte within the video RAM are still valid.

The VGA card is capable of 25, 43 and even 50 lines in text mode, depending on the monitor in use.

These parallels also apply to the graphics modes already available to the CGA card. The position of the video RAM and its structure are identical to the those of the CGA card.

#### EGA/VGA and graphic modes

The EGA card offers the following new graphics modes:

- 320x200 pixels, 16 colors (BIOS code: ODH)
- 640x200 pixels, 16 colors (BIOS code: OEH)
- 64Ox350 pixels. 2 colors (BIOS code: OFH)

• 640x350 pixels, 16 cobs (BIOS code: 10H)

The VGA card offers the following graphic modes:

- 640x480 pixels, 2 colors (BIOS code: IlH)
- 64Ox480 pixels, 16 colors (BIOS code: 12H)
- 320x200 pixels, 256 colors (BIOS code: 13H)

Some EGA cards have even more modes with higher resolution or more colors, but these modes are not part of the EGA standard and are supported by only a few programs.

It is somewhat difficult to talk about a "standard", because almost every manufacturer has their own modes. Let's look at the lowest common denominator-the modes which practically all EGA/VGA cards support. These are the modes supported by the original EGA card, the IBM EGA.

These video modes, in which the video RAM can occupy more than lOOK, show a structure quite different from those used by the MDA, CGA and Hercules cards. The maximum of 256K of RAM is divided into four *bit planes* which are arranged in a kind of a three-dimensional organization. From the processor's point of view these bitplanes reside between segment addresses AOOOH and BOOOH.

Each bitplane contains one bit for each individual pixel. If you place the bitplanes on top of each other, each pixel is represented by a total of four bits, which together make up the color value of the pixel. Bitplane zero contains bit zero of the color value of each pixel, bitplane one contains bit one, and so on. This limits the number of displayable colors to 16, since four bits (or bitplanes) can represent  $2<sup>4</sup>$ , or 16 different numbers.

The color value obtained from combining individual bitplanes does not correspond directly to a color. It is actually used as an index into one of the 16 palette registers of the EGA card, each of which designates a particular color. Since the EGA card can display a total of 64 different colors, the palette registers allow you to select 16 of these colors to be displayed on the screen simultaneously. The individual palette registers can be loaded with the help of the extended EGA BIOS functions, as described in Section 7.4.

The structure of each bitplane corresponds to the organization of the pixels on the screen, and parallels that of video RAM in text mode. Since each pixel occupies one bit in the bitplane, eight consecutive pixels are combined into a byte. The pixels on each line are placed left to right in successive memory locations. The length of each line can be determined using the fonnula:

```
horizontal resolution / 8
```
Since the individual screen lines follow each other in sequence starting from the top of the screen, the starting address of each line is obtained by multiplying the line number by this value. The byte within this line which contains the desired pixel is calculated by dividing the column number by eight (bits per byte). Adding this to the starting address of the line gives us the following formula, which calculates the offset address of the byte containing the coordinates  $(X, Y)$ :



 $Y *$  (horizontal resolution / 8) + X / 8

*Bitplane arrangement on EGA card* 

The bit number at which the pixel is located in this byte results from the remainder of the division of the column number by eight:

7 - (column\_number MOD 8)

These two formulas can be used to localize a pixel within a bitplane and implement graphics primitives.

However, the bitplanes cannot be accessed individually because they all lie at the identical segment address. The EGA card has four latch registers, each of which contains a complete byte from one of the four bitplanes. When the CPU performs a read access from the EGA video RAM at segment address AOOOH, one byte is frrst read from each of the four bitplanes at the specified offset address and loaded into the four latch registers. This applies to instructions which access memory directly, such as MOY or LODS, as well as all insttuctions in which a byte from the video RAM appears as an operand. This can be the case with arithmetic insttuctions (ADD, SUB, OR, AND, etc.) and comparison instructions (CMP, CMPS).

The process is similar for writing bytes to the video RAM. In this situation the contents of the four latch registers are written back to the four bitpJanes.



*Video RAM access-loading the foUT latch registers* 



*Video RAM access-writing the foUT latch registers* 

Since the latch registers are not directly accessible to the processor, we must alternate conversion between eight and 32 bits when reading and writing the video RAM. When reading, 32 bits from the latch registers must be compressed into one byte, while the eight bits from the CPU when writing must be divided among the 32 bits of the latch registers. The nine graphic controller registers in the EGA card perform this conversion.



Access to these registers is similar to CRTC register access on the Hercules graphics card. Here too there is an address register at port address 3DEH, into which we must first load the number of the register in the graphics controller that we want to access. The value for this register can then be written to the data register located at address 3CFH, immediately after the address register. These ports do not have to be accessed separately: A 16-bit OUT instruction to the address register performs the access in one move. The AX register, which will be sent to this port, must contain the register number in the low-order byte (AL), and the value for this register in the high-order byte (AH). Although values can be loaded into the graphics controller registers in this manner, it is not possible to read data from the EGA card.

The contents of register number five, the mode register, are responsible for the behavior of the video RAM. This register controls the current read and write modes and thereby the manner in which the data from the latch registers is combined with the other registers in the graphics controller and the CPU data.



*Mode register structure* in *EGA card graphics controller* 

There are a total of two different read modes and three write modes.

### Read mode 0

Read mode 0 is the simpler of the two read modes. As usual, a read access in this mode first loads the specified byte from the four bitplanes into the four latch registers. Then the contents of the latch register specified by the lower two bits of the read map select register (register four) are tramferred to the CPU.



Video RAM read access *in* read *mode* 0

The following sequence of assembly language instructions first sets read mode 0, then writes the value 2 into the Read Map Select register, and fmally reads a byte from offset address 0003H in the video RAM. As a result, the AL register contains the bit values for the pixels with coordinates (24, 0) to (31, 0) from bitplane 2.

```
mov dx,3CEh ;port address of the graphics cont. addr. reg. mov ax,0005h ;write read mode 0 in the mode register
out dx, ax<br>mov ax, 0204h
mov ax,0204h ;write the value 2 (plane number) in the out dx, ax ;read map select register<br>mov ax,0A000h ;seqment address of the video RAM
                                 ; segment address of the video RAM
mov ds,ax ;to DS<br>mov si,0003h ;offset
mov si,0003h ;offset address into the video RAM<br>lodsb : read byte from plane 2
                                  ; read byte from plane 2
```
# Read mode 1

Read mode 1 specifies which of the eight pixels in the specified byte of video RAM is set to a certain color. This is determined by the individual bits in the read byte which correspond to the one of the eight pixels from the specified byte in the video RAM. If a pixel has the specified color (appropriate bit map), then the corresponding bit will be I, else O. The bit pattern of the color to be compared must be loaded into the lower four bits of the Color Compare register. The lower four bits of the Color Don't Care register show which bitplanes will be taken into consideration in the comparison. The value 1 includes the given plane in the comparison, while the value 0 excludes it.



*Video RAM read access in read* mode *1* 

The following program sequence determines which of the pixels between coordinates (0, 0) and (7. 0) have color value five. First. read mode 1 is set by the Mode register. Then the color value to be tested (five) is loaded into the Color Compare register. We must also load the Color Don't Care register with the value Illlb so that all four bitplanes will be included in the comparison. However. this is the default value and we have not loaded any other value into this register, so we can skip this step. After programming the registers of the graphics controller, we load the segment and offset addresses of the pixels to be compared into the OS and SI registers. Then the read is executed from the video RAM.

```
mov dx, 3CEh ; port address of the graphics cont. addr. reg.<br>mov ax, 0805h ; write read mode 1 into the mode register
mov ax,0805h ; write read mode 1 into the mode register<br>out dx,ax
mov ax,0502h ; write color value 15 into the out dx,ax ; Color Compare register
mov ax, 0A000h ; segment address of the video RAM<br>mov ds,ax ; to DS
mov ds, ax<br>xor si, si
xor si,si ;load offset address 0<br>lodsb :read and compare pixe
                              ; read and compare pixels,
                              ;return result in AL
```
### **Write mode 0**

Writing to the video RAM in write mode 0 results in a number of operations, all of which depend on the contents of several registers. The contents of the Bit Mask register determine whether the value of a bit in the four latch registers will be written unchanged to the found bitplanes or whether it will first be modified. The individual bits in the Bit Mask register correspond to the individual bits in the four latch registers. If a bit in the Bit Mask register is 0, the corresponding bits in the latch registers will be written to the bitplanes unchanged. If this bit is I, a modification will take place, dependent on the contents of the Function Select register. As the following figure shows, the bits can be replaced or modified with the logical operations AND, OR, and XOR.



*Function Select Register structure in EGA card graphics controller* 

The contents of the Enable Set/Reset register determines from where the other operand in these operations will come. Ifthe lower four bits contain the value I, the other operand will come from the lower four bits of the Set/Reset register. Each of these bits is then combined with the bits from the latch registers as described by the contents of the Function Select register. All of the bits to be modified from latch register 0 will then be operated on with bit 0 of the Set/Reset register. In the same manner, all of the bits to be modified from latch registers I, 2, and 3 are combined with bits 1,2, and 3 of the Set/Reset register, respectively. The byte which is actually written to the graphics controller becomes irrelevant at this point-the write access is reduced to a trigger, which cannot have any direct influence on the contents of the latch register (and therefore the bitplanes).



*contains a value o/OOOOllll(b)* 

The following assembly language fragment assigns the pixels at coordinates (5, 0) and  $(7, 0)$ , found at offset address  $0000H$  in the video RAM, the color 1011 $(b)$ .

Since we don't want to change the color of the other pixels, the contents of the byte are first read into the latch register with a read access to the video RAM. It is not important which read mode is active because the byte transmitted to the CPU is irrelevant; all we are interested in is loading the latch register. Since only bits 0 (coordinates  $(7, 0)$ ) and 2 (coordinates  $(5, 0)$ ) will be changed, we load the value 00000101b (05h) into the bitmask register. In the Function Select register we write the value 0 because we want to replace bits 0 and 2 with a new bit combination. We write the color we want to give to the two bits  $(1011b = 0Bh)$  in the Set/Reset register. We must also write the value I 111(b) (OFH) to the Enable Set/Reset register of the graphics controller so that the color value will be taken from the Set/Reset register. We can then execute the write access to video RAM.



Things are different when the Enable Set/Reset register contains the value zero. In this case all of the bits to be modified from the four latch registers are combined with the CPU byte latch by latch. Here again the type of operation performed
depends on the contents of the Function Select register. For example, if the OR operation is selected and bits 1,2,4, and 6 are to be modified, than these bits of all four latch registers will be individually ORed with bits 1,2,4, and 6 in the CPU byte.



## **Write mode 1**

Write mode 1 is quite simple compared to the complex operations of write mode O. The contents of the registers and the CPU byte are irrelevant because the contents of the four latch registers are loaded unchanged into the specified offset address within the four bitplanes. This is useful for copying the color values of eight successive pixels to eight other pixels, for instance. The byte containing the eight pixels can be read under one of the read modes, placing it in the latch registers. Then a write access can be made to the byte in video RAM to which you want to copy the color values. The graphics controller will automatically copy the contents of the latch registers to the specified position within the four bitplanes.

To write these color values to other locations, you can use additional write accesses. No more read accesses are necessary, since the latch registers already contain the appropriate values and their contents are not changed by the write access.

#### **Write mode 2**

Write mode 2 resembles a combination of the various modes of write mode O. As in write mode 0, the bitmask register detennines which bits will be taken directly from the latch registers and which will be modified. The manner in which these bits are manipulated is again determined by the mode selected in the Function Select register. The lower four bits of the CPU byte will be combined with the latch registers, independent of the Enable Set/Reset register. Bit zero of the CPU byte is combined with all bits in latch register zero which are to be modified. The same applies for CPU bits 1, 2, and 3, which are combined with the bits of latch registers 1, 2, and 3, respectively.



Write access to video RAM in write mode 2

This mode is good for setting the colors of individual pixels, as we demonstrated in the example in write mode 0. In contrast to write mode 0, the assemblylanguage fragment is somewhat shorter because neither the Enable Set/Reset nor the Set/Reset register has to be programmed. Here is the same example using write mode 2:



#### Demonstration program

The following program demonstrates the following basic graphics routines:

- Calculating the position of a pixel within the video RAM
- Setting the color of a pixel
- Reading the color of a pixel
- Filling the entire video RAM with a color

If you have followed this section closely, especially the material on the read and write modes, you won't have any problems following the logic of the various functions. Since it contains detailed documentation, we won't say anything more about it.

It should be noted that the program is intended for demonstration purposes only. You can develop it further if you want to make a graphics library out of these functions. For example, the function PIXPTR loads the segment address of the video RAM into the ES register for calculating the position of a pixel within the video RAM each time it is called. This can be eliminated by loading this address into the register once at the beginning of the program and leaving it there, as long as the other functions do not change this register.

The graphics controller register programming can also be improved. Here the various registers are reloaded with the ROM-BIOS default values after the function has completed. This can be eliminated as long as you do not use the BIOS functions for character output (in the graphics mode) or the functions for setting and testing points within the module or program. If you avoid these calls, then these registers can be reset to their default values once at the end of the program instead of at the end of each routine.

```
Assembler listing: VEGA.ASM
```

```
\mathcal{F}^{\star}7*-
                                                                           .....
                   , \starTask : Creates elementary functions for accessing the *;<br>graphic modes on an EGA/VGA card *;
\frac{1}{2};*-…∗.
** Author : MICHAEL TISCHER<br>** Developed on : 10/3/1988
                                                                             \star ;
                                                                             \star ;
; *Last update : 6/19/1989
                                                                             \star ;
                                                                            ..*;
; * -\mathbf{r}^{\star}Assembly : MASM VEGA;<br>LINK VEGA:
                                                                             ٠,
; *٠,
                       LINK VEGA;
; *---∗;
\mathbf{r}^{\star}Call : VEGA
                                                                             \star :
; == Constants ============
                              ;Segment address of video RAM<br>
;in graphic mode<br>
;Every graphi line in EGA/VGA graphic<br>
;modes require 80 bytes<br>
;Bitmask register<br>
;Mode register<br>
;Function select register<br>
;Function select register<br>
;Enable Set/Reset re
VIO\_SEG = 0A000hLINE LEN
             = 80BITMASK REG = 8
MODE REG = 5FUNCSEL REG = 3MAPSEL \overline{REG} = 4ENABLE<sup>-</sup> REG = 1SETRES<sup>-</sup>REG = 0GRAPH\ CONT = 3CEh
OP MODE
            = 0, 00h = \text{Replace}\ddot{\phantom{0}}08h = AND comparison\frac{1}{2} 10h = OR comparison
                                    ; 18h = EXCLUSIVE OR comparison
GR 640 350 = 10h
                        ;BIOS code for 640x350-pixel
```
i16-color graphic mode  $TX 80 25 = 03h$  ; BIOS code for  $80*25$ -char. itext mode ; == Stack ================ stack segment para stack ;Definition of stack segment dw 256 dup (?) ; 256-word stack stack ends ;End of stack segment **; == Data ==--========-=....=-=---=---==-----===-----=-===**  data segment para 'DATA' ;Definition of data segment ;-- Data for the demo program -=====-~====-=-----------=----=--==--- initm db 13,10 db "VEGA (c) 1988 by Michael Tischer" db 13,10,13,10 db "This demonstration program operates only with an EGA/",13,10 db "card and a hi-res monitor. If your PC doesn't have this",13,10 db "configuration, please press the <s> key to abort the",13,10 db "program.",13,10 db "Press any other key to start the program.",13,10,"S" data ends ;End of data segment ;~= **Code ======-=====--======-======-----------------=======-=-=----===** code segment para 'CODE' ;Definition of code segment assume cs:code, ds:data, es:data, ss:stack *i==* **Demo program** ==========~-=======-=------==-==----==-=====-=--===-- demo proc far mov **ax, data** *iGet* segment addr. from data segment mov **ds,ax iand** load into DS mov ds, ax iand load<br>
mov es, ax iand ES ;-- Display opening message and wait for input -------------mov ah, 9 ; Function number for string display mov dx, offset initm ;Message address<br>int 21h :Call DOS interr ;Call DOS interrupt xor ah,ah ;Get function number for key<br>
int 16h ;Call BIOS keyboard interrupt<br>
cmp al,"s" ;Was <s> entered? je ende ;YES --> End program<br>
cmp al, "S" ;Was <S> entered? cmp **al,<sup>n</sup>S"** ;Was <S> entered?<br>jne startdemo ;NO --> Start demo ;NO --> Start demo ende: mov ax,4COOh ;Function no. for end program<br>int 21h :Call DOS interrupt 21H ;Call DOS interrupt 21H  $:$  -- Initialize graphic mode -------startdemo label near mov ax, GR\_640\_350 ;Initialize 64x350-pixel<br>int 10h :16-color graphic mode ;16-color graphic mode



shr bx,l add bx, ax add **bx,ax** ;Add line offset mov ax, VIO\_SEG ; Load segment address of video RAM<br>mov es, ax ; into ES mov es, ax and cl,7 ;And bits 4 - 7 of graphic column<br>xor cl,7 ;Turn bits 0 - 3 then ;Turn bits 0 - 3 then<br>;subtract 7 - CL mov ah,1 ;After shift, bit 0 should be ;left alone pop dx  $\begin{array}{ccc} 1 & 0 & 0 \\ 0 & 0 & 0 \end{array}$  ; Pop DX off of stack ret ; Back to caller pixptr endp *i*-- SETPIX: Sets a graphic pixel in the new EGA/VGA graphic modes ------<br> *i*-- Input AX = graphic line *i-*<br> *i-* BX = graphic column <br>  $i$ -- Output none **i-** pixel color ;-- Output none ;-- Registers: ES, DX and CL are changed setpix proc near push ax ;Push coordinates onto push bx ; the stack call pixptr ; Computer pointer to the pixel mov dx, GRAPH CONT ;Load port addr. of graphic controller ;-- Set bit position in bitmask register ------------------- shl ah,cl ;Mask for bit to be changed mov al, BITMASK REG ; Move bitmask register from AL out dx, ax  $\cdot$  ; Write to register  $:--$  Set read mode 0 and write mode 2 -- ------mov ax, MODE\_REG + (2 shl 8) ; Reg. no. and , mode value<br>out dx.ax : Write in the register ;Write in the register ;-- Define comparison mode between preceding latch ----------  $;--$  contents, and CPU byte mov ax, FUNCSEL REG + (OP MODE shl 8) ; Write register number<br>out dx, ax : and comparison operator ; and comparison operator ;-- Pixel control mov al, es: [bx] ; Load latches<br>mov es: [bx], ch ; Move color i ; Move color into bitplanes ;-- Set altered registers to their default (BIOS) ;-- status mov ax,BITMASK\_REG + (OFFh shl 8) ;Set old bitmask out dx,ax ;Write in the register<br>mov ax,MODE\_REG ;Write old value for for mode register<br>out dx.ax out dx,ax  $\overline{\phantom{a}}$  ;into register<br>mov ah,FUNCSEL\_REG ;Write old value for function select<br>out dx,ax ;register into register

pop bx ;Pop coordinates off of stack pop ax ret in the set of the s setpix endp ;-- GETPIX: Places a pixel's color in one of the new EGA/VGA -----------<br>;-- graphic modes<br>;-- Input : AX = graphic line  $;--$  BX = graphic column<br> $;--$  Output : CH = graphic pixel color ;-- Registers: ES, DX , CX and DI are changed getpix proc **near**  push ax ;Push coordinates onto<br>
push bx ;the stack ; the stack call pixptr  $\begin{array}{ccc} \text{c} & \text{c} \\ \text{c} & \text{c} \\ \text{c} & \text{c} \\ \text{c} & \text{d} \end{array}$  : Move bitmask to CH mov ch, ah ;Move bitmask to CH<br>shl ch, cl ;Shift bitmask by b ;Shift bitmask by bit positions mov di,bx ;Move video RAM offset to DI<br>xor bl,bl ;Color value will be compute ; Color value will be computed in BL mov dx, GRAPH CONT ; Load graphic controller port address mov ax,MAPSEL\_REG + (3 shl 8) ;Access bitplane f3 ;-- Go through each of the four bitplanes ------------------gpl: out dx,ax ;Activate bitplane #AH only<br>mov bh,es:[di] ;Get byte from the bitplane mov bh,es: [di] ;Get byte from the bitplane<br>and bh,ch ;Omit uninteresting bits and bh,ch  $\frac{1}{2}$ ; Omit uninteresting bits<br>neg bh neg bh  $\begin{array}{ll}\n ;\text{Bilt } 7 = 1, \text{ when a pixel is set} \\
 ;\text{Shift bit } 7 \text{ from BH to Bit 1 in}\n \end{array}$ ;Shift bit 7 from BH to Bit 1 in BL dec ah ;Oecrement bitplane number ;Not -1 yet? --> next bitplane **;--** The map select register must not be reset, since **;--** the EGA- and VGA-BIOS default to a value of 0 mov ch,bl ;Get color from CH<br>pop bx :Pop coordinates o pop bx ;Pop coordinates off pop ax ;of stack<br>ret : Back to ; Back to caller getpix endp ;-- FILLSCR: Sets all screen pixels to one color ------ ----;<br>;-- Input : AX = number of graphic lines on the screen<br>;-- CH = pixel color  $;--$  Output : none ;-- Registers: ES, AX, CX, 01, OX and BL are changed fillscr proc near mov dx,GRAPH\_CONT ;Load graphic controller port address<br>mov al,SETRES\_REG ;Numbmer of Set-/Reset registers<br>mov ah,ch  $\frac{1}{N}$ ;Move bit combination to AL<br>out dx,ax ;Write to the register mov ax, ENABLE\_REG + (OFh shl 8) ; Write OFH in the<br>out dx, ax : :Enable Set-/Reset registe: ; Enable Set-/Reset register mov bx, LINE LEN / 2 ; Length of a graphic line / 2 into BX<br>mul bx - ;Multiply by number of graphic lines<br>mov cx, ax - ;Move to CX as repeat counter **mov cx,ax** ;Move to CX as repeat counter xor di,di ;Address first byte in video RAM ;Segment address of video RAM

;Load into ES **mov es,ax**  ;Increment on string instructions cld rep stosw ; Fill video RAM ;-- Return old contents of Enable Set-/Reset register  $-----$ ;Load graphic controller port address ;Write OOH in Enable Set-/ mov dx, GRAPH\_CONT rnov ax, ENABLE\_REG ;Reset register out dX,ax ret ; Back to caller fillscr endp  $\bar{~}$ ; **End -=---....-------'""--------------------=--------** code ends ;End of code segment end demo ;Start program execution with DEMO

# **10.6 Determining the Type of Video Card**

Whenever you want to access video card hardware or use a BIOS function which is only available in special versions of the BIOS, you should first ensure that the card in question is actually installed in the system. If your program doesn't make such a test, then the result may not be what you wanted to appear on the screen.

It is especially important for an application program to recognize the type of video card installed, if your program is supposed to work the same on all types of cards while still directly accessing video hardware. The output routines need this information to make optimum use of the special properties of the given card

Remember that the PC can have both a monochrome video card (MOA, HOC or EGA with a monochrome monitor) and a color video card (EGA, VGA, or CGA) installed, although only one of the two cards may be active at one time.



We need to find out what video cards are installed. There are no BIOS or DOS functions for doing this, nor are there any variables we can read. We have to write an assembly language routine which checks the existence of different video cards. We can refer to the documentation for the various cards, since most manufacturers include some procedure for determining if their card is in use. It is important to keep the test specific (Le., it does not return a positive result if a certain type of video card is not installed). This presents problems for EGA and VGA cards, which can emulate CGA or MOA cards with the appropriate monitor, and are difficult to distinguish from true CGA or MOA cards.

All of the tests described here are found at the end of this section in the fonn of two assembly language programs intended for use with C and Pascal programs. The functions place the type of video card installed and the type of monitor connected to it into an array to which the function is passed a pointer. Iftwo video cards are installed, their order in the array indicates which one is active.

The following cards can be detected by the assembly language routine:

- MDAcards
- CGAcards
- HGC cards

#### EGA cards

VGAcards

Since the assembly language routine checks selectively for the existence of a certain video card, there is a separate subroutine for each type of video card. It bears the name of the video card for which it tests. These routines have names like TEST\_EGA, TEST\_ VGA, etc. The tests could be called sequentially, but certain tests can be excluded if we know they would return a negative result This is case for the CGA test, for example, if an EGA or VGA card has already been detected and is connected to a high-resolution color monitor. A CGA card cannot be installed alongside such a card, so there is no point in testing for it.

There is a flag for each test which determines whether or not the test will be performed. Before the ftrst test, the VGA test, all of the flags are set to 1 so that all of the tests will be performed in order. During the testing, certain flags can be set to 0 for reasons mentioned above, and the corresponding tests will not be made.

## VGA test

The tests begin with the VGA test. It is very easy because there is a special function in the VGA BIOS, sub-function OOH of function IAH, which returns precisely the information that the assembly language routine needs. The information is available only if a VGA card and hence a VGA BIOS is installed. This is the case if the value lAH is found in the AL register after the call. If the test routine encounters a different value there, the VGA test will be terminated and the other tests will be performed. This indicates that a VGA card is not installed.

After this function is called, the BL register contains a special device code for the active video card and the BH register contains a code for the inactive card. The following codes can occur:



These codes are separated into values for the video card and the monitor connected to it, and loaded into the array whose address is passed to the assembly language routine. Since this routine already has information about both video cards, the following tests do not have to be performed. The routine executes the monochrome test, however, if the functions discover a monochrome card, since it cannot distinguish between an MDA and HOC card.

### EGA test

After the VGA test comes the EGA test, which it performed only if the VGA test was unsuccessful, and thus the EGA flag was not cleared. It uses a function which is found only in the EGA BIOS: sub-function 10H of function 12H. If no EGA card is installed and this function is not available, the value lOH will still be found in the BL register after the function call. In this case the EGA test ends.

If an EGA card is installed, the CL register will contain the settings of the DIP switches on the EGA card after the call. These switches indicate what type of monitor is connected. They are converted to the monitor codes the assembly language routine uses and placed in the array along with the code for the EGA card. The CGA or monochrome test flag is cleared depending on the type of monitor connected. The EGA routine ends.

#### CGA test

If the CGA flag has not been cleared by the previous tests, the CGA test follows the EGA test. As with the monochrome test, there are no special BIOS functions which can be used and we have to check for the presence of the appropriate hardware. In both routines this is done by calling the routine TEST\_6845, which tests to see ifthe 6845 video controller found on these cards is at the specified port address. On a CGA card this is port address 3D4H, which is passed to the routine TEST\_6845.

The only way to test the existence of the CRTC at a given port address is to write some value (other than 0) to one of the CRTC registers and then read it back immediately. If the value read matches the value written, then the CRTC and thus the video card are present. But before writing a value into a CRTC register, we should stop to consider that these registers have a major impact on the construction of the video signals and careless access to them can not only thoroughly confuse the CRTC, it can even harm the monitor. Registers 0 to 9 are out of the question for this test, leaving us with registers 10 to 15, all of which have an effect on the screen contents. The best we can do is registers 10 and 11, which control the starting and ending lines of the cursor.

The assembly language routine first reads the contents of register 10 before it loads any value into this register. After a short pause so that the CRTC can react to the output, the contents of this register are read back. Before the value read is compared to the original value, the old value is fIrSt written back into the register so that the test disturbs the screen as little as possible. If the comparison is positive, then a CRTC is present and so is the video card (CGA in this case). The CGA routine responds by loading the code for a color monitor into the array, since this is the only type of monitor which can be used with a CGA card.

#### Monochrome test

The last test is the monochrome test, which also checks for the existence of a CRTC, this time at port address 3B4H. If it fmds a CRTC there, then a monochrome card is installed and we have to figure out if it is an MDA or HGC hard. The status registers of the two cards, at port address 3BAH, are used to determine this. While bit 7 of this register has no significance on the MDA card and its value is thus undefined, it contains a 1 on an HOC card whenever the electron beam is returning across the screen. Since this is not permanent and occurs only at intervals of about two milliseconds, the contents of this bit constantly alternates between 0 and 1.

#### Hercules

The test routine frrst reads the contents of this register and masks out bits 0 to 6. The resulting value is used in a maximum of 32768 loop passes, where the value is read again and compared with the original value. If the value changes. meaning that the state of bit 7 changes, then an HOC card is probably installed. If this bit does not change over the course of 32768 loop passes, then an MDA card is in use.

Here again we place the appropriate code for the video card in the array. The monitor code is also set to monochrome, since this is the only monitor which can be connected to an MDA or HGC card.

#### Primary and secondary video systems

The tests are now over. Now we have to figure out which card is active (primary) and which is inactive (secondary). If the outcome of the VGA test was positive, we can skip this because the VGA BIOS routine determines the active card automatically.

In other cases we can determine the active video card from the current video mode. which can be read with the help of function OFH of the BIOS video interrupt. If the value seven is returned, then the 80x25 text mode of the monochrome card is active. All of the other modes indicate that a CGA. EGA. or VGA card is active. This information is used to exchange the order of the two entries in the array if it does not match the actual situation.

The assembly language routine returns control to the calling program.

Here we include C and Pascal programs which call the function GetVIOS from the assembly language module. and demonstrate how GetVIOS works.

#### C listing: VIOSC.C

```
1***************************************************** *****************/ 
1* v I 0 S C *1 
1*--------------------------------------------------------------------*1 
1* Task : Determines the type of video card and monitor *1 
1* installed in the system. *I 
1*--------------------------------------------------------------------*1 
1* Author MICHAEL TISCHER *1 
1* Developed on : 10/02/1988 *1 
1* Last update : 06/20/1988 *1 
1*--------------------------------------------------------------------*1 
1* (MICROSOFT C) *I 
1* Creation CL lAS Ic VIOSC.C *1 
1* LINK VIOSC VIOSCA *1 
1* Call VIOSC *1 
1*--------------------------------------------------------------------*1 
1* (BORLAND TURBO C) *1 
1* Creation Create project file made of the following: *1 
1* VJOSC *1 
1* VIOSCA.OBJ *1 
1* Info Some cards may return errors or "unknown" *1 /****••••••••••••••••***•••***••••••••••****•••••••••••••••••••••••••**/ 
1*-- Declarations of external functions --------------------*1 
extern void get_vios ( struct vios * ); 
1*-- Type defs ----=------------------------------==*1 
typedef unsigned char BYTE; \frac{1}{2} /* Create a byte */
1*-- Structures -------------------------------------------------=-*1 
struct vios 1* Describes video card and attached monitor *1 
             BYTE vcard, 
                 monitor; 
            /; 
1*-- Constants ------------=-----------=--=---------=---=-=---*1 
1*-- Constants for the video card ------------------------------------*1 
\text{#define NO VIOS} 0 /* No video card */<br>
\text{#define VGA} 1 /* VGA card */
'define VGA 1 1* VGA card *1 
% #define EGA 2 /* EGA card */<br>
#define MDA 3 /* Monochrome Display Adapter */
\text{#define MDA} 3 /* Monochrome Display Adapter */<br>
\text{#define HGC} 4 /* Hercules Graphics Card */
% # define HGC 4 \neq 14 \neq 14 \neq 14 \neq 16 \neq 1
                                           'define CGA 5 1* Color Graphics Adapter *1 
1*-- Constants for monitor type --------------------------------------*1 
'define NO MON 0 1* No monitor *1 
'define MONO 1 1* Monochrome monitor *1 
'define COLOR 2 1* Color monitor *1 
% #define COLOR 2 <br>
#define EGA HIRES 3 /* High-res/multisync monitor */<br>
#define ANLG MONO 4 /* Analog monochrome monitor */
\text{define ANIG}\_\text{MOD}\quad\text{4}\quad\text{%}\quad\text{Analog monochrome monitor */}\n\text{define ANIG}\_\text{CODE}\quad\text{5}\quad\text{/*}\quad\text{Analog color monitor */}\n/* Analog color monitor */
/****••••••**•• *************** ••••*.*.******•••****•••****.*.*.*.*•••**/ 
                   MAIN PROGRAM
/.***••**•••••• *******************************************••********.**/ 
void main()
4
static char *vcnames[] - 1* Pointer to the video card name *1 
                           "VGA- , 
                           -EGA-,
```

```
"MOA", 
                          "HGC", 
                          "CGA" 
                         }; 
static char *monnames[] = \frac{1}{2} /* Pointer to the monitor type's name */
                           "monochrome monitor", 
                           "color monitor", 
                           "high-res/multisync monitor", 
                           "analog monochrome monitor", 
                           "analog color monitor" 
                          \cdotstruct vios vsys[2]; 1* Vector for GET_VIOS *1 
get vios( vsys ); 1* Determine video system *1 
printf("\nVIOSC (c) 1988 by Michael Tischer\n\n"); 
printf("Primary Video System: \\ \s card/ \\s\n",
        vcnames[vsys[O].vcard-lj, monnames[vsys[Oj .monitor-l]); 
if ( vsys[l].vcard !- NO VIas) 1* Is there secondary video system? *1 
  printf("Secondary Video System: %s card/ %s\n",
          vcnames[vsys[l].vcard-1j, monnames[vsys[l].monitor-1]); 
\mathbf{1}
```
#### Assembler listing: VIOSCA.ASM

*i\*\*\*\*\*\*\*\*\*·\*·\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*i*  ;\* VIOSCA \*; *i\*--\*i*  Task Creates a function for determining video ;\* ;\* adapter and monitor type, when linked with ;\* a C program. \*; \*; \*; *i\*---*---------------\*; ;\* Author MICHAEL TISCHER \*; ;\* Developed on : *10/02/1988* \*; ;\* Last update : *06/20/1989* \*; ;\*-----------------------~--\*: . \* Assembly : MASM VIOSCA; \*; ;\* •.• link to a C program \*; ;\*.\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* •••\*\*\*\**·\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*i i==* Constants for VIOS structure =--=========================---======= ;Video card constants  $NO_VIOS$  = 0<br>  $VGA$  = 1<br>  $VGA$  card<br>  $VGA$  $VGA = 1$ <br>EGA = 2  $EGA$  = 2 ; EGA card<br>MDA = 3 ; Monochron  $MDA$  = 3  $MDA$  ;  $Monochrome$  Display Adapter  $HGC$  = 4  $HGC$  $HGC = 4$ <br>  $CGA = 5$ <br>  $7Color Graphics Adapter$ ; Color Graphics Adapter ;Monitor constants  $NO$   $MO$   $= 0$  ; No monitor<br>  $MO$   $= 1$  ; Monochrome<br>  $COLOR$   $= 2$  : Color monitor = 1 ;Monochrome monitor<br>= 2 ;Color monitor COLOR = 2 ;Color monitor<br>
EGA HIRES = 3 ;High-resolution EGA HIRES =  $3$ <br> $\qquad$  ;High-resolution or multisync monitor<br> $N\overline{LG}$  MONO =  $4$ <br> $\qquad$  ;Analog monochrome monitor ANLG MONO = 4 ;Analog monochrome monitor<br>ANLG COLOR = 5 ;Analog color monitor ; Analog color monitor ;-- Segment declarations for the C program/--------==---======---=====- IGROUP group text ;Addition to program segment DGROUP group const, bss, \_data ;Addition to data segment DGROUP group const, bss, data ; Addition to data segma assume CS:IGROUP, DS:DGROUP, ES:DGROUP, SS:DGROUP CONST segment word public 'CONST';This segment includes all read-only<br>constants<br>constants ; constants \_BSS segment word public 'BSS' ; This segment includes all

 $BSS$ ends ; in-initialized static variables DATA segment word public 'DATA' ;Data segment vios tab equ this byte ;-- Conversion table for return values of function lAH, ;-- sub-function OOH of the VGA-BIOS db NO\_VIOS, NO\_MON ;No video card<br>db MDA , MONO ;MDA card and monochrome monitor<br>db CGA , COLOR ;CGA card and color monitor<br>db ? , ? ;Code 3 unused<br>db EGA , MONO ;EGA card and hi-res monitor<br>db EGA , MONO ;EGA card and mon db ? (Code 6 unused<br>db VGA , ANLG MONO ; VGA card and analog mono monitor<br>db VGA , ANLG COLOR : VGA card and analog color monitor , ANLG\_COLOR ; VGA card and analog color monitor ega dips equ this byte ;-- Conversion table for EGA card DIP switch settings ----- db COLOR, EGA HIRES, MONO db COLOR, EGA HIRES, MONO DATA ends ;-= Program --=========--==========-----------==-=-------------------== TEXT segment byte public 'CODE' ;Program segment public get vios **;--** ;-- GET VIOS: Determines types of installed video cards ---------------;-- Call from C : void get\_vios( struct vios \*vp ); ;-- Declaration : struct vios { BYTE vcard, monitor; }; **;-- Return value: none**  : This example uses function in SMALL memory model get vios proc near sframe **struc** ; Stack **access structure**  cga\_possi db ?<br>ega possi db ? tLocal variable;<br>Local variable; mono\_possi db ?<br>bptr dw ? bptr dw ? ;Take BP<br>ret adr dw ? ;Return : ret\_adr dw ? <br>vp dw ? <br>Pointer to first VIOS stigma and the context of t vp dw ;Pointer to first VIOS structure ; End of structure frame equ [ bp - cga\_possi ] ;Address elements of the structure push bp  $\begin{array}{ccc} 1 & \text{push BP onto stack} \\ \text{sub} & \text{sp.3} \end{array}$  : Allocate space for sub sp,3 ;Allocate space for local variables<br>mov bp, sp ;Transfer SP to BP mov bp,sp ;Transfer SP to BP push di **iPush 01 onto stack**  mov frame.cga possi,l ;Could be CGA mov frame.ega\_possi,1 ;Could be EGA mov frame.mono\_possi,l;Could be MDA or HGC mov di,frame.vp ;Get offset address of structure mov word ptr [di], NO VIOS ; Still no video mov word ptr [di+2], NO VIOS ; system found call test vga fest for VGA card cmp frame.egayossi,O ;EGA card still possible? ;NO --> Test for CGA

gvl: call test ega **;Test for EGA card** cmp frame.cga\_possi,0 ;CGA card still possible<br>je gv2 ;NO --> Test for MDA/HGC je gv2 ;NO --> Test for *MDA/HGC*   $\sigma v$ ? call test cga **; Test for CGA card** cmp frame.mono\_possi,0;MDA or HGC card still possibleh?<br>je qv3 ;NO --> End tests ;NO --> End tests call test mono ;Test for *MDA/HGC* cards ;-- Determine active video card --------------------------- gv3: cmp byte ptr [di], VGA ; VGA card active?<br>je gvi\_end ; YES, active card ;YES, active card already determined cmp byte ptr [di+2], VGA ; VGA card as secondary system?<br>je gvi\_end ; YES, active card already determ ;YES, active card already determined mov ah, OFh ;Determine active video mode using the int 10h :BIOS video interrupt ; BIOS video interrupt and al, 7  $\ldots$  ;Only modes 0-7 are of interest<br>cmp al, 7  $\ldots$  ;Monochrome card active? cmp al, 7 **implementary implement in the control of the c** jne gv4 **iNO,** in CGA or EGA mode ;-- MDA, HGC, or EGA card (mono) is active ---------------- cmp byte ptr [di+l],MONO ;MonQ monitor in first structure? je gvi end ;YES, Sequence o.k. jmp short switch ;NO, Change sequence ;-- CGA or EGA card currently active ---------------------- gv4: cmp byte ptr [di+1], MONO ; Mono monitor in first structure?<br>jne gviend ; NO, Sequence o.k. ; NO, Sequence o.k. switch:  $mov$  ax, [di] ;Get contents of first structure xchg ax, [di+2] ;Exchange with second structure mov [di], ax gvi\_end: pop di ; Get DI from stack<br>add sp,3 ; Get local variable add sp, 3 ; Get local variables from stack<br>pop bp ; Get BP from stack pop bp  $\begin{array}{ccc} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{array}$  ; Return to C program ; Return to C program \_get\_vios endp ,<br>;-- TEST\_VGA: Determines whether a VGA card is installed test\_vga proc near mov ax, la00h ;Function 1AH, sub-function 00H<br>int 10h ;calls VGA-BIOS  $\begin{array}{c} 10n \\ \text{cmp} \\ \text{dn} \\ \end{array}$ cmp al, lah ;Is this function supported?<br>jne tvga end ;NO --> End routine ;NO --> End routine ;-- If function is supported, BH contains the active video ;-- system code; BH contains the inactive video sys. code mov cx,bx ;Move result to CX<br>
xor bh,bh ;Set BH to 0<br>
or ch,ch ;Just one video system?<br>
je tvga\_1 ;YES --> Convey first s ;YES --> Convey first system's code ;-- Convert code of second system ------------------------- mov bl, ch ;Move second system code to BL<br>add bl, bl ;Add offset to table ;Add offset to table mov ax, offset DGROUP:vios\_tab[bx] ;Get code from table and

mov [d1+2], ax ;place in caller's structure<br>mov bl.cl : :Move first system's codes to ..<br>;Move first system's codes to BL ;-- Convert code of first system --------------------------  $tvga 1:$ add bl,bl ;Add offset to table<br>mov ax,offset DGROUP:vios\_tab[bx];Get code from table and<br>mov [di],ax ;place in caller's structure ;place in caller's structure mov frame.cqa possi, 0 ;CGA test failed mov frame.ega\_possi, 0 ; EGA test failed mov frame.mono\_possi,O ;MONO still needs testing mov bx,di ;Address of active structure<br>cmp byte ptr [bx],MDA ;Monochrome system available?<br>je do tmono ;YES --> Execute MDA/HGC test ;YES --> Execute MDA/HGC test add bx,2 ;Address of inactive structure<br>cmp byte ptr [bx],MDA ;Monochrome system available?<br>jne tvga end ;NO --> End routine ;NO --> End routine do tmono: mov word ptr [bx], 0 ; Pretend that this system ; is still unavailable mov frame.mono possi, 1; Execute monochrome test tvga end: ret ;Back to caller test vga endp **;--** ;-- TEST\_EGA: Determines whether an EGA card is installed test ega proc near mov ah, 12h ; Function 12H<br>mov bl.10h ; Sub-function mov bl,10h ;Sub-function 10H int 10h ; Call EGA-BIOS<br>
cmp bl, 10h ; Is the function cmp bl,10h ;Is the function supported?<br>je tega end ;NO --> End routine ;NO --> End routine ;-- When this function is supported, CL contains the EGA ----;-- card's DIP switch settings mov al, cl ;Move DIP switch settings to AL<br>shr al, 1 ;Shift one position to the right ; Shift one position to the right mov bx, offset DGROUP:ega\_dips ;Offset address of table<br>xlat . Woys element AL from table to Al xlat ;Move element AL from table to AL<br>mov ah, al ;Move monitor type to AH<br>mov al,EGA :It's an EGA card ; Move monitor type to AH mov al, EGA ;It's an EGA card<br>call found it ;Move data to vec ;Move data to vector cmp ah, MONO ;Connected to monochrome monitor?<br>je is mono ; YES --> not MDA or HGC ;YES --> not MDA or HGC mov frame.cga\_possi, 0 ; Cannot be a CGA card<br>jmp short tega end ; End routine jmp short tega\_end is\_mono: mov frame.mono-possi, 0; If EGA card is connected to a mono ;monitor, it can be installed as ;either an HGC or MDA tega\_end: ret ;Back to callerr test\_ega endp **;--** ;-- TEST\_CGA: Determines whether a CGA card is installed **proc near** 

mov dx,3D4h *j***CGA** tests port addr. of CRTC addr.<br>call test 6845 *i*reg., to see if 6845 is installed call test  $6845$  ireg., to see if 6845 is installed<br>jc tega end :NO --> End test  $; NO \rightarrow > End test$ mov al, CGA is installed<br>mov ah, COLOR : CGA has color monitor at mov ah, COLOR *iCGA* has color monitor attached jmp found it *iTransfer data to vector* ; Transfer data to vector test\_cga endo ï **;--** i-- TEST\_MONO: Checks for the existence of an MDA or HGC card test\_mono proc near mov dx,3B4h ;Check port address of CRTC addr. reg.<br>call test 6845 :with MONO to see if there's a 6845 ; with MONO to see if there's a 6845 *i* installed jc tega end iNO --> End test ;-- If there is a monochrome video card installed, the -----:-- following determines whether it's an MDA or an HGC -----mov dl, OBAh ;Read MONO status port using 3BAH in al,dx<br>and al,80h  $\cdot$  : and al,80h ;Check bit 7 only and mov ah,al **imove to AH ;--** If contents of bit 7 change during one of the following **i--** readings, the card is handled as an HGC mov cx,8000h ;Maximum of 32768 loop executionse mov cx, 8000h<br>test\_hgc: in al,dx<br>and al,80h and al,80h ; Check bit 7 only cmp al, ah  $\therefore$  contents changed?<br>jne is hgc  $\therefore$  Bit 7 = 1 --> HGC jne is\_hgc  $;$  Bit  $7 = 1$  --> HGC<br>loop test hgc  $;$  Continue loop ;Continue loop mov al, MDA ; Bit 7 <> 1 --> MDA<br>jmp set\_mono. ; Set parameters ;Set parameters  $is\_hgc:$  mov al, HGC ;Bit  $7 = 1$  --> 1st HGC set mono: mov ah, MONO :MDA/HGC on mono monito mov ah, MONO ;MDA/HGC on mono monitor<br>
jnp found it ;Set parameters ;Set parameters test mono endp **;---** i-- TEST\_6845: Sets carry flag if no 6845 exists in port address of OX test 6845 proc near mov al, OAh iP and the service of the serv out dx, al  $;$  Register number of CRTC address reg.<br>inc dx  $;$  DX now in CRTC data register ;DX now in CRTC data register in al,dx ; Get contents of register 10<br>mov ah,al ; and move to AH ; and move to AH mov al,4Fh ;Any value<br>out dx,al ;Write to register 10 mov cx, 100 ;Short delay loop--gives 6845 time<br>loop wait ; to react wait: loop wait foreact in al,dx ;Read contents of register 10 xchg al,ah ;Exchange AH and AL out dx, al (3) ; Send old valuen cmp ah, 4Fh iWritten value read?

je t6845 end ;YES --> End test stc  $;NO \rightarrow Set carry flag$ t6845 end: ret ; Back from caller test 6845 endp **;--** ;- FOOND\_IT: Transfers video card type to AL and monitor type to ;- AH in the video vector found it proc near mov bx,di ;Address of active structure<br>cmp word ptr [bx],0 ;Video system already onboard cmp word ptr [bx], 0 ; Video system already onboard?<br>je set\_data : NO --> Data in active structu ;NO --> Data in active structure add bx, 2  $;$  7ES, Address of inactive structure set\_data: mov [bx], ax ;Place data in structure<br>ret ;Back to caller ; Back to caller found it endp **;---** text ends ; Find of code segment<br>end ; Find of program ; End of program

#### **Pascal listing: VIOSP.PAS**



```
program VIOSP;
```

```
{SL c:\masm\viospal { Link assembler module 
                                       Change path to suit your DOS needs 
\begin{array}{lll}\n\text{const} & \text{NO} & \text{VIOS} & = & 0; \\
\text{VGA} & = & 1; & \n\end{array}
{ No video card }
      VGA = 1; \{ VGA \text{ card }<br>EGA = 2; \{ EGA \text{ card }EGA = 2; { EGA card }<br>MDA = 3; { Monochrome Display Adapter }
      MDA = 3; (Monochrome Display Adapter )<br>HGC = 4; (Hercules Graphics Card )
      HGC = 4; GCA = 5; GAA + GCA + GAA 
                                                    { Color Graphics Adapter }
      NO MON = 0;<br>MONO = 1;<br>MONO = 1;<br>{ Monochrome monitor }
       MONO "'" 1; Monochrome monitor 
      COLOR = 2;<br>
EGA HIRES = 3;<br>
{ High-resolution monitor }
      EGA HIRES = 3;<br>
ANLG MONO = 4;<br>
{ Monochrome analog monitor }
      ANLG_MONO = 4;<br>ANLG_COLOR = 5;<br>{Color analog monitor }<br>{Color analog monitor }
                                                      { Color analog monitor }
type Vios = record { Describes video card and attached monitor }
              Vcard, 
              Monitor : byte;
             end;
```

```
{ Pointer to a VIOS structure }
    ViosPtr = \gamma Vios;procedure GetVios(vp : ViosPtr ) ; external ;
var VidSys : array[1..2] of Vios; { Array containing video structures }
* PrintSys: Gives information about a video system
                                                           \star{* Input : - VCARD: Code number of the video card
                                                            \star- MON : Code number of the attached monitor
                                                           \star}
\mathbf{f}^{\star}\star )
{* Output : none
procedure PrintSys ( VCard, Mon : byte );
begin
 write('');
 case VCard of
   NO VIOS : write ('Unknown');
                              { For "other" code }
   VGA : write('VGA');
   EGA : write('EGA');
   MDA : write('MDA');
   CGA : write('CGA');
   HGC: write('HGC');end;
 write('card/');case Mon of
   NO MON : write ('unknown monitor'); { For "other" monitors }
   \begin{array}{ll}\n\text{MONO} & \text{:\n  written (monochrome monitor');\n}\n\text{CONOR} & \text{:\n  written (nonochrome monitor');\n}\n\end{array}COLOR
            : writeln('color monitor');
   EGA HIRES : writeln('high-resolution monitor');
   ANLG MONO : writeln ('monochrome analog monitor');
   ANLG COLOR : writeln('color analog monitor');
 end:
end:
*MAIN PROGRAM
                                                          ***begin
 GetVios(@VidSys);
                                    { Check installed video card }
 writeln('VIOSP - (c) 1988 by MICHAEL TISCHER');
 write('Primary video system: ');
 PrintSys(VidSys[1].VCard, VidSys[1].Monitor);
 writeln(#13#10);
 if VidSys[2].VCard <> NO VIOS then { Second video system installed? }
   begin
                                                       {YES}write('Secondary video system:');
     PrintSys(VidSys[2].VCard, VidSys[2].Monitor );
     writeln(13,10);
   end:
end.
```
#### Assembler listing: VIOSPA.ASM



 $; *$ ٠, ... Link to a Turbo Pascal program  $, \star$ using the {\$L VIOSPA} compiler directive \*; ;== Constants for the VIOS structure === ;Video card constants NO VIOS  $= 0$ ;No video card/unrecognized card VGA  $-1$ :VGA card **EGA**  $-2$ ;EGA card **MDA**  $-3$ ;Monochrome Display Adapter HGC : Hercules Graphics Card  $= 4$  $= 5$ CGA ;Color Graphics Adapter ;Monitor constants  $= 0$ NO MON ;No monitor/unrecognized code **MONO**  $= 1$ ;Monochrome monitor ;Color Monitor **COLOR**  $= 2$ ; High-resolution/multisync monitor EGA HIRES =  $3$ ANLG MONO =  $4$ ;Monochrome analog monitor  $ANLG$  COLOR = 5 ;Analog color monitor "= Data segment ===== ----------------------segment word public ;Turbo data segment **DATA DATA** ends ;== Code segment ======= CODE segment byte public ; Turbo code segment assume cs:CODE, ds:DATA public getyios ;-- Initialized global variables must be placed in the code segment ---vios tab equ this word ;-- Conversion table for supplying return values of VGA ----;-- BIOS function 1A(h), sub-function 00(h) db NO VIOS, NO MON ; No video card ; MDA card/monochrome monitor  $db$  MDA , MONO db CGA , COLOR Particular Code 3 unused<br>
2 (2016 3 unused<br>
2 (2016 2017) EGA card/monochrome monitor<br>
2 (2016 6 unused<br>
2 (2016 6 unused<br>
2 (2016 6 unused<br>
2 (2016 1000 1920 2017)<br>
2 (2016 1018 2017) Particular Code<br>
2 (2017 1018 2017)  $db$ ? db EGA db EGA  $db$  ? db VGA db VGA , ANLG COLOR ; VGA card/analog color monitor ega dips equ this byte :-- Conversion table for EGA card DIP switches ----db COLOR, EGA HIRES, MONO db COLOR, EGA HIRES, MONO ;-- GETVIOS: Determines type(s) of installed video card(s) ----------;-- Pascal call : GetVios ( vp : ViosPtr ); external; ;-- Declaration : Type Vios = record VCard, Monitor: byte; ;-- Return Value: None getvios proc near sframe struc ;Stack access structure cga possi db ? ; local variables

ega\_possi db ? ;local variables<br>mono possi db ? ;local variables mono\_possi db ?<br>bptr dw ? bptr dw ? ;BPTR<br>ret adr dw ? ;Retu dw ? Feturn address of calling program<br>dd ? Pointer to first VIOS structure vp dd ? ;Pointer to first VIOS structure : End of structure frame equ [ bp - cga possi ] ;Address elements of structure push bp  $\begin{array}{ccc} 1 & \text{push} & \text{BP} \\ \text{sub} & \text{sp},3 & \text{in} \\ \end{array}$ sub sp, 3 ;Allocate memory for local variables<br>mov bp, sp ;Transfer SP to BP ;Transfer SP to BP mov frame.cga possi, 1 ; Is it a CGA? mov frame.ega possi, 1; Is it an EGA? mov frame.mono possi, 1; Is it an MDA or HGC? mov di,word ptr frame.vp ;Get offset addr. of structure mov word ptr [di],NO VIOS ;No video system or unknown mov word ptr [di+2], NO\_VIOS ; system found call test\_vga **;Test for VGA card** cmp frame.ega\_possi,0 ;Or is it an EGA card?<br>je qvl :NO -->Go to CGA test ;NO -->Go to CGA test call test\_ega **;Test for EGA card** gvl: cmp frame.cga\_possi,0 ;Or is it a CGA card?<br>de qv2 :NO --> Go to MDA/HGC ;NO --> Go to MDA/HGC test call test cga ;Test for CGA card gv2: cmp frame.mono\_possi,0;Or is it an MDA or HGC card?  $j$ e gv3  $j$ NO --> End tests call test mono ; Test for MDA/HGC card ;-- Determine video configuration ------------------------- gv3: cmp byte ptr [di],VGA ;VGA card? je gvi end ;YES --> Active card already indicated cmp byte ptr [di+2], VGA; VGA card part of secondary system? je gvi\_end ;YES -~> Active card already indicated ;Determine video mode using BIOS video mov ah,OFh int lOh ; interrupt and al,7 ;only modes 0-7 are of interest  $cmp$  al,  $7$ ;Mono card active? jne gv4 ;NO --> CGA or EGA mode ;-- MIlA, HGC or EGA card (mono) currently active ---------- cmp byte ptr [di+1],MONO ;Mono monitor in first structure? gvi\_end ;YES, Sequence o.k. je jmp short switch ;NO, Switch sequence ;-- CGA or EGA card currently active --gv4: crop byte ptr [di+l],MONO ;Mono monitor in first structure? jne gvi end ;NO -->Sequence o.k. switch: mov ax, [di] ;Get contents of first structure  $xchg$  ax,  $[d1+2]$ ;Switch with second structure mov [di],ax gvi end: add sp,3 ;Add local variables from stack pop bp ; Pop BP off of stack ret 4 ;Clear variables off of stack; ;Return to Turbo getvios endp

**;--** ;-- TEST\_VGA: Determines whether a VGA card is installed test vga proc near mov ax, 1a00h ; Function 1A(h), sub-function 00(h)<br>int 10h ; Call VGA-BIOS int 10h ;Call VGA-BIOS<br>
cmp al,1ah ;Function supp cmp al, lah ; Function supported?<br>jne tvga\_end ; NO --> End routine ;NO --> End routine ;-- If function is supported, BL contains the code of the ;-- active video system, while BH contains the code of ;-- the inactive video system mov cx,bx ;Move result in CX<br>xor bh,bh ;Set BH to 0 xor bh, bh ;Set BH to 0<br>or ch, ch ;Only one vi or ch,ch ;Only one video system?<br>je tvga 1 ;YES --> Display first je tvga\_l ;YES --> Display first system's code ;-- Convert code of second system ------------------------- mov bl, ch ;Move second system's code to BL<br>add bl, bl ;Add offset to table add bl, bl ;Add offset to table<br>mov ax, vios tab [bx] ;Get code from table mov ax, vios\_tab [bx] ;Get code from table and move into<br>mov [di+2], ax ;caller's structure mov [di+2], ax ;caller's structure<br>mov bl, cl ; Move first system' ; Move first system's code into BL ;-- Convert code of second system ----add bl,bl ;Add offset to table<br>mov ax,vios tab[bx] ;Get code from table  $tvga_1$ : ;Get code from table mov [di], ax ; and move into caller's structure mov frame.cga\_possi, 0 ;CGA test fail? mov frame.ega\_possi,0 ;CGA test fail? mov frame.mono possi, 0 ;Test for mono mov bx,di ;Address of active structure cmp byte ptr [bx], MDA ; Monochrome system online?<br>je do tmono : YES --> Execute MDA/HGC to ;YES --> Execute MDA/HGC test add bx, 2 ;Address of inactive structure cmp byte ptr  $[bx]$ , MDA ; Monochrome system online?<br>jne tvga end ; NO --> End routine ;NO --> End routine do tmono: mov word ptr [bx],O ;Emulate if this system mov frame.mono possi, l; Execute monochrome test tvga end: ret ; Return to caller test vga endp **;--** ;-- TEST\_EGA: Determine whether an EGA card is installed test\_ega proc **near**  mov ah, 12h ; Function 12(h)<br>mov bl, 10h ; Sub-function 1 mov bl,10h ;Sub-function 10(h)<br>int 10h :Call EGA-BIOS int lOh ;Call EGA-BIOS cmp bl, 10h ; Is this function supported?<br>je tega end ; NO --> End routine ;NO --> End routine ;-- If the function IS supported, CL contains the ;-- EGA card DIP switch settings mov bl,cl ;Move DIP switches to BL<br>shr bl,1 ;Shift one position to the shr bl, 1 ; Shift one position to the right<br>xor bh, bh ; Index high byte to 0 ; Index high byte to 0

mov ah, ega\_dips[bx] ;Get element from table<br>mov al,EGA ;Is it an EGA card? mov al, EGA ; is it an EGA card?<br>
call found it ;Transfer data to the vector cmp ah, MONO ; Mono monitor connected?<br>je is mono ; YES --> Not MDA or HGC ; YES --> Not MDA or HGC mov frame.cga\_possi, 0 ;No CGA card possible jmp short tega\_end ;End routine is\_mono: mov frame.mono possi, O;EGA can either emulate MDA or HGC, ; if mono monitor is attached tega end: ret ;Back to caller test ega endp ;-- ;-- TEST\_CGA: Determines whether a CGA card is installed test\_ega proc near mov dx,3D4h ;Port addr. of CGA's CRTC addr. reg.<br>call test\_6845 ;Test for installed 6845 CRTC<br>jc tega\_end ;NO --> End test mov al, CGA ;YES, CGA installed<br>mov ah, COLOR ;CGA uses color mon mov ah, COLOR ; CGA uses color monitor<br>imp found it ; Transfer data to vector ;Transfer data to vector test cga endp *i--*------------ ;-- TEST\_MONO: Checks for MDA or HGC card test\_mono proc near mov dx,3B4h ;Port addr. of MONO's CRTC addr. reg.<br>call test 6845 ;Test for installed 6845 CRTC ;Test for installed 6845 CRTC jc tegaend ;NO --> End test ;-- Monochrome video card installed  $---$ ;--<br>mov dl,0BAh ; MONO status port at 3BA(h) in al,dx ;Read status port<br>and al,80h ;Separate bit 7 am and al,80h ; Separate bit 7 and mov ah,al ; move to AH ;move to AH ;-- If the contents of bit 7 in the status port change  $;--$  during the following readings, it is handled as an  $---$ <br> $;--$  HGC  $--$ mov cx,8000h ;maximum 32768 loop executions<br>in al,dx ;Read status port test\_hgc: in al,dx<br>and al,80h and al,80h ;Isolate bit 7 anp al,ah ;Contents changed? dom al, ah ; contents changed?<br>
jne is hgc ; Bit 7 = 1 --> HGC<br>
loop test hgc ; continue<br>
(continue loop test hgc inov al,MDA ;Bit 7 <> 1 --> MDA jmp set mono iset parameters is\_hgc: mov al, HGC  $\qquad$  ; Bit  $7 = 1$  --> HGC<br>set mono: mov ah, MONO ; MDA and HGC set as mov ah, MONO ;MDA and HGC set as mono screen<br>imp found it ;Set parameters ;Set parameters test\_mono endp

*i---*----------------- ;--'TEST\_6845: Returns set carry flag if 6845 doesn't lie in the

```
;-- port address in DX 
test 6845 proc near 
            mov al, OAh ; Register 10<br>out dx, al ; Register nu
             out dx, al ; Register number in CRTC address reg.<br>inc dx : DX now in CRTC data register
                                      ;DX now in CRTC data register
            in al,dx ;Get contents of register 10<br>mov ah,al ;and move to AH
                                      ;and move to AH
            mov al,4Fh ;Any value<br>out dx,al ;Write to :
                                       ;Write to register 10
            mov cx,100 ; Short wait loop to which<br>loop wait ; 6845 can react
wait: loop wait ;6845 can react
            in al,dx ;Read contents of register 10<br>xchg al,ah ;Exchange Ah and AL
            xchg al,ah ; Exchange Ah and AL 
                                       ;Send value
             cmp ah,4Fh ; Written value been read?<br>je t6845_end ; YES --> End test
                                       ;YES --> End test
             stc ;N0 \rightarrow Set \ carry \ flagt6845_end: ret ; Back to caller
test 6845 endp 
;----------------------------------------------------------------------
;-- FOUND_IT: Transfers type of video card to AL and type of 
;-- monitor in AH in the video vector 
found it proc near
             mov bx,di ;Address of active structure 
cmp word ptr [bx],O ;Video system already onboard? 
            omp word ptr (bx), 0 ; Video system already onboard?<br>je set_data ;NO --> Data in active structure
            add bx, 2 ; YES --> Address of inactive structure
set_data: mov [bx], ax ;Place data in structure<br>ret :Back to caller
                                       ;Back to caller
found_it endp 
;----------------------------------------------------------------------
code ends ;End of code segment<br>end end :End of program
                                       ; End of program
```
## **10.7 Accessing Video RAM from High Level Languages**

The beginning of this chapter mentioned the option of video RAM access from high level languages. This would allow the developer to write screen output routines for high level languages that would execute faster than output commands available to the languages, BIOS functions, or DOS functions. This option would be particularly attractive if it meant that we could write these routines without assembly language programming.

The demonstration programs below implement direct video RAM access routines which display a string on the screen. Althrough there are some major differences between the three programs as a result of the differences between the respective languages (BASIC, Pascal and C), all three programs contain the same elements.

## Initialization

Each program includes an initialization routine which determines the segment address of the video RAM. The routine has a variable which contains the address of the CRTC address register. There is a direct relationship between the video RAM and this address register: just as this register is always at port address 3B4H, the video RAM on a monochrome card is always found at segment address BOOOH. This combination also applies to color cards, where the address register is at port address 3D4H and the video RAM is at segment address B800H. If we know the port address of the CRTC address register, we can determine the segment address of the video RAM. Once we have determined this address, we can place it in a global variable and execute the initialization routine.

## **Output**

All three programs have an output routine which uses the segment address we determined above. Each time the routine displays something, it determines the starting address of the video page currently displayed on the screen. This ensures that the output appears on the visible screen, and not on an undisplayed video page. We can find this from the CRT\_START BIOS variable. This variable is located at address 0040:OO4E, and specifies the offset address of the displayed video page relative to the video page found at offset address OOOOH.

After this address is determined, we can access the video RAM. The method used in the program depends on the given programming language. Let's look at each program in more detail.

#### The C implementation

From a programming point of view, this is the cleanest of the three implementations because the video RAM can be treated as a normal variable in C. We first define the structure VELB, which describes the ASCII/attribute pair as it appears in the video RAM. We create a new data type, VP, to act as a pointer to this structure. It is important that this pointer be of type FAR because these

structures are in the video RAM and therefore outside the C data segment. Smaller memory models in C require the declaration of this pointer as a FAR pointer.

The global variable VPTR is initialized to be a pointer to the first ASCII/attribute pair in page 0 of the video RAM. This occurs in the INIT\_DPRINT routine. It is used within the DPRINT function (the function used for display) as the basis for addressing the characters within the video RAM.

The DPRINT function loads the LPTR pointer with the address of the screen output position passed to the routine. LPTR is fIrst loaded with the contents of the global variable VPTR, and then with the offset address of the active video page, as found in the CRT\_START BIOS variable. LPTR must be cast as a BYTE pointer because the contents of the BIOS variable refers to bytes, and not to VELB structures. If the cast operator were missing, the C compiler would generate code which would first multiply the contents of the BIOS variable by the length of the VELB structure before adding it, resulting in the wrong value.

We can now add the display position to this pointer. The output position is passed to DPRINT as row and column coordinates. The video RAM is treated as an array of 2000 components, each of which is a VELB structure. Since we have computed the base address of the array in LPTR, all we need is to index into it. We multiply the row coordinate by 80 (columns per line) and then add the column coordinate. Finally we have a pointer to the output position in video RAM, which we can treat like any other C pointer.

Each time through, the loop increments the pointer to the next VELB structure. We write the ASCII code of the character and the color passed to DPRINT to the specified address. This repeats until the program reaches the end of the string.

C listing: DVIC.C

```
/******.***** ••*****••*****•••**•••****•••• ****.***.**************•••• */ 
1* D v I C *1 
 1*--------------------------------------------------------------------*1 
1* Task : Demonstrates direct access to video RAM. *I 
 1*--------------------------------------------------------------------*1 
1* Author : MICHAEL TISCHER *I 
 1* Developed on : 10101/1988 *1 
1* Last update : 06/2111989 *I 
1*--------------------------------------------------------------------*1 
1* (MICROSOFT C) *1 
 1* Creation : CL lAS DVIC.C *1 
1* Call : DVIC *I 
1*--------------------------------------------------------------------*1 
1* (BORLAND TURBO C) *1 
1* Creat ion : RUN menu cOJliMnd (no project file needed) *I /* ••***••**************************************.******•• ***************/ 
I*~- Include files -~~~==~~~~~--~==-=-====---~=~-----------==========*I 
'include <dos.h> 
'include <stdlib.h> 
'include <string.h> 
'include <stdarg.h> 
#include <br/> <br/>bios.h>
```

```
/*-- Type definitions ~=--=---~-*/ 
typedef unsigned char BYTE; /* Create a byte */ 
typedef struct velb far * VP; /* VP - FAR pointer in video RAM * / 
/*-- Structures ---------- --*/ 
typedef BYTE BOOL; /* similar to BOOLEAN in Pascal */ 
struct velb { /* Describes a 2-byte position on the screen */<br>BYTE character, /* ASCII code */
            BYTE character, \arctan/* Character attribute */
           I; 
/-!II<'. Macros ______________*/ 
/*-- MK_FP creates a FAR pointer to an object from a segment -----*//*-- address and offset address
Hfndef MK FP /* MK FP not defined yet? */ 
#define MK_FP (seg, ofs) ((void far *) ((unsigned long) (seg) <<16| (ofs)))
.endit 
'define COLOR(VG, HG) 	 (fVG« 3) + HG) 
/*-== Constants 	_~_===---=:r;-==-= _____----====*/
\#define TRUE 1 /* Constants for use with BOOL */
'define FALSE 0 
/*-- The following constants return pointers to variables from the ---*/<br>/*-- BIOS variable segment at segment address 0x40
/*-- BIOS variable segment at segment address 0x40
'define CRT START «unsigned far *) MK FP(Ox40, Ox4E» 
#define ADDR 6845 ((unsigned far *) MK FP(0x40, 0x63))
'define NORMAL OxO? /* Character attribute definition */ 
                     0x0f /* Based on monochrome video card*/<br>0x70
#define INVERSE
'define UNDERSCORED Ox01 
\#define BLINKING
'define BlACK OxOO /* Color attributes for color card */ 
               0 \times 01<br>0 \times 02#define GREEN
'define COBALTBLUE Ox03 
'define RED Ox04 
'define VIOLET Ox05 
%define BROWN 0x06<br>%define LIGHTGRAY 0x07
'define LIGHTGRAY OxO? 
'define DARKGRAY Ox01 
'define LIGHTBLUE Ox09 
\#define LIGHTGREEN
'define LIGHTCOBALT OxOB 
\texttt{\#define } LIGHTRED
fdefine LIGHTVIOLET OxOD 
%WELLOW OXOE<br>#define YELLOW OXOE<br>#define WHITE OXOF
#define WHITE
/*-= Global variables -~~------=--./ 
VP vptr; /* pointer to first character in video RAM */ 
, ••••••••••••••***.**.***.**•••••••••••••••••••••***••*******••••*.*.*•• 
 Function : 0 P R I N T 
**----------------------------------------------------------------------** 
* Task : Writes a string directly to video RAM
* Input parameters : - COLUMN = Output column * *<br>
* - LINES = Output row * * - COLOR = Character attribute * *
```

```
Abacus
```

```
- STRING - Pointer to string
                                                         ٠
* Return value : None
void dprint (BYTE column, BYTE lines, BYTE color, char * string)
\mathbf{f}/* Floating pointer in video RAM */
register VP lptr;
register BYTE i;
                             /* Points to number of characters */
/*-- Set pointer to output position in video RAM ---
                                                        —∗/
lptr = (VP) ((BYTE far *) vptr + *CRT START) + lines * 80 + column;
for (i=0; *string; ++lptr, ++i)/* Execute string */
  1ptr->character = *(string++);<br>
\frac{1}{2} /* Character in video when \frac{1}{2}<br>
/* Set character attribute */
 \mathbf{I}\mathbf{1}\mathbf{I}* Function : INIT DPRINT
***--* Task
           : Determines video RAM segment address for DPRINT *
 Input parameters : None
* Return value : None
* Info
              : Allocates segment address of video RAM in VPTR *
                 global variable
void init dprint ()
\mathbf{f}vptr = (VP) MK FP( (*ADDR 6845 == 0x3B4) ? 0xB000 : 0xB800, 0);
\mathbf{I}Function : C L S
* Task
          : Clears the screen with the help of DPRINT
\star* Input parameters : - COLOR = Character attribute
                                                         \bullet* Return value : None
***********************
                    void cls ( BYTE color )
\mathbf{f}static char blankline [81] =
 a shi ne ne ne har bir ne ne ne ne ne ne ne ne ne.<br>Tir ne her ne ne
   وكالموارد والإسماع والموارد والإسماع والمراجع والموارد والإسماع
                                          エチ・チャチ
   \alpha , \beta , \alpha , \beta , \alpha , \beta , \alpha , \beta , \alpha , \alpha};
register BYTE i;
                                           /* Loop counter */
for (i=0; i<24; ++i)/* Execute each line */
 dprint (0, i, color, blankline);
                                      /* Display blank line */
J
* Function : NOKEY
***\star Task
          : Tests for a keypress
* Input parameters : None
* Return value : TRUE if a key is pressed, otherwise FALSE
******************
               ************
```

```
BOOL nokey ()
```

```
#ifdef TURBOC
                                           /* Using Microsoft C */
telse
return( _bios_keybrd( _KEYBRD READY ) == 0 );
                                                 /* Read from BIOS */
#endif
\star\starMAIN PROGRAM
1 + tvoid main ()
 BYTE firstcol, \sqrt{*} Color of first square on the screen */color,
                                         /* Color of current square */
                                         /* Current output position */
     column.
     lines;
 init dprint ();
                          /* Determine segment address of video RAM */
 cls(COLOR(BLACK, GREEN));/* Clear screen */
 dprint (22, 0, WHITE, "DVIC - (c) 1988 by Michael Tischer");
dprint (22, 0, \ldots)<br>firstcol = BIACK ;
                                               /* Start with black */
                           /* Repeat until the user presses a key */
 if (++firstcol > WHITE)<br>
if (++firstcol = BLUE;<br>
color = firstcol;<br>
(* YES, continue with blue */<br>
color = firstcol;<br>
(* Set first color on the screen */
   /*-- Fill screen with squares --------------------------
   for (column=0; column < 80; column += 4)
    for (lines=1; lines < 24; lines += 2)
     dprint ( column, lines,  color, "\blacksquare");/* Block characters can */<br>dprint ( column, lines+1, color, "\blacksquare");/* be created by press-*/
                                        /* ing <Alt><2><1><9> */
     color = +color + 4.15;
    \mathbf{I}\overline{\phantom{a}}\mathbf{I}
```
#### The Pascal implementation

By using the keyword ABSOLUTE or by linking in a small assembly language routine it would also be possible to treat the video RAM as a normal variable in Turbo Pascal. But there's an easier way.

Turbo Pascal offers the arrays MEMW and MEM for accessing memory which is outside of the data segment of the Turbo Pascal program. The array MEM consists of bytes and the array MEMW of words. The two arrays don't actually exist and are just mapped to the address space, but that doesn't affect their usefulness.

We can write values into the array as well as read from it. This is done with the following statement:

MEMW [ segment address : offset address ] := expression

 $\alpha$ 

variable := MEMW[ segment address : offset address ]

The MEM array might be easier to use for this particular application since we will be alternating between ASCII characters and a constant attribute. However, the output procedure DPrint uses the MEMW array instead, because 16-bit accesses are performed faster than two successive 8-bit accesses on 16-bit machines.

When accessing the MEMW array, DPrint takes the segment address of the video RAM from the variable VSeg, which is initialized at the start of the program in the procedure InitDPrint. As described before, this is done by examining the BIOS variable which contains the port address of the CRTC address register. This and the other BIOS variables are declared using the ABSOLUTE keyword, allowing them to be used in the program like any other global variables.

The offset within the MEMW array is computed from the starting address of the screen page. The coordinates are passed to DPrint, in which the row coordinate is multiplied by 160 and the column coordinate by two. When running through the string to be printed, the memory offset is incremented by two on each pass, moving it one ASCII/attribute pair to the right.

#### Pascal listing: DVIP.P

**(\*.\* ••• \*\*\*\*\*\*\*\*\*\*••\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*••\*\*\*\*\*••••\*.\*.\*\*\*\*••••••••\*\*\*\*\*\*\*\*\*)**  ${\small \begin{array}{l} \text{\texttt{\texttt{\texttt{*}}}} & \text{\texttt{b}} & \text{\texttt{v}} & \text{\texttt{r}} \\ \text{\texttt{\texttt{*}}}} & \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} \\ \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} \\ \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} \\ \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} & \text{\texttt{*}} \\ \text{\texttt{*}} & \text{\$ (\* Turbo Pascal \*)<br>
(\* 1990)<br>
(\* Author : MICHAEL TISCHER \*)<br>
(\* Developed on : 10/02/1989)<br>
(\* Last update : 06/20/1989)<br>
(\* Last update : 06/20/1989) program DVIP; Uses Crt, Dos;  ${ \text{Use CRT and DOS units } }$ const NORMAL = \$07;  $\begin{array}{r} 1 \quad \text{Self:} \\ 1 \quad \text{Self:} \end{array}$  = \$01;  $\begin{array}{r} 1 \quad \text{Self:} \\ 0 \quad \text{Output:} \end{array}$ LIGHT =  $$0f;$  { conjunction with monochrome }<br>INVERSE =  $$70;$  { video card INVERSE *- \$70;* { video card } UNDERSCORED =  $$01;$ <br>BLINKING =  $$80;$ BLINKING BIACK =  $$00;$  { Color attributes for color card }<br>BIJIE =  $$01$  $= $01;$  $GREEN = $02;$  $COBALTBLUE = $03;$ <br>RED =  $$04:$ RED  $= $04;$ <br>VIOLET  $= $05;$  $= $05;$  $BROMN = $06;$  $LIGHTGRAY$  = \$07;<br>DARKGRAY = \$01: = \$01;<br>= \$09; LIGHTBLUE = \$09;<br>LIGHTGREEN = \$0A; LIGHTGREEN LIGHTCOBALT =  $$0B;$ <br>LIGHTRED =  $$0C;$ LIGHTRED LIGHTVIOLET = \$0D; YELLOW = \$0E;  $WHITE = 50F;$ type TextTyp =  $string[80]$ ; var VSeg : word; { Segment address of video RAM }

 $\mathfrak{i}_{\mu_\alpha}$ 

```
\star{* InitDPrint: Determines segment address of video RAM for DPrint
                                                          \star{* Input : none
{* Output : none
                                                          \starprocedure InitDPrint;
var CRTC PORT : word absolute $0040:0063; { Variable in BIOS var.seg. }
begin
 if CRTC PORT = $3B4 then
                                  { Monochrome card connected? }
   VSeq := $B000{ YES, video RAM at B000:0000 }
                                   { NO, must be a color card }
 else
   VSeq := $B800;{ Video RAM at B800:0000 }
end:
{* DPrint: Writes a string direct into video RAM
                                                          \star{* Input : - COLUMN: Output column
                                                          \star- LINES : Output line
\uparrow\star\{ \star- COLOR : Color (attribute) for individual characters
                                                          \star\uparrow- STROUT: String to be displayed
                                                          \star }
{* Output : none
                                                          \starprocedure DPrint ( Column, Lines, Color : byte; StrOut : TextTyp);
var PAGE OFS : word absolute $0040:$004E; { Variable in BIOS var.seg. }
   Offset : word; { Pointer to current output position }
   1, 1: byte;
                                              { Loop counter }
   Attribute : word;
                                        { Attribute for output }
begin
 Offset := Lines * 160 + Column * 2 + PAGE OFS:
 Attribute := Color shl 8; { High byte for word access to video RAM }
 i := length(StrOut);{ Determine string length }
 for j:=1 to i do
                                            { Execute string }
   begin
               { Put character & attribute directly into video RAM }
    memw[VSeg:Offset] := Attribute or ord( StrOut[j]);
    Offset := Offset + 2; { Set offset to next ASCII/attribute pair }
   end:
end:
{* Demo: Demonstrates application of DPrint
                                                          \starj
{* Input : none
                                                          \star }
{* Output : none
                                                          \starprocedure demo;
var Column,
                                     { Current output position }
   Lines,
   Color
        : integer;
begin
 TextBackGround(BLACK);
                                       { Turn background black }
 ClrScr;
                                              { Clear screen }
 DPrint (22, 0, WHITE, 'DVIP - (c) 1988 by Michael Tischer');
 Randomize:
                               { Enable random number generator }
 while not KeyPressed do
                              { Repeat until user presses a key }
   begin
     Column := Random(76):
                                     { Select column, row and }
    Lines := Random( 22 ) + 1;<br>Color := Random( 14 ) + 1;
                                     { color at random
                                                           \overline{\phantom{a}}Color := Random( 14 ) + 1;
    DPrint ( Column, Lines, Color, '[[[['); { Block character can be }
```

```
DPrint ( Column, Lines+1, Color, '[[[['); { created by pressing
                                             \overline{\phantom{a}}end;
                             {<Alt><2><1><9>
 ClrScr;
                                   I Clear screen I
end;
****MAIN PROGRAM
begin
 InitDPrint;
                       { Initialize output using DPrint }
 Demo;
                               { Demonstrate DPrint }
end.
```
#### The BASIC implementation

This version doesn't really fulfill its goal, since it is slower than the already slow PRINT command. But we have included it for the sake of completeness, and because it is a good example of how you can access the entire address space of the 8088 from within BASIC.

The commands DEF SEG, PEEK, and POKE are the heart of memory access in BASIC. DEF SEG sets the segment address of the "current" 64K segment. PEEK and POKE can then be used to read and write bytes from or to this segment. This technique is used in the initialization routine at line number 50000, which first defines the BIOS variable segment as the current segment. From there two PEEK commands read the port address of the CRTC address register and the variable VR is loaded with the segment address of the video RAM.

This address is used in the output routine at line number 51000 in combination with the DEF SEG command, which defines the video RAM as the current segment. But first we calculate the offset address in the video RAM by reading the start address of the current screen page from the BIOS variable area and then adding the offset address of the output position within the video RAM. As in the Pascal version, this is calculated by adding the product of the row coordinate (variable CLINE%) by 160 and the column coordinate (COLUMN%) by 2.

#### **BASIC** listing: DVIB.B

```
110 +\ddot{\phantom{0}}D V I B
120 **----------------------
                                                                              -1---------------
130 ** Task : Demonstrates direct access to video RAM<br>150 ** Author : MICHAEL TISCHER<br>160 ** Developed on : 10/01/1988
                                                                               \star\ddot{\bullet}÷.
170 * Last update : 06/21/1989
                                                                               \star .
190 '200 CLS : KEY OFF
210 GOSUB 50000
                                    'Determine segment address of video RAM
220 COLUMN$=22 : CLINE$=0 : COL$ = 15
230 T$ = "DIVB - (c) 1988 by MICHAEL TISCHER" : GOSUB 51000
240 FCOL& = 0 : T$ = "[[[["<br>
240 FCOL& = 0 : T$ = "[[[["<br>
250 A$ = INKEY$ : IF A$<>" THEN 400 'Repeat until user presses a key<br>
260 FCOL& = FCOL& + 1 'Increment starting color<br>
270 IF FCOL& > 15 THEN FCOL& = 1 'When FCOL& 
                                                 'Set color for first square
280 COL\frac{1}{2} = FCOL\frac{1}{2}290 FOR COLUMN$=0 TO 76 STEP 4
                                                     'Execute for each column
300 FOR 2%=1 TO 24 STEP 2
                                                        'Execute for each line
```

```
310 CLlNEt - U: GOSUB 51000 'Display first line of square 
320 CLINEt - Zt+1 GOSUB 51000 'Display second line 
330 COLt - COLt + 1 AND 15 'Set next color 
340 NEXT 
350 NEXT 
360 GOTO 250 
370 '<br>400 CLS
                                                                               'Clear screen
410 END<br>460 ·
460 ' 50000 1*_••••••_••••__ •••••• _--•••• __ ••••••••_--••••• _-_ ••••***********. 
50010 '* Determine segment address of video RAM *' 
50020 ,*--------------------------------------------------------------" 50030 '* Input : none " 
50040 " Output: VR is the segment address of video RAM 
50050 .•••••••_••••••••••••••••••_••••••••••••••••••••••••••*.-......_.' 
50060 '<br>50070 DEF SEG = £H40
                                          50070 DEF SEC - GH40 'Segment address of BIOS variable range 
50080 VR = PEEK(&H63) + PEEK(&H64) * 256
50090 IF VR = \epsilonH3B4 THEN VR = \epsilonHBOOO ELSE VR = \epsilonHB800 50100 RETURN
                                                                           'Back to caller
50120 ' 
51000 ••••••••••••••••••••••_••••_-_••••••••••••••••••••••••***._.__._.' 
51010 " Write string direct into video RAM " 
 51020 "--------------------------------------------------------------" 
51030 ,* Input - COLUMNt - the output column 
 51040 * - CLINEs = the output line \star,
 51050 - COLt - string color 
51060 - TS - the string to be displayed 
                                                                                            \star .
51070 Output: none 51080 1***.**••••••*••••••••••••••••••••••••*****•••*••••••••••••••••••. 
51090 ' 
51100 DEF SEC - GH40 'Segment address of BIOS variable range 
51110 OF% = PEEK(&H4E) + PEEK(&H4F) * 256 'Starting address of page
51120 OFt = OFt + COLUMN' * 2 + CLlNEt * 160 'Offset of first character 
                                              Set segment address of video RAM<br>Execute string
51140 FOR I<sup>*</sup>=1 TO LEN(T$) FIRE UP TO LEN USE TO PORT ONE OF A ASCILLENTIAN TO PORT OF A ASCILLENT TO PORT THE SCILLENT TO UP THE SCILLEN
51150 POKE OF', ASC(MIDS(TS,I',1)) 'ASCII code in video RAM<br>51160 POKE OF'+1, COL<sup>1</sup><br>51170 OF': ext offset to next character<br>51170 OF': ext offset to next character
51180 NEXT<br>51190 RETURN
                                                                           'Back to caller
51200 '
```