### Chapter 1

## Complete I/O Port List

Here is some public domain information on I/O Ports. Many of the devices mentioned here are not installed on the Eos systems. Other devices (like the floppy) are probably not of interest. Information on EISA systems has been removed since Eos systems do not have an EISA bus (instead, they have PCI).

The original authors give us this warning:

Do *not* consider this information as complete and accurate. If you want to do hardware programming check *always* the appropriate data sheets. Be aware that erroneously programming can put your hardware or your data at risk.

Some terminalogy used here is different than in the rest of this documentation. In particular, these authors use PIC (Programable Interrupt Controller) to refer to what the rest of this documents calls the ICU (Interrupt Control Unit). When in doubt, the chip numbers are the best name and you should be encouraged to use the chip numbers because it makes you sound really knowledgable.

0000-001-01       0H 1 (first Direct Manory Access controller 8237)					bit $7-6 = 00$ demand mode
<ul> <li>MA channel 0 address jurgesset tealect</li> <li>MA channel 0 address jurgesset tealect</li> <li>MA channel 1 address jurgesset tealect</li> <li>MA channel 1 address jurgesset tealect</li> <li>MA channel 1 address jurgesset tealect</li> <li>MA channel 2 address jurgesset tealect</li> <li>MA channel 2 address jurgesset tealect</li> <li>MA channel 2 address jurgesset</li>     &lt;</ul>					= 01 single mode
0000       r/w       DMA channel 0 address byte 0, then byte 1.       bit 5 = 0 address increant select         0001       r/w       DMA channel 1 address byte 0, then byte 1.       bit 3 = 2 o0 verify operation         0004       r/w       DMA channel 2 address byte 0, then byte 1.       bit 3 = 1 oread from senory         0005       r/w       DMA channel 2 address byte 0, then byte 1.       bit 7 = 0 channel 0 select         0006       r/w       DMA channel 2 address byte 0, then byte 1.       bit 7 = 0 channel 0 select         0006       r/w       DMA channel 2 request       bit 7 = 0 channel 1 select         0008       r       DMA channel 2 request       0000 v       DMA channel 2 request         0008       r       DMA channel 0 request       0000 v       DMA channel 0 request         0008       r       DMA channel 0 request       0000 v       DMA channel 0 request         0008       r       DMA channel 0 request       0000 v       DMA channel 0 request         0008       v       DMA channel 0 request       0000 v       DMA channel 0 request         0008       v       DMA channel 0 request       0000 v       DMA channel 0 request         0008       v       DMA channel 0 request       0000 v       DMA channel 0 request         0010	0000-0	01F	DMA 1 (first Direct Memory Access controller 8237)		= 10 block mode
0001       r/v       DMA channel 0 word count tyte 0, then byte 1.       = 1 address decrement select         0002       r/v       DMA channel 1 word count tyte 0, then byte 1.       = 01 write oreservic         0005       r/v       DMA channel 2 word count byte 0, then byte 1.       = 01 write oreservic         0006       r/v       DMA channel 2 word count byte 0, then byte 1.       = 01 write oreservic         0006       r/v       DMA channel 2 word count byte 0, then byte 1.       = 01 channel 1 select         0007       r/v       DMA channel 3 word count byte 0, then byte 1.       = 01 channel 1 select         0007       r/v       DMA channel 3 word count byte 0, then byte 1.       = 01 channel 1 select         0007       r/v       DMA channel 3 word count byte 0, then byte 1.       = 01 channel 1 select         0007       r/v       DMA channel 0 request       0000 r       DMA read temporary register         bit 6 = 1 channel 2 request       0000 r       DMA read temporary register       = 11 channel 3 word count on channel 3         0008       w       DMA channel 0 -3 command register       0000 r       DMA read temporary register         0017       DMA channel 0 -3 command register       0000 r       DMA read temporary register         0018       w       DMA channel 0 -3 command register       0010 r					= 11 cascade mode
0002       r/v       DMA channel 1 address byte 0, then byte 1.       bit 3-2 = 00 verity operation         0004       r/v       DMA channel 2 address byte 0, then byte 1.       - 01 vriet on secory         0005       r/v       DMA channel 2 address byte 0, then byte 1.       - 01 vriet on secory         0006       r/v       DMA channel 3 address byte 0, then byte 1.       - 01 channel 1 select         0007       r/v       DMA channel 0-3 status register       - 01 channel 1 select         0008       r       DMA channel 3 request       0000 v       DMA channel 3 select         0015       the channel 1 request       0000 v       DMA channel 2 select       - 10 channel register         0008       r       DMA channel 0-3 status register       0000 v       DMA read temporary register         0015       tit 3 = 1 channel terminal count on channel 3       0000 v       DMA read temporary register         0016       u       DMA channel 0-3 command register	0000	r/w	DMA channel 0 address byte 0, then byte 1.		bit 5 = 0 address increment select
0003       r/v       DMA channel 1 word count byte 0, then byte 1.       = 01 words of the secty         0006       r/v       DMA channel 2 word count byte 0, then byte 1.       = 01 cad from secty         0006       r/v       DMA channel 3 word count byte 0, then byte 1.       = 01 cad from secty         0007       r/v       DMA channel 3 word count byte 0, then byte 1.       = 01 cad from secty         0008       r       DMA channel 0-3 status register       = 01 channel 1 select         0008       r       DMA channel 0-3 status register       = 01 channel 1 select         0015       r 1 channel 1 verd count on channel 2       DOD0       w       DMA relater byte pointer flip-flop         015       r 1 channel terminal count on channel 2       DOD0       w       DMA relater byte pointer flip-flop         015       r 1 channel terminal count on channel 2       DOD0       w       DMA relater byte pointer flip-flop         015       r 1 channel terminal count on channel 2       DOD0       w       DMA relater byte pointer flip-flop         015       r 1 channel terminal count on channel 2       DOD0       w       DMA relater byte pointer flip-flop         015       r 1 channel terminal count on channel 2       DOD0       w       DMA relater byte pointer flip-flop         015       r 1 channel termi	0001	r/w	DMA channel 0 word count byte 0, then byte 1.		= 1 address decrement select
0004       r/v       DMA channel 2 vord count byte 0, then byte 1.       = 10 read from memory         0005       r/v       DMA channel 3 vord count byte 0, then byte 1.       = 11 reserved         0006       r/v       DMA channel 3 vord count byte 0, then byte 1.       = 11 reserved         0007       r/v       DMA channel 3 vord count byte 0, then byte 1.       = 11 reserved         0008       r       DMA channel 3 vord count byte 0, then byte 1.       = 10 reserved         0008       r       DMA channel 3 vord count byte 0, then byte 1.       = 10 reserved         0008       r       DMA channel 3 vord count byte 0, then byte 1.       = 10 reserved         0008       r       DMA channel 3 vord count byte 0, then byte 1.       = 10 reserved         0008       r       DMA channel 1 vord count o channel 3       0000 r       DMA reserved         0000       r       DMA reserved       0000 r       DMA reserved         0001       r       DMA reserved       0000 r       DMA reserved         0002       v       DMA reserved       0000 r       DMA reserved         0003       r       DMA reserved       0000 r       DMA reserved         0004       r       DMA reserved       0000 r       DMA reserved         000	0002	r/w	DMA channel 1 address byte 0, then byte 1.		bit 3-2 = 00 verify operation
0005       r/w       PMA channel 2 vord court byte 0, then byte 1.       = 11 reserved         0007       r/w       PMA channel 3 ødres byte 0, then byte 1.       = 01 channel 0 select         0008       r       PMA channel 0 - 3 status register       = 01 channel 1 select         0018       r       PMA channel 0 - 3 status register       = 01 channel 2 select         0017       r/w       PMA channel 0 - 3 status register       = 0000 r         0018       r       PMA channel 0 - 3 status register       = 0000 r         0015       r 1 channel 1 request       0000 r       PMA claar mask register         0015       r 1 channel 1 request       0000 r       PMA claar mask register         0015       r 1 channel torninal count on channel 1       0000 r       PMA rite mask register         0015       r 1 channel torninal count on channel 1       0000 r       PMA rite mask register         0016       r 1       PMA channel 0 - 3 command register       0000 r       PMA rite mask register         0018       r 1       PMA channel 0 - 3 command register       0000 r       PMA rite mask register         0018       r 0       PMA channel 0 - 3 command register       0000 r       PIC 1 (Programmable Interrupt Controller 8259)         0018       r 0 fixed priority       r 0 fixe	0003	r/w	DMA channel 1 word count byte 0, then byte 1.		= 01 write to memory
0000       r/w       DMA channel 3 address byte 0, then byte 1.       bit 1-0 = 00 channel 0 select         0007       r/w       DMA channel 3 address byte 0, then byte 1.       = 01 channel 1 select         0008       r       DMA channel 0-3 status register       = 01 channel 1 select         0008       r       DMA channel 0-3 status register       = 00 channel 1 select         0010       r       DMA channel 3 address byte 0, then byte 1.       = 01 channel 1 select         0008       r       DMA channel 0-3 status register       0000 r       DMA channel 1 select         0011       channel 1 request       0000 r       DMA channel 1 select       = 01 channel 1 request         0008       v       DMA channel 1 request       0000 r       DMA channel register       = 000000000000000000000000000000000000	0004	r/w	DMA channel 2 address byte 0, then byte 1.		= 10 read from memory
<pre>0007 r/w DMA channel 3 word count byte 0, then byte 1. 0008 r DMA channel 0-3 status register 0007 v DMA channel 1 - channel 3 request 0000 v DMA master clear 0000 v DMA clear mask register 0010 v DMA clear mask register 0020-0037 PIC 1 (Programmable Interrupt Controller 8259) 0000 v DMA channel 0-3 command register 001 v DMA channel 0-3 command register 0010 v DMA channel 0-3 command register 0010 v DMA channel 0-3 command register 001 to vite selection 001 to vite selection 001 v DMA vite regist riggered mode 1 level triggered mode 1 level triggered mode 0 lit 3 - 0 edge triggered mode 1 level triggered mode</pre>	0005	r/w	DMA channel 2 word count byte 0, then byte 1.		= 11 reserved
<ul> <li>10 channel 2 select</li> <li>11 channel 3 select</li> <li>12 channel 1 sequest</li> <li>13 channel 1 sequest</li> <li>14 channel 0 select</li> <li>15 channel 1 sequest</li> <li>16 channel 1 sequest</li> <li>17 channel 1 sequest</li> <li>18 channel 1 sequest</li> <li>19 Channel 1 select</li> <li>10 channel 2 select</li> <li>11 channel 1 sequest</li> <li>11 channel 1 sequest</li> <li>12 channel terminal count on channel 3</li> <li>13 channel terminal count on channel 1</li> <li>14 channel 0 section channel 0</li> <li>11 channel terminal count on channel 1</li> <li>11 channel terminal count on channel 1</li> <li>11 channel terminal count on channel 1</li> <li>11 channel terminal count on channel 0</li> <li>11 channel terminal count on channel 1</li> <li>11 channel terminal count on channel 1</li> <li>11 channel terminal count on channel 0</li> <li>11 channel terminal count on channel 1</li> <li>11 channel terminal count on channel 0</li> <li>11 channel terminal count on channel 0</li> <li>11 channel terminal count on channel 1</li> <li>11 channel terminal count on channel 0</li> <li>11 channel terminal terminal count on channel 0</li> <li>11 contrast terminal terminal tendet</li> <li>11 contra</li></ul>	0006	r/w	DMA channel 3 address byte 0, then byte 1.		bit 1-0 = 00 channel 0 select
<ul> <li>10 channel 2 select</li> <li>11 channel 3 select</li> <li>12 channel 1 select</li> <li>13 channel 1 select</li> <li>14 class type pointer flip-flop</li> <li>15 channel 1 select</li> <li>15 channel 1 select</li> <li>16 channel 1 select</li> <li>17 channel 1 select</li> <li>10 channel 2 select</li> <li>11 channel 1 select</li> <li>12 channel trequest</li> <li>0000 v</li> <li>10 MA neter Class</li> <li>11 channel treminal count on channel 1</li> <li>11 channel treminal count on channel 1</li></ul>	0007	r/w	DMA channel 3 word count byte 0, then byte 1.		= 01 channel 1 select
<pre>bit 7 = 1 channel 3 request bit 6 = 1 channel 1 request bit 4 = 1 channel 1 request bit 3 = 1 channel t erminal count on channel 3 bit 2 = 1 channel terminal count on channel 2 bit 1 = 1 channel terminal count on channel 2 bit 2 = 1 channel terminal count on channel 2 bit 1 = 1 channel terminal count on channel 2 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 bACK sense active high e 0 DACK sense active high bit 5 = 1 extended write selection bit 4 = 1 rotating priority e 0 late write selection bit 2 = 1 extended write selection bit 2 = 1 extended write selection bit 2 = 1 extended tring bit 2 = 1 enable controller e 0 enable memory-to-memory 0009 w DMA vrite request register bit 7-3 = 0 reserved bit 7-3 = 0 reserved bit 7-3 = 0 reserved bit 7-3 = 0 reserved bit 7-3 = 0 channel 0 select = 1 channel 1 select 0021 w PIC Intialization command yord IGW1 bit 3 = 1 compressed timing e 1 channel terminal count on the priority bit 2 = 0 channel 0 select = 1 IGW2 interrupt vectors use 8 bytes e 1 IGW2 interrupt vectors use 4 bytes bit 7-3 = 0 reserved bit 7-0 = 0 share active high e 1 channel 1 select 0021 w PIC IGW2, IGW3, IGW4 after IGW1 to 0020 interrupt pin e 1 channel 1 select 0021 w PIC IGW2, IGW3 interrupt vectors active address for PIC bit 7-0 = 0 share controller not attached to corresponding interrupt pin e 1 channel 1 select 0021 w processed tring e 1 channel 1 select 0022 bit 7-0 = 0 share controller attached to corresponding interrupt pin e 1 channel 1 select 0022 bit 7-0 = 0 share controller attached to corresponding interrupt pin 0023 bit 2</pre>					= 10 channel 2 select
<pre>bit 7 = 1 channel 3 request bit 6 = 1 channel 1 request bit 5 = 1 channel 1 request bit 3 = 1 channel terminal count on channel 3 bit 2 = 1 channel terminal count on channel 2 bit 1 = 1 channel terminal count on channel 2 bit 0 = 1 channel terminal count on channel 2 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 bACK sense active high = 0 late write selection = 0 late write selection = 0 late write selection = 0 late write selection = 0 interrupt vectors use 1 bit 1 = 0 cascade mode = 1 single mode, no TGW ineeded = 1 i Single mode, no TGW ineeded = 1 i GW2: bit 7-3 = 0 reserved bit 7-3 = 0 reserved bit 7-3 = 0 reserved bit 7-3 = 0 reserved bit 7-3 = 0 cear mask bit = 1 coulchannel 0 select = 0 channel 0 select = 0 channel 1 select</pre>	0008	r	DMA channel 0-3 status register		= 11 channel 3 select
<pre>bit 6 = 1 channel 2 request 000C v DMA clear byte pointer flip-flop bit 4 = 1 channel 1 terminal count on channel 3 000C v DMA measter clear 000D v DMA measter clear 000D v DMA measter clear 000E v DMA measter clear 000E v DMA clear mask register 000F v DMA vrite register 000F v DMA vrite register 000F v DMA vrite register 0020-003F FIC 1 (Programmable Interrupt Controller 8259) 0008 v DMA clear mask register 0000F v DMA vrite register 0000 v DMA vrite register 0020-003F FIC 1 (Programmable Interrupt Controller 8259) 0008 v DMA clear mask register 0000F v DMA vrite register 0 DACK sense active high 0000 v DMA vrite register 0 DACK sense active high 0000 = 0 DACK sense active low 0000 = 0 normal timing 0000 = 0 normal timing 0000 = 0 normal timing 0000 = 0 normal timing 0000 = 0 enable sensery-to-meenry 0000 = v DMA vrite request register 0000 r/D DMA clear 0 select 0000 r/D DMA vrite request bit 1 set mask controller attached to corresponding 1 neterrupt pin 1 set we controller attached to corresponding 1 neterrupt pin 1 set we controller attached to corresponding 1 neterrupt pin 1 set mask bit 1 se</pre>					
<pre>bit 5 = 1 channel 1 request bit 4 = 1 channel terminal count on channel 3 bit 2 = 1 channel terminal count on channel 3 bit 2 = 1 channel terminal count on channel 2 bit 1 = 1 channel terminal count on channel 2 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 bit 7 = 0 noty used in 80/85 mode bit 4 = 1 rotating priority bit 3 = 1 compressed tring priority bit 3 = 1 compressed tring priority bit 1 = 1 cotating priority bit 2 = 1 enable meory-to-memory 0000 v DMA write request register bit 7 = 0 enable meory-to-memory 0000 v DMA write request register bit 7 = 0 reserved bit 7 = 0 reserved bit 7 = 0 clear mask bit bit 1 =</pre>				000C w	DMA clear byte pointer flip-flop
<ul> <li>bit 4 = 1 channel 0 request</li> <li>bit 3 = 1 channel terminal count on channel 3</li> <li>bit 2 = 1 channel terminal count on channel 2</li> <li>bit 2 = 1 channel terminal count on channel 2</li> <li>bit 1 = 1 channel terminal count on channel 1</li> <li>bit 0 = 1 channel terminal count on channel 0</li> <li>0006 w DMA write mask register</li> <li>bit 7 = 1 DACK sense active high         <ul> <li>0 DACK sense active high</li> <li>0 DACK sense active low</li> <li>0 ODE 1 we closed write selection</li> <li>1 low triggered mode</li> <li>1 low triggered mode</li></ul></li></ul>				000D r	
<ul> <li>bit 3 = 1 channel terminal count on channel 3 bit 2 = 1 channel terminal count on channel 2 bit 1 = 1 channel terminal count on channel 2 bit 1 = 1 channel terminal count on channel 1 bit 0 = 1 channel terminal count on channel 0</li> <li>0006 w DMA write mask register</li> <li>0007 w DMA write mask register</li> <li>0008 w DMA channel 0 - 3 command register</li> <li>0010 w PIC initialization command word ICW1 bit 7 = 1 DACK sense active high = 0 DAECK sense active low bit 6 = 1 DREU sense active high = 0 DREU sense active low bit 5 = 1 extended write selection = 0 late write selection = 0 late write selection = 0 interrupt vectors use 4 bytes = 1 successive interrupt vectors use 8 bytes = 1 successive interrupt vectors use 8 bytes = 1 successive interrupt vectors use 8 bytes = 1 successive interrupt vectors use 4 bytes = 1 Single mode, no ICW3 needed = 1 ICW4 needed = 1 ICW4 needed = 1 ICW4 needed = 1 ICW4 needed = 1 Single mode, no ICW3 needed = 1 Single mode, no ICW3 needed = 1 Single mode, no ICW4 needed = 1 Single mode hor LOW1 to 0020 ICW2: bit 7-3 = or ceserved bit 2 - 0 reserved bit 2 - 0 reserved = 1 set mask bit = 1 set mask bit = 0 richannel 1 select</li> </ul>					
<pre>bit 2 = 1 channel terminal count on channel 2 bit 1 = 1 channel terminal count on channel 1 bit 0 = 1 channel terminal count on channel 0 bit 0 = 1 channel terminal count on channel 0 0008 v DMA channel 0-3 command register bit 7 = 1 DACK sense active high 0008 v DMA channel 0-3 command register 0008 v DMA channel 0-3 command register 0 DACK sense active high 0 D DREQ sense active high 0 a D DREQ sense active high 0 a D DREQ sense active low 0 bit 5 = 1 extended write selection 0 a D BREQ sense active low 0 bit 5 = 1 extended write selection 0 a Date write selection 0 a Date priority 0 a O fixed priority 0 a O mormal timing 0 a D and timing 0 a D mail timing 0 a normal tiselet 0 a normal tiselet 0 a no</pre>					
<pre>bit 1 = 1 channel terminal count on channel 1 bit 0 = 1 channel terminal count on channel 0 0008 w DMA channel 0-3 command register bit 7 = 1 DACK sense active high = 0 DACK sense active low bit 6 = 1 DREQ sense active low bit 6 = 1 DREQ sense active low bit 5 = 1 extended write selection = 0 late write selection = 0 late write selection bit 2 = 1 concreasive interrupt vectors use 8 bytes = 0 fixed priority = 0 enable memory-to-memory 0009 w DMA write request register bit 7 = 0 or reserved bit 2 = 0 successive interrupt vectors use 8 bytes = 0 enable memory-to-memory 0001 w DMA write request register bit 2 = 0 reserved bit 2 = 0 clear mask bit = 1 set mask</pre>					
<pre>bit 0 = 1 channel terminal count on channel 0 0008 v DMA channel 0-3 command register bit 7 = 1 DACK sense active high 0020 v PIC initialization command word ICW1 0020 v PIC initialization command word ICW1 0020 v PIC initialization command word ICW1 0020 v PIC initialization command word ICW1 bit 6 = 1 DREQ sense active high 0 DREQ sense active low bit 5 = 1 extended write selection 0 DREQ sense active low bit 5 = 1 extended write selection 0 DREQ sense active low bit 4 = 1 ICW1 is being issued 1 avel triggered mode 1 avel triggered mode 1 avecessive interrupt vectors use 8 bytes 1 avecessive interrupt vectors use 8 bytes 1 avecessive interrupt vectors use 8 bytes 1 avecessive interrupt vectors use 4 bytes 1 avecessive interupt vectors use 4 bytes 1 avecessive intervector of a</pre>				0001 W	Dik witte mask fegister
0008       w       DMC channel 0-3 command register       0020-003F       PIC 1       (Programmable Interrupt Controller 8259)         0008       w       DMC kannel 0-3 command register       0020       w       PIC initialization command word ICW1         008       w       DACK sense active high       0020       w       PIC initialization command word ICW1         008       w       DACK sense active high       bit 7-5 = 0       only used in 80/85 mode         008       w       DIEQ sense active high       bit 7-5 = 0       only used in 80/85 mode         008       w       DIEQ sense active high       bit 7-5 = 0       only used in 80/85 mode         009       w       DREQ sense active low       bit 3 = 0       edge triggered mode         0       DIEQ restricts priority       bit 3 = 1       cencessive interrupt vectors use 8 bytes         0       onranal timing       = 1       successive interrupt vectors use 4 bytes         0       normal timing       = 1       cascade mode         0       normal timing       = 1       cascade mode         0010       w       DMA write request register       DIC 10W2, ICW3, ICW4 after ICW1 to 0020         0010       w       DMA write request register       DIC 7-0       DI save controller not at					
0008       w       DMA channel 0-3 command register         bit 7 = 1       DACK sense active high = 0       0020       w       PIC initialization command word ICW1 bit 7-5 = 0       only used in 80/85 mode bit 7-0 = 0       interrup in interrup pin       interrup pin         0000A       r/w       DMA vrite request register bit 7-3 = 0       r/w       DMA vrite request interrup to corresponding interrupt pin			bit 0 - 1 channel terminal count on channel 0	0020-003F	PIC 1 (Programmable Interrupt Controller 8259)
bit 7 = 1 DACK sense active high = 0 DACK sense active high = 0 DEEQ sense active high = 0 DEEQ sense active low bit 6 = 1 DEEQ sense active low = 0 late write selection = 0 late write selection = 0 late write selection = 0 fixed priority = 0 fixed priority = 0 fixed priority = 0 is compressed timing = 0 normal timing bit 2 = 1 enable controller = 0 enable memory-to-memory 0009 v DMA write request register 0000 r/w DMA channel 0-3 mask register bit 7 = 0 conserved bit 1 = 0 conserved bit 1 = 0 conserved bit 2 = 0 successive interrupt vectors use 4 bytes = 1 set mask bit = 0 reserved bit 2 = 1 enable controller = 0 enable memory-to-memory 0001 v DMA channel 0-3 mask register bit 1 = 0 conserved bit 1 = 0 conserved bit 1 = 0 controller conserved bit 1 = 0 controller controller = 0 reserved bit 2 = 0 slave controller not attached to corresponding = 1 set mask bit = 1 set mask bit = 1 set mask bit = 0 channel 0 select = 0 channel 0 select = 0 channel 0 select = 0 channel 1 select = 0	0008	W	DMA channel 0-3 command register		
<pre></pre>				0020 w	PIC initialization command word ICW1
<ul> <li>9 DREQ sense active lov</li> <li>bit 5 = 1 extended write selection</li> <li>bit 5 = 1 extended write selection</li> <li>a late write selection</li> <li>bit 4 = 1 rotating priority</li> <li>bit 4 = 1 rotating priority</li> <li>bit 3 = 1 evel triggered mode</li> <li>a low cessive interrupt vectors use 8 bytes</li> <li>a low cessive interrupt vectors use 4 bytes</li> <li>b low cessive interrupt vectors use 4 bytes</li> <li>a low cessive interrupt vectors use 4 bytes</li> <li>a low controller</li> <li>a low controller</li> <li>b low cessive interrupt vectors</li> <li>a low controller not attached to corresponding interrupt pin</li> <li>a low controller attached to corresponding interrupt pin</li> </ul>					bit 7-5 = 0 only used in 80/85 mode
<pre>bit 5 = 1 extended write selection = 0 late write selection = 0 late write selection = 0 fixed priority = 0 fixed priority</pre>			bit 6 = 1 DREQ sense active high		bit 4 = 1 ICW1 is being issued
<pre>bit 5 = 1 extended write selection</pre>			= 0 DREQ sense active low		bit 3 = 0 edge triggered mode
<pre></pre>			bit 5 = 1 extended write selection		
<pre>bit 4 = 1 rotating priority = 0 fixed priority = 0 fixed priority = 0 fixed priority = 0 fixed priority = 0 cascade mode = 1 single mode, no ICW3 needed = 1 single mode, no ICW3 needed = 1 ICW4 needed</pre>			= 0 late write selection		
<ul> <li>= 0 fixed priority</li> <li>bit 3 = 1 compressed timing</li> <li>= 0 normal timing</li> <li>bit 2 = 1 enable controller</li> <li>= 0 enable memory-to-memory</li> <li>0009 w</li> <li>0004 r/w</li> <li>DMA write request register</li> <li>0 reserved</li> <li>bit 7-3 = 0 reserved</li> <li>bit 7-3 = 0 reserved</li> <li>bit 2 = 0 clear mask bit</li> <li>= 1 set mask bit</li> </ul>			bit 4 = 1 rotating priority		
<pre>bit 3 = 1 compresed timing = 0 normal timing bit 0 = 0 no TGW3 needed = 1 CGW4 needed = 1 CGW4 needed = 0 no TGW4 needed = 1 CGW4 needed = 1 CGW4 needed = 0 no TGW4 needed = 1 CGW4 needed = 1 SeW4 needed = 1 CGW4 needed = 1 SeW4 need</pre>					
<ul> <li>= 0 normal timing</li> <li>bit 0 = 0 no TWA needed</li> <li>= 0 enable memory-to-memory</li> <li>0009 w</li> <li>DMA write request register</li> <li>0000 r/w</li> <li>DMA channel 0-3 mask register</li> <li>bit 7-3 = 0 reserved</li> <li>bit 7-3 = 0 reserved</li> <li>bit 2 = 0 claar mask bit</li> <li>= 1 set mask bit</li> <li>= 1 set mask bit</li> <li>= 0 no TWA</li> <li>bit 10 = 0 no TWA</li> <li>bit 0 = 0 no TWA</li> <li>DMA channel 10-3 mask register</li> <li>bit 7-3 = 0 reserved</li> <li>bit 7-3 = 0 reserved</li> <li>bit 7-0 = 0 slave controller not attached to corresponding interrupt pin</li> <li>= 0 channel 1 select</li> </ul>					
bi 2 = 1 enable controller = 0 enable memory-to-memory 0009 w DMA write request register 0004 r/w DMA channel 0-3 mask register bit 7-3 = 0 reserved bit 2 = 0 clear mask bit = 1 set mask bit = 1 set mask bit = 0 channel 0 select = 01 ICW2 = 1 ICW2 icW3, ICW4 after ICW1 to 0020 ICW2: bit 2-0 reserved ICW3: bit 2-0 reserved bit 2 = 0 clear mask bit = 1 slave controller not attached to corresponding interrupt pin = 1 slave controller attached to corresponding interrupt pin					
0009     w     DMA write request register     001     w     PIC     ICW2; ICW3, ICW4 after ICW1 to 0020       0000     r/w     DMA write request register     ICW2;       0000     r/w     DMA channel 0-3 mask register     bit 7-3 = address lines A0-A3 of base vector address for PIC       0010     bit 7-3 = 0     reserved     ICW3;       0010     w     PIC     ICW2;       0010     w     PIC     ICW3;       0100     w     PIC     ICW3;       0100     w     PIC <td></td> <td></td> <td></td> <td></td> <td></td>					
0009     w     DMA write request register     0021     w     PIC     IGW2, IGW3, IGW4 after IGW1 to 0020       0009     w     DMA write request register     bit 7-3 = address lines A0-A3 of base vector address for PIC       0000     r/w     DMA channel 0-3 mask register     bit 2-0 = reserved       bit 7-3 = 0     reserved     IGW3:       bit 2 = 0     clear mask bit     bit 7-0 = 0     slave controller not attached to corresponding interrupt pin       = 1     set mask bit     = 1     slave controller attached to corresponding interrupt pin       = 01     channel 1 select     = 1     slave controller attached to corresponding interrupt pin					1 1001 100404
0009     w     DMA write request register     ICW2:       000A     r/w     DMA channel 0-3 mask register     bit 7-3 = address lines A0-A3 of base vector address for PIC       000A     r/w     DMA channel 0-3 mask register     bit 2-0 = reserved       bit 7-3 = 0     reserved     ICW3:       1     set mask bit     bit 7-0 = 0 slave controller not attached to corresponding interrupt pin       bit 1-0 = 00     channel 0 select     = 1 slave controller attached to corresponding interrupt pin			o chabic memory of memory	0021 ₩	PIC ICW2 ICW3 ICW4 after ICW1 to 0020
000A       r/w       DMA channel 0-3 mask register       bit 7-3 = address lines A0-A3 of base vector address for PIC         000A       r/w       DMA channel 0-3 mask register       bit 2-0 = reserved         bit 7-3 = 0       reserved       Dit 2-0 = reserved         bit 2 = 0       clear mask bit       Dit 7-0 = 0         = 1       set mask bit       bit 7-0 = 0         = 1       set mask bit       bit 7-0 = 0         = 01       channel 1 select       interrupt pin	0009	17	DMA write request register		
000A     r/w     DMA channel 0-3 mask register     bit 2-0 = reserved       bit 7-3 = 0     reserved     ICW3:       bit 2     0     clear mask bit     bit 70=0     slave controller not attached to corresponding interrupt pin       = 1     set mask bit     = 1     slave controller attached to corresponding interrupt pin       = 0     channel 0 select     = 1     slave controller attached to corresponding interrupt pin	0000		pun wiite iedress iePisesi		
bit 7-3 = 0 reserved ICW3: bit 2 = 0 clear mask bit = 1 set mask bit bit 1-0 = 0 clearnel 0 select = 1 slave controller not attached to corresponding = 01 channel 1 select = 1 slave controller attached to corresponding interrupt pin	0004	r/11	DMA channel 0=3 mask register		
bit 2     = 0     clear mask bit     bit 7-0 = 0     slave controller not attached to corresponding interrupt pin       bit 1-0 = 00     channel 0 select     = 1     slave controller attached to corresponding interrupt pin       = 01     channel 1 select     interrupt pin	OUUA	1/*			
= 1 set mask bit interrupt pin bit 1-0 = 00 channel 0 select = 1 slave controller attached to corresponding = 01 channel 1 select interrupt pin					
bit 1-0 = 00 channel 0 select = 1 slave controller attached to corresponding = 01 channel 1 select interrupt pin					
= 01 channel 1 select interrupt pin					
			= 10 channel 2 select		ICW4:
= 10 channel 2 select Luw: = 11 channel 3 select bit 7-5 = 0 reserved					
			= 11 channel 3 select		
bit 4 = 0 no special fully-nested mode	0000		DMA shares 1 0 2 mode manister		
	0008	w	DMA channel 0-3 mode register		= 1 special fully-nested mode
000B w DMA channel 0-3 mode register = 1 special fully-nested mode	0005	-			- Sportar rarry monoral mono

0021 r/w 0020 r	<pre>bit 3-2 = 0x nonbuffered mode = 10 buffered mode/master bit 1 = 0 normal EDI = 1 Auto EDI bit 0 = 0 8085 mode = 1 8086/8088 mode PIC master interrupt mask register OCW1: bit 7 = 0 enable parallel printer interrupt bit 6 = 0 enable fixed disk interrupt bit 5 = 0 enable fixed disk interrupt bit 4 = 0 enable serial port 1 interrupt bit 2 = 0 enable serial port 2 interrupt bit 2 = 0 enable video interrupt bit 1 = 0 enable keyboard, mouse, RTC interrupt bit 0 = 0 enable timer interrupt</pre>		05h 64K 06h 128K 07h 256K 08h 512K 09h 11M 04h 24 05h 4M 07h 8M 07h 18M 07h 18M 07h 46 Configuration Register 0 format: bit 0 "NGO" first 64K of each 1M noncacheable in real/V86 bit 1 "NGO" first 64K of each 1M noncacheable in real/V86 bit 2 "A20M" enables A20M# input pin bit 3 "KEN" enables KEN# input pin bit 3 "KEN" enables KEN# input pin bit 4 "FLUSH" enables KEN# input pin bit 5 "BARB" enables internal cache flushing on bus holds bit 6 "O" cache direct-mapped instead of 2-way associative
	request register: bit 7-0 = 0 no active request for the corresponding int. line = 1 active request for corresponding interrupt line in-service register: bit 7-0 = 0 corresponding line not currently being serviced = 1 corresponding int. line currently being serviced		bit 7 "SUSPEND" enables SUSP# input and SUSPA# output pins Configuration Register 1 format; bit 0 "RPL" enables output pins RPLSET and RPLVAL#
0020 w	OCW2: bit 7-5 = 000 rotate in auto EOI mode (clear) = 001 nonspecific EOI = 010 no operation = 011 specific EOI	0026 w 0027 r/w	Power Management index for data port power management data
	<ul> <li>= 100 rotate in auto EDI mode (set)</li> <li>= 101 rotate on nonspecific EDI command</li> <li>= 110 set priority command</li> <li>= 111 rotate on specific EDI command</li> <li>bit 4 = 0 reserved</li> <li>bit 3 = 0 reserved</li> <li>bit 2 - 0 interrupt request to which the command applies</li> </ul>	0040-005F 0040 r/w 0041 r/w 0042 r/w	PIT (Programmable Interrupt Timer 8253, 8254) XT & AT uses 40-43 PS/2 uses 40, 42, 43, 44, 47 PIT counter 0, counter divisor (XT, AT, PS/2) PIT counter 1, RAM refresh counter (XT, AT) PIT counter 2, cassette & speaker (XT, AT, PS/2)
	PIC OCW3 Dit 7 = 0 reserved Dit 6-5 = 0x no operation = 10 reset special mask = 11 set special mask Dit 4 = 0 reserved Dit 2 = 0 no poll command = 1 poll command Dit 1-0 = 0x no operation = 10 read int.request register on next read at 0020 = 11 read int.in-service register on next read 0020	0043 r/w	<pre>PIT mode port, control word register for counters 0-2 bit 7-6 = 00 counter 0 select = 01 counter 1 select (not PS/2) = 10 counter 1 select bit 5-4 = 00 counter 2 select bit 5-4 = 00 counter latch command = 01 read/write counter bits 0-7 only = 10 read/write counter bits 0-7 first, then 8-15 bit 3-1 = 000 mode 0 select = 001 mode 1 select - programmable one shot = x11 mode 3 select - aquare wave generator = 100 mode 4 select - software triggered strobe = 101 mode 5 select - hardware triggered strobe bit 0 = 0 binary counter 16 bits = 1 BCD counter</pre>
0022 002B	<ul> <li>Intel 82355, part of chipset for 386sx initialisation in POST will disable these addresses, only a hard reset will enable them again.</li> <li>82335 MCR memory configuration register</li> </ul>	0044 r/w	PIT counter 3 (PS/2, EISA) used as fail-safe timer. generates an NMI on time out. for user generated NMI see at 0462.
0024 0026 0028 0028	82335 RC1 roll compare register 82335 RC2 roll compare register 82335 RC0 compare register 82335 CC1 compare register values for CC0 and CC1: 00F9,0000 enable range compare CC0 0-512K CC1 disable 00F1,0000 enable range compare CC0 0-1024K CC1 disable 00F1,10F9 enable range compare CC0 0-1M CC1 1M-1M5 00E1,0000 enable range compare CC0 0-2M CC1 disable 00E1,0000 enable range compare CC0 0-2M CC1 disable 00E1,0000 enable range compare CC0 0-2M CC1 disable 00E1,0000 enable range compare CC0 0-4M CC1 disable 00E1,40E1 enable range compare CC0 0-4M CC1 disable	0047 w 0048 0049 0048 0049	<pre>PIT control word register counter 3 (PS/2, EISA) bit 7-6 = 00 counter 3 select = 01 reserved = 10 reserved = 11 reserved bit 5-4 = 00 counter latch command counter 3 = 01 read/write counter bits 0-7 only = 1x reserved bit 3-0 = 00 EISA 8254 timer 2, not used (counter 1) EISA programmable interval timer 2 EISA programmable interval timer 2</pre>
0022-0023	- Chip Set Data		Keyboard controller 804x (8041, 8042) (or PPI (8255) on PC,XT)
	index for accesses to data port chip set data		XT uses 60-63, AT uses 60-64 AT keyboard controller input port bit definitions bit 7 = 0 keyboard inhibited
0022-0023 0022 w 0023 r/w	<ul> <li>Cyrix Cx486SLC/DLC processor Cache Configuration Registers index for accesses to next port COh CR0 CIh CR1 C4h non-cacheable region 1, start address bits 31-24 C5h non-cacheable region 1, start address bits 23-16 C6h non-cacheable region 2, start address bits 31-24 C8h non-cacheable region 2, start address bits 31-24 C8h non-cacheable region 2, start address bits 31-24 C8h non-cacheable region 3, start address bits 31-24 C8h non-cacheable region 4, start address bits 31-24 C9h non-cacheable region 4, start address 515 C9h non-cacheable region</li></ul>		<pre>bit 6 = 0 CGA, else MDA bit 5 = 0 manufacturing jumper installed bit 4 = 0 system RAM 512K, else 640K bit 3-0 reserved AT keyboard controller input port bit definitions by Compaq bit 7 = 0 security lock is locked bit 6 = 0 Compaq dual-scan display, 1=non-Compaq display bit 5 = 0 system board dip switch 5 is ON bit 4 = 0 auto speed selected, 1=high speed selected bit 3 = 0 slow (4HE2), 1 = fast (8HH2) bit 2 = 0 80287 installed, 1= no NDP installed bit 1=0 reserved AT keyboard controller output port bit definitions bit 7 = keyboard data output bit 5 = 0 input buffer full bit 4 = 0 output buffer mpty bit 3 = reserved (see note) bit 2 = reserved (see note) bit 1 = gate A20 bit 0 = system reset Note: bits 2 and 3 are the turbo speed switch or password lock on Award/AMI/Phoenix BIOSes. These bits make</pre>

		use of nonstandard keyboard controller BIOS functionality to manipulate			bit $5-4 = 00$ reserved = 01 40*25 color (mono mode)
		pin 23 (8041 port 22) as turbo switch for AWARD pin 35 (8041 port 15) as turbo switch/pw lock for			= 10 80*25 color (mono mode) = 11 MDA 80*25
		Phoenix			bit 3-2 = 00 256K (using 256K chips)
0060	r/w	KB controller data port or keyboard input buffer (ISA, EISA)			= 01 512K (using 256K chips) = 10 576K (using 256K chips)
		should only be read from after status port bit0 = 1			= 11 640K (using 256K chips)
		should only be written to if status port bit1 = 0 keyboard commands (data also goes to port 0060):			bit 3-2 = 00 64K (using 64K chips) = 01 128K (using 64K chips)
		E6 sngl set mouse scaling to 1:1 E7 sngl set mouse scaling to 2:1			= 10 192K (using 64K chips) = 11 256K (using 64K chips)
		E7 Shgi set mouse scaling to 2:1 E8 dbl set mouse resolution			bit 1-0 reserved
		(00h = 1/mm,01h = 2/mm,02h = 4/mm,03h = 8/mm) E9 sngl get mouse information	0064	r	KB controller read status (ISA, EISA)
		read two status bytes:	0004	1	bit 7 = 1 parity error on transmission from keyboard
		byte 0 bit 7 unused			bit 6 = 1 receive timeout bit 5 = 1 transmit timeout
		bit 6 remote rather than stream mode			bit 4 = 0 keyboard inhibit
		bit 5 mouse enabled bit 4 scaling set to 2:1			<pre>bit 3 = 1 data in input register is command 0 data in input register is data</pre>
		bit 3 unused			bit 2 system flag status: 0=power up or reset 1=selftest OK
		bit 2 left button pressed bit 1 unused			<pre>bit 1 = 1 input buffer full (input 60/64 has data for 8042) bit 0 = 1 output buffer full (output 60 has data for system)</pre>
		bit 0 right button pressed byte 1: resolution	0064	r	KB controller read status (MCA)
		ED dbl set/reset mode indicators Caps Num Scrl	0004	1	bit 7 = 1 parity error on transmission from keyboard
		bit 2 = CapsLk, bit 1 = NumLk, bit 0 = ScrlLk EE sngl diagnostic echo. returns EE.			<pre>bit 6 = 1 general timeout bit 5 = 1 mouse output buffer full</pre>
		EF sngl NOP (No OPeration). reserved for future use			bit 4 = 0 keyboard inhibit
		F0 dbl get/set scan code set 00h get current set			<pre>bit 3 = 1 data in input register is command 0 data in input register is data</pre>
		01h scancode set 1 (except Type 2 ctrlr)			bit 2 system flag status: 0=power up or reset 1=selftest OK
		02h scancode set 2 (default) 03h scancode set 3			<pre>bit 1 = 1 input buffer full (input 60/64 has data for 804x) bit 0 = 1 output buffer full (output 60 has data for system)</pre>
		F2 sngl read keyboard ID (read two ID bytes)	0064		
		F2 sngl read mouse ID (read two ID bytes) F3 dbl set typematic rate/delay	0064	r	KB controller read status by Compaq bit 7 = 1 parity error detected (11-bit format only). If an
		F3 db1 set mouse sample rate in reports per second F4 sng1 enable keyboard			error is detected, a Resend command is sent to the keyboard once only, as an attempt to recover.
		F4 sngl enable mouse			bit 6 = 1 receive timeout. transmission didn't finish in 2mS.
		F5 sngl disable keyboard. set default parameters F5 sngl disable mouse, set default parameters			<pre>bit 5 = 1 transmission timeout error bit 5,6,7 cause</pre>
		F6 sngl set default parameters			1 0 0 No clock
		F7 sngl [MCA] set all keys to typematic (scancode set 3) F8 sngl [MCA] set all keys to make/release			1 1 0 Clock OK, no response 1 0 1 Clock OK, parity error
		F9 sngl [MCA] set all keys to make only			bit 4 = 0 security lock engaged
		FA sngl [MCA] set all keys to typematic/make/release FB sngl [MCA] set al keys to typematic			<pre>bit 3 = 1 data in OUTPUT register is command 0 data in OUTPUT register is data</pre>
		FC dbl [MCA] set specific key to make/release FD dbl [MCA] set specific key to make only			<pre>bit 2 system flag status: 0=power up or reset 1=soft reset bit 1 = 1 input buffer full (output 60/64 has data)</pre>
		FE sngl resend last scancode			
					bit 0 = 0 no new data in buffer (input 60 has data)
		FF sngl perform internal power-on reset function FF sngl reset mouse	0064	w	bit 0 = 0 no new data in buffer (input 60 has data) KB controller input buffer (ISA, EISA)
		FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access	0064	w	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060):
		FF sngl perform internal power-on reset function FF sngl reset mouse	0064	W	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x
0060	r	FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions	0064	w	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060
0060	r	FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT)	0064	W	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved
0060 0061	r	FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092)	0064	w	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure:
		FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset )	0064	W	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure:     bit 7 reserved     bit 6 = 1 convert KB codes to 8066 scan codes     bit 5 = 0 use 11-bit codes, 1=use 8086 codes     bit 4 = 0 enable keyboard, 1=disable keyboard</pre>
		FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255	0064	W	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structures bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes</pre>
		FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1 = IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 1 parity check enable	0064	w	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure:     bit 7 reserved     bit 6 = 1 convert KB codes to 8086 scan codes     bit 5 = 0 use 11-bit codes, 1=use 8086 codes     bit 4 = 0 enable keyboard, 1=use 8086 codes     bit 3 = 1 ignore security lock state     bit 2 this bit goes into bit2 status reg.     bit 1 = 0 reserved</pre>
		<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable</pre>	0064	w	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, l=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of</pre>
0061	W	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 1 = 1 speaker data enable bit 0 = 1 timer 2 gate to speaker enable</pre>	0064	W	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM
		<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset) bit 3= 1 channel check enable bit 3 = 1 parity check enable bit 1 = 1 speaker data enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B (ISA, EISA) KB controller port B control register (ISA, EISA) system control port for compatibility with 8255</pre>	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8066 scan codes bit 5 = 0 use 11-bit codes, l=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of</pre>
0061	W	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 2 = 1 parity check enable bit 2 = 1 speaker data enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check cocurred</pre>	0064	ũ	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F db1 writes the data byte to the address specified in the 5 lower bits of the command.</pre>
0061	W	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check controller of the system control port B control port B control port B control bit 6 channel check occurred bit 6 channel check occurred bit 6 mirrors timer 2 output condition</pre>	0064	ũ	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 0 = 1 censerved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved</pre>
0061	W	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check refresh request bit 4 toggles with each refresh request bit 3 = 1 channel check status</pre>	0064	ŭ	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use il-bit codes, I=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit6 = IBM PC mode</pre>
0061	W	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 2 = 1 parity check enable bit 2 = 1 is peaker data enable bit 0 = 1 timer 2 gate to speaker enable kE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check occurred bit 4 toggles with each refresh request bit 3 channel check status bit 2 parity check status</pre>	0064	ŭ	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 1EMP FC compatibility mode bit6 = IEM FC compatibility mode bit6 = IEM FC mode</pre>
0061	W	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check refresh request bit 4 toggles with each refresh request bit 3 = 1 channel check status</pre>	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit4 = disable kb bit3 = inhibit override bit3 = inhibit override bit3 = inhibit override</pre>
0061	W	FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 (second to a second	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = IBM PC mode bit3 = inhibit override bit2 = system flag bit1 = 0 reserved</pre>
0061	r	FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 (reserved bit 0 = 1 timer 2 gate to speaker enable bit 0 = 1 parity check courred bit 6 channel check occurred bit 6 channel check scrured bit 3 channel check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control per ti	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 1EM PC mode bit6 = IEM PC compatibility mode bit5 = IBM PC mode bit3 = inhibit override bit3 = inhibit override bit1 = 0 reserved bit1 = 0 reserved bit0 = enableoutput buffer full interrupt</pre>
0061	r	<pre>FF ssgl perform internal power-on reset function FF sngl reset mouse Note: must issue command DAh to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check status bit 1 speaker data status bit 2 speaker data status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 7 = 1 clear Keyboard bit 6 o hold keyboard check low</pre>	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = IBM PC mode bit3 = inhibit override bit2 = system flag bit1 = 0 reserved</pre>
0061	r	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 6255 bit 7 (i= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check courred bit 5 mirrors timer 2 output condition bit 4 toggles with each refresh request bit 1 = parity check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 6 = 0 hold keyboard bit 6 = 0 hold keyboard bit 6 = 0 I/O check enable</pre>	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8066 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 1 ignors security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F db1 writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC mode bit5 = IBM PC mode bit2 = system flag bit1 = 0 reserved bit0 = enableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) Al Compaq uhknown speedfunction ?? bit Compaq uhknown speedfunction ??</pre>
0061	r	<pre>FF ssgl perform internal power-on reset function FF sngl reset mouse Note: must issue command DAh to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check status bit 1 speaker data status bit 2 speaker data status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 7 = 1 clear Keyboard bit 6 o hold keyboard check low</pre>	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit 6 = IBM PC compatibility mode bit5 = IBM PC mode bit2 = system flag bit1 = 0 reserved bit0 = enableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) A1 Compaq unknown speedfunction ??</pre>
0061	r	<pre>FF sogl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PPI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 5 ending check status bit 2 parity check status bit 2 parity check status bit 1 speaker data status bit 1 speaker data status bit 1 speaker data status bit 1 chear keyboard bit 5 = 0 hold keyboard chock low bit 5 = 0 hold keyboard chock enable bit 3 = 0 reset yed, often used as turbo switch </pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, I=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = inhibit override bit2 = system flag bit1 = 0 reserved bit2 = enableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) Al Compaq mknown speedfunction ?? A2 Compaq Enable system speed control A4 MCA check if password installed A4 Compaq Toggle speed
0061	r	<pre>FF ssgl perform internal power-on reset function FF sngl reset mouse Note: must issue command DAh to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 2 = 1 parity check enable bit 2 = 1 arity check enable bit 0 = 1 timer 2 gate to speaker enable bit 0 = 1 timer 2 gate to speaker enable bit 6 channel check occurred bit 6 channel check scatus bit 1 speaker data tentus bit 2 toggles with each refresh request bit 3 channel check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 7 = 1 clear keyboard bit 5 = 0 I/O check enable bit 3 = 0 read low switches</pre>	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 3 = 1 ignors security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit 7 = 0 reserved bit 8 = IBM PC compatibility mode bits = IBM PC conde bit 2 = system flag bit 1 = 0 reserved bit 0 = nableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) AL Compaq unknown speedfunction ?? A2 Compaq Load new command (60 to [64], command to [60]) AL Compaq inspective specified in a AL Compad function ?? A3 Compad I cod new command (ba to ba command to [60]) AL Compad is system speed control AL AC check if password installed AL Compad Specified read. the 8042 places the real values</pre>
0061	r	<pre>FF sngl perform internal power-on reset function FF sngl reset mouse Note: must issue command DAh to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check courred bit 6 channel check occurred bit 6 channel check occurred bit 3 channel check status bit 1 speaker data status bit 2 parity check status bit 2 parity check status bit 2 parity check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 5 = 0 I/O check enable bit 4 = 0 AM parity check enable bit 5 = 0 read low switches bit 2 = 0 read low switches bit 3 = 0 read low switches bit 4 = 1 pareved, for used as turbo switch bit 4 = 1 speaker data enable</pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = i convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 3 = 1 ignore security lock state bit 0 = i convert KB codes in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit 0 = IBM PC compatibility mode bit3 = inhibit override bit2 = system flag bit1 = 0 reserved bit3 = inhibit override bit2 = eastPed control A MCA check if password installed A Compaq Togge speed A Compaq Togge speed
0061	Ŧ	<pre>FF ssgl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PFI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check courred bit 6 channel check status bit 1 speaker data status bit 2 parity check status bit 2 parity check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PFI Programmable Peripheral Interface 8255 (XT only) system control port bit 5 = 0 hold keyboard clock low bit 5 = 0 hold keyboard bit 3 = 0 read low switches bit 2 reserved, often used as turbo switch bit 1 = 1 papaker data enable bit 2 = 1 apaker data enable bit 3 = 0 read low switches bit 2 reserved, often used as turbo switch bit 1 = 1 papaker data enable bit 2 = 1 reserved, often used as turbo switch bit 1 = 1 papaker data enable bit 2 = 1 reserved, often used as turbo switch bit 0 = 1 timer 2 gate to speaker enable bit 0 = 1 timer 2 reserved reserved bit 0 = 1 timer 2 reserved reserved bit 0 = 1 reserved reserved bit 0 = 1 timer 2 reserved reserved reserved reserved bit 0 = 1 timer 2 reserved r</pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use i1-bit codes, 1=use 8086 codes bit 5 = 0 use i1-bit codes, 1=use 8086 codes bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 6 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = IBM PC mode bit4 = disable kb bit3 = inhibit override bit2 = system flag bit1 = 0 reserved bit0 = neableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) Al Compaq unknown speedfunction ?? Al Compaq unknown speedfunction ?? Al Compaq Endle system speed control Al MCA check if password installed AL Compaq Toggle speed AL Compaq Special reed. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer. No output buffer full is generated.
0061	Ŧ	<pre>FF sol perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 6255 bit 7 (i= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 6255 bit 7 parity check enable bit 6 = channel check ecured bit 5 mirrors timer 2 output condition bit 4 toggles with each refresh request bit 1 channel check status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 7 = 1 clear Keyboard bit 4 = 0 RAM parity check enable bit 4 = 0 FAM parity check enable bit 2 reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 2 reserved, status bit 2 nearly check enable bit 4 = 0 FAM parity check enable bit 4 = 0 FAM parity check enable bit 4 = 0 FAM parity check enable bit 2 reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 2 reserved, often used as turbo switch bit 2 reserved, often used as turbo switch bit 2 timer 2 gate to speaker enable bit 2 timer 2 gate to speaker enable bit 2 reserved, often used as turbo switch bit 5 = 1 funcer 2 gate to speaker enable bit 0 = 1 timer 2 gate to speaker enable</pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8066 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 1 ignors security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F db1 writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = IBM PC mode bit2 = system flag bit1 = 0 reserved bit0 = enableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) 11 Compaq unknown speedfunction ?? 13 Compaq Load new command (60 to [64], command to [60]) 14 Compaq unknown speedfunction ?? 15 Compaq Special read. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer routput four for using 15 Compaq Special read. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer.
0061	Ŧ	<pre>FF sugl perform internal power-on reset function FF sugl reset mouse Note: must issue command DAh to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check status bit 1 speaker data status bit 2 parity check status bit 2 parity check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 3 = 0 read low switches bit 3 = 0 read low switches bit 2 = 1 timer 2 gate to speaker enable bit 4 = 1 speaker data enable bit 4 = 1 reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 4 = 1 reserved, often used as turbo switch bit 5 = 1 I/O channel check bit 6 = 1 timer 2 channel out bit 6 = 1 timer 2 chan</pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit 7 = 0 reserved bit 2 = IBM PC compatibility mode bit3 = IBM PC mode bit3 = inbit override bit3 = inbit to verride bit3 = inbit override bit3 = inbit of the full interrupt 60 Compaq Load new command (60 to [64], command to [60]) 11 Compaq unknown speedfunction ?? 22 Compaq unknown speedfunction ?? 33 Compaq Enable system speed control 44 MCA check if password installed 45 Compaq Special reed, the 8042 places the real values of port 2 except for bits 4 and 5 with are given a new definition in the output buffer. No output buffer full is generated. if bit 5 = 0, a 9-bit keyboard is in use if bit 4 = 0, outp-buff-full interrupt isabled
0061	Ŧ	<pre>FF sogl perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KB controller data output buffer (via PFI on XT) KB controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check bit 0 = 1 timer 2 gate to speaker enable KB controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check ecurred bit 1 speaker data status bit 1 speaker data status bit 2 parity check status bit 2 parity check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 4 = 0 AAM parity check enable bit 3 = 0 read low switches bit 2 = reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 2 = 1 timer 2 gate to speaker enable bit 3 = 0 read low switches bit 2 = reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 2 = 1 timer 2 gate to speaker enable bit 2 = 1 timer 2 reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 0 = 1 timer 2 are to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 timer 2 is to speaker enable bit 0 = 1 time</pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 3 = 1 ignore security 10ck state bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = IBM PC mode bit2 = system flag bit1 = 0 reserved bit0 = easeleoutput buffer full interrupt 50 Compaq Load new command (60 to [64], command to [60]) A1 Compaq unknown speedfunction ?? 23 Compaq conduct system speed control A4 MCA check if password installed A5 MCA load password A5 Compaq Special read. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer. No output buffer full is generate. if bit 5 = 1, an 11-bit koyboard is in use if bit 4 = 0, outp-buffer-full interrupt disabled if bit 4 = 1, output-buffer-full interrupt disabled if bit 4 = 0, outp-buffer-full interrupt disabled if bit 4 = 1, output-buffer-full interrupt disabled
0061	Ŧ	<pre>FF sol perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 6255 bit 7 (i= IRQ 0 reset) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 6255 bit 7 parity check enable bit 6 = 0 channel check occurred bit 5 mirrors timer 2 output condition bit 4 toggles with each refresh request bit 0 timer 2 gate to speaker status bit 0 timer 2 gate to speaker status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 6255 (XT only) system control port bit 7 = 1 clear Keyboard bit 4 = 0 RAM parity check enable bit 2 reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 2 reserved, often used as turbo switch bit 2 reserved, often used as turbo switch bit 7 = 1 timer 2 gate to speaker enable PPI (XT only) bit 7 = 1 RAM parity check bit 5 = 1 timer 2 channel out bit 4 = 1 system board RAM size type 2 bit 2 = 1 system board RAM size type 2 bit 2 = 1 system board RAM size type 2 bit 2 = 1 system board RAM size type 2 bit 1 = 1 coprocessor installed</pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8066 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 1 ignors security 10ck state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F db1 writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC code bit5 = IBM PC mode bit2 = system flag bit1 = 0 reserved bit0 = enableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) 11 Compaq unknown speedfunction ?? 13 Compaq Load new command (60 to [64], command to [60]) 14 Compaq unknown speedfunction ?? 15 Compaq Special read. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer routput buffer full is generated. if bit 5 = 1, an 11-bit keyboard is in use if bit 5 = 1, an 9-bit keyboard is in use if bit 5 = 1, an 11-bit keyboard is in use if bit 5 = 1, an 11-bit keyboard is in use if bit 4 = 1, output-buffer-full interrupt disabled if bit 4 = 1, output-buffer-full interrupt disable
0061	u F v	<pre>FF smgl perform internal power-on reset function FF smgl reset mouse Note: must issue command DAh to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 6 channel check status bit 1 speaker data status bit 2 parity check status bit 2 parity check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 7 = 1 clear Keyboard bit 3 = 0 read low switches bit 2 = 1 reserved, often used as turbo switch bit 1 = speaker data enable bit 2 = 1 timer 2 gate to speaker enable bit 3 = 0 read low switches bit 4 to 7 = 1 timer 2 gate to speaker enable bit 5 = 1 if or channel check enable bit 4 = 1 system board RAM size type 1 bit 6 = 1 1/0 channel check bit 6 = 1 1/0 channel check bit 6 = 1 system board RAM size type 1 bit 3 = 1 system board RAM size type 2 bit 1 = 1 coprocessor installed bit 0 = 1 loop in POST</pre>	0064	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 4 = 0 enable keyboard, 1=disable keyboard bit 3 = 1 ignore security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit0 = IBM PC compatibility mode bit2 = system flag bit1 = 0 reserved bit2 = system flag bit1 = 0 reserved bit2 = oreased control A Compaq unknown speedfunction ?? A Compaq unknown speedfunction ?? A Compaq index ordinatalled A Compaq Toggle system speed control A MCA check if password installed A Compaq Toggle speed A Ca load password A Ca load password A Ca load password A Compaq Special reed. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer. No output buffer full is generated. if bit 5 = 1, an 11-bit keyboard is in use if bit 4 = 1, output-buffer-full interrupt lisaled if bit 4 = 1, output-buffer-full interrupt A Ca check apsasyord A Ca check apsasyord A Ca check password A Ca check password A Ca check password A Ca check password A Ca check apsasword A Ca check apsasword A Ca check apsasword A Ca check password A Ca check password A Ca check password A Ca check password A Ca check apsasword A Ca check apsasword A Ca check apsasword A Ca check apsasword A Ca check password A Ca check apsasword A Ca</pre>
0061	Ŧ	<pre>FF sol perform internal power-on reset function FF sngl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 6255 bit 7 (i= IRQ 0 reset) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 6255 bit 7 parity check enable bit 6 = 0 channel check occurred bit 5 mirrors timer 2 output condition bit 4 toggles with each refresh request bit 0 timer 2 gate to speaker status bit 0 timer 2 gate to speaker status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 6255 (XT only) system control port bit 7 = 1 clear Keyboard bit 4 = 0 RAM parity check enable bit 2 reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 2 reserved, often used as turbo switch bit 2 reserved, often used as turbo switch bit 7 = 1 timer 2 gate to speaker enable PPI (XT only) bit 7 = 1 RAM parity check bit 5 = 1 timer 2 channel out bit 4 = 1 system board RAM size type 2 bit 2 = 1 system board RAM size type 2 bit 2 = 1 system board RAM size type 2 bit 2 = 1 system board RAM size type 2 bit 1 = 1 coprocessor installed</pre>	0064	v	KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 3 = 1 ignore security 10cK state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = IBM PC mode bit2 = system flag bit1 = 0 reserved bit0 = neableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) A1 Compaq unknown speedfunction ?? A3 Compaq Toggle speed A5 MCA check if password installed A4 Compaq Toggle speed A5 MCA check if password installed A5 Compaq Special read. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer. No output buffer full is generated. If bit 5 = 0, a 9-bit keyboard is in use if bit 4 = 1, output-buffer-full interrupt disabled if bit 4 = 1, output-
0061	u F v	<pre>FF sugl perform internal power-on reset function FF sugl reset mouse Note: must issue command D4h to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PFI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (i= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B ortor or register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check enable bit 6 = 0 hold keyboard bit 1 = 1 speaker data enable bit 2 parity check status bit 0 timer 2 gate to speaker status PFI Programmable Peripheral Interface 8255 (XT only) system control port bit 3 = 1 channel check nable bit 4 = 0 RAM parity check enable bit 2 reserved, often used as turbo switch bit 1 = 1 speaker data enable bit 2 reserved, often used as turbo switch bit 3 = 1 timer 2 gate to speaker enable PFI (XT only) Not 7 = 1 RAM parity check bit 5 = 1 timer 2 channel out bit 5 = 1 loop in POST PFI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PFI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PFI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PFI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PFI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PFI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PFI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST</pre>	0054	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8066 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 5 = 1 ignors security lock state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM FC compatibility mode bit6 = IBM FC code bit2 = system flag bit1 = 0 reserved bit0 = enableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) A M CA check if password installed A Compaq Toggle speed bit 5 = 0.0000 A CA check if password is 4 and 5 wich are given a new definition in the output buffer. No output buffer full is generated. if bit 5 = 0, a 9-bit keyboard is in use if bit 5 = 1, an 11-bit keyboard is in use if bit 4 = 1, output-buffer-full interrupt disabled if bit 4 = 1,</pre>
0061	u F v	<pre>FF smgl perform internal power-on reset function FF smgl reset mouse Note: must issue command DAh to port 64h first to access mouse functions KeyBoard or KE controller data output buffer (via PPI on XT) KE controller port B (ISA, EISA) (PS/2 port A is at 0092) system control port for compatibility with 8255 bit 7 (1= IRQ 0 reset ) bit 6-4 reserved bit 3 = 1 channel check enable bit 2 = 1 parity check enable bit 0 = 1 timer 2 gate to speaker enable KE controller port B control register (ISA, EISA) system control port for compatibility with 8255 bit 7 parity check occurred bit 6 channel check occurred bit 1 engles with each refresh request bit 2 parity check status bit 1 speaker data status bit 0 timer 2 gate to speaker status PPI Programmable Peripheral Interface 8255 (XT only) system control port bit 4 - Clear keyboard bit 5 = 0 Hold keyboard clock low bit 5 = 0 I/O check enable bit 2 = 1 speaker data enable bit 0 = 1 timer 2 gate to speaker enable PPI (XT only) bit 7 = 1 system board RLM size type 1 bit 3 = 1 system board RLM size type 2 bit 1 = 1 coprocessor installed bit 0 = 1 loop in POST PPI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PPI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PPI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PPI (XT only) command mode register (read dipswitches) bit 0 = 1 loop in POST PPI (XT only) command mode register (read dipswitches)</pre>	0054	v	<pre>KB controller input buffer (ISA, EISA) KB controller commands (data goes to port 0060): 20 read read byte zero of internal RAM, this is the last KB command send to 804x Compaq Put current command byte on port 0060 command structure: bit 7 reserved bit 6 = 1 convert KB codes to 8086 scan codes bit 5 = 0 use 11-bit codes, 1=use 8086 codes bit 3 = 1 ignore security 10ck state bit 2 this bit goes into bit2 status reg. bit 1 = 0 reserved bit 0 = 1 generate int. when output buffer full 21-3F read reads the byte specified in the lower 5 bits of the command in the 804x's internal RAM 60-7F dbl writes the data byte to the address specified in the 5 lower bits of the command. Alternate description KB IO command 60 summary: bit7 = 0 reserved bit6 = IBM PC compatibility mode bit5 = IBM PC mode bit2 = system flag bit1 = 0 reserved bit0 = enableoutput buffer full interrupt 60 Compaq Load new command (60 to [64], command to [60]) A1 Compaq unknown speedfunction ?? A2 Compaq unknown speedfunction ?? A3 Compaq Conde system speed control A4 MCA check if password installed A5 MCA load password A5 Compaq Special read. the 8042 places the real values of port 2 except for bits 4 and 5 wich are given a new definition in the output buffer. No output buffer full is generated. if bit 5 = 1, an 11-bit keyboard is in use if bit 4 = 1, output-buffer-full interrupt disabled if bit 4 = 0, cutp-buffer-full interrupt disabled if bit 4 = 0, outp-buffer-full interrupt disabled if bit 4 = 1, output-buffer-full interrupt disabled if bit 4 = 0, outp-buffer-full interrupt disabled if bit 4 = 0</pre>

		AB sngl	<pre>initiate interface test. result values: 0 = no error</pre>
			1 = keyboard clock line stuck low 2 = keyboard clock line stuck high
			3 = keyboard data line is stuck low 4 = keyboard data line stuck high
		Compaq AC read	
			output port, input port, status word are send. disable keyboard (sets bit 4 of commmand byte)
		AE sngl	enable keyboard (resets bit 4 of command byte)
			Enhanced Command: read keyboard version read input port
			Places status of input port in output buffer. use
		C1 MCA	this command only when the output buffer is empty Enhanced Command: poll input port Low nibble
		C2 MCA	Enhanced Command: poll input port High nibble
			read output port Places byte in output port in output buffer. use
		D1 db1	this command only when the output buffer is empty write output port. next byte written to 0060
			will be written to the 804x output port; the original IBM AT and many compatibles use bit 1 of
		Compag	the output port to control the A20 gate. The system speed bits are not set by this command
		compaq	use commands A1-A6 (!) for speed functions.
		D2 MCA D3 MCA	Enhanced Command: write keyboard output buffer Enhanced Command: write pointing device out.buf.
		D4 MCA	write to mouse
			Enhanced Command: write to auxiliary device disable address line A20 (HP Vectra only???) default in Real Mode
			enable address line A20 (HP Vectra only???)
			<pre>read test inputs. bit0 = kbd clock, bit1 = kbd data</pre>
			Enhanced Command: active output port
		ED Compaq	This is a two part command to control the state of the NumLock CpasLock and ScrollLock LEDs
			The second byte contains the state to set LEDs.
			<pre>bit 7-3 reserved. should be set to 0. bit 2 = 0 Caps Lock LED off</pre>
			<pre>bit 2 = 0 Caps Lock LED off bit 1 = 0 Num Lock LED off bit 0 = 0 Scroll Lock LED off</pre>
		FO-FF sngl	pulse output port low for 6 microseconds.
			bits 0-3 contain the mask for the bits to be pulsed. a bit is pulsed if its mask bit is zero.
			bit0=system reset. Don't set to zero. Pulse only!
general	note:		trollers are widely different from each other.
note on	Award	You cannot g	enerally exchange them between different machines. Award's Enhanced KB controller advertising sheet.
note on	Compaq:	Derived from	the Compaq Deskpro 386 Tech. Ref. Guide.
0065			
0005	r	communication	s port (Olivetti M24)
0068	w		
0068 0069		HP-Vectra co HP-Vectra SV	s port (Olivetti M24) ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done
0068 0069 006A	w r w	HP-Vectra co HP-Vectra SV HP-Vectra cl	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done
0068 0069	w r w	HP-Vectra co HP-Vectra SV HP-Vectra cl HP-HIL (Huma	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7)
0068 0069 006A 006C-006	w r w 6F	HP-Vectra co HP-Vectra SV HP-Vectra cl HP-HIL (Huma	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done
0068 0069 006A 006C-006	w r w 6F	HP-Vectra co HP-Vectra SV HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006	w r w 6F 7F	HP-Vectra co HP-Vectra SV HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006	w r w 6F 7F	HP-Vectra co HP-Vectra SV HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006	w r w 6F 7F	HP-Vectra co HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	w r w 6F 7F	HP-Vectra co HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM inde bit g 0 bit 6-0 any write to or the RTC wi	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) (Real Time Clock MC146818) x register port (ISA, EISA) NMI disabled NMI enabled CMOS RAM index (64 bytes, sometimes 128 bytes) 0070 should be followed by an action to 0071
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM inte bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra co HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM inde bit 7 = 0 o bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 0 current	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) (Real Time Clock MC146818) x register port (ISA, EISA) NMI disabled NMI enabled CMDS RAM index (64 bytes, sometimes 128 bytes) 0070 should be followed by an action to 0071 l be left in an unknown state. port (ISA, EISA) :
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra co HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/ARC CMOS RAM/ARC CMOS RAM/ARC i = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 01 alarm s 2 current	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMDS RAM/ATC CMDS RAM/ATC CMDS RAM/ATC Dit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMDS RAM data RTC registers 00 current cl alarm s 02 current 03 alarm s	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra I HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers Or current 01 alarm s 02 current 03 alarm h	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM/ATC CMOS RAM it bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current claarm s current 03 alarm m d current 06 day of	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current for current for current for current for day of 07 day of 07 day of 08 month i	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 01 alarm s 02 current 03 alarm h 06 day of 07 day of 07 day of 08 month i 09 year i 04 status	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM/ATC CMOS RAM data RTC registers 00 current cmOS RAM data RTC registers 00 current 01 alarm s 02 current 03 alarm f 04 day of 07 day of 08 month i 09 year i 0A status bit 7	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/ATC CMOS RAM/ATC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current for current for current for current for day of 07 day of 07 day of 08 month i 09 year i 04 status bit 7 bit 6-0	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra I HP-HIL (Huma CMOS RAM/ATC CMOS RAM/ATC CMOS RAM/ATC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 10 alarm s 02 current 03 alarm h 6 day of 07 day of 07 day of 08 month i 09 year i 0A status bit 7 bit 6- 0 05 ataus	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMDS RAM/ATC CMDS RAM/ATC CMDS RAM/ATC CMDS RAM data RTC registers 00 current 01 alarm s 02 current 03 alarm s 04 current 05 alarm h 06 day of 07 day of 08 month i 09 year i 0A status bit 7 bit 6- bit 3- 08 status bit 7	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra cl HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM/RTC CMOS RAM tata bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current cl alarm s 02 current 03 alarm s 04 current 05 alarm h 66 day of 07 day of 08 month i 09 year i 0A status bit 7 bit 6- bit 3- 0B status bit 7 bit 6	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vactra CO HP-Vactra SW HP-Vactra I HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 01 alarm s 02 current 01 alarm s 02 current 01 alarm s 04 current 05 alarm m 04 current 05 alarm fi 06 month i 09 year i 0A status bit 7 bit 3- 0B status bit 7 bit 6- bit 5	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vactra CO HP-Vactra SW HP-Vactra I HP-HIL (Huma CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 01 alarm s 02 current 03 alarm m 04 current 05 alarm h 06 day of 07 day of 08 smonth i 09 year i 09 year i 04 status bit 7 bit 6 bit 3 0B status bit 7 bit 6 bit 3 bit 6 bit 4 bit 3 bit 6 bit 4 bit 3 bit 6 bit 3 bit 6 bit 4 bit 3 bit 6 bit 3 bit 6 bit 4 bit 3 bit 6 bit 4 bit 4 bit 3 bit 6 bit 4 bit 3 bit 6 bit 4 bit 4 bit 4 bit 3 bit 6 bit 4 bit 4 b	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, dome n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra 1 HP-HIL (Huma CMOS RAM/ATC CMOS RAM/ATC CMOS RAM/ATC CMOS RAM/ATC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 01 alarm s 02 current 03 alarm m 04 current 05 alarm h 06 day of 07 day of 07 day of 07 day of 08 month i 09 year i 0A status bit 7 bit 6- bit 3 oB status bit 7 bit 6 bit 4 bit 3 bit 2	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, dome n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vactra CO HP-Vactra SW HP-Vactra I HP-HIL (Huma CMOS RAM/RTC CMOS RAM/RTC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 01 alarm s 02 current 01 alarm s 02 current 03 alarm m 04 current 05 alarm m 06 day of 07 day of 07 day of 08 month i 09 year i 0A status bit 7 bit 6- bit 3- 0B status bit 7 bit 3- bit 3 bit 2 bit 3 bit 2 bit 3 bit 2 bit 3 bit 3 bit 3 bit 2 bit 3 bit 3	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra 1 HP-HIL (Huma CMOS RAM/ATC CMOS RAM/ATC CMOS RAM/ATC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 1 alarm s 02 current 03 alarm h 6 day of 07 day of 07 day of 07 day of 08 month i 09 year i 04 status bit 7 bit 6- bit 3- 0B status bit 7 bit 6 bit 3 bit 2 bit 1	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra 1 HP-HIL (Huma CMOS RAM/ATC CMOS RAM/ATC CMOS RAM/ATC CMOS RAM inde bit 7 = 1 = 0 bit 6-0 any write to or the RTC wi CMOS RAM data RTC registers 00 current 1 alarm s 02 current 03 alarm h 6 day of 07 day of 07 day of 07 day of 08 month i 09 year i 04 status bit 7 bit 6- bit 3- 0B status bit 7 bit 6 bit 3 bit 2 bit 1	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, done n Interface Link = async. serial inputs 0-7) 
0068 0069 006A 006C-006  0070-007 0070	ч г ч 7F	HP-Vectra CO HP-Vectra SW HP-Vectra I HP-Vectra I HP-HIL (Huma CMOS RAM/ATC CMOS RAM/ATC CMOS RAM/ATC CMOS RAM data RTC registers 00 current I CMOS RAM data RTC registers 00 current I CMOS RAM data RTC registers 00 current I 04 current 05 alarm h 06 day of 07 day of 07 day of 08 month i 09 year i 00 status bit 7 bit 6- bit 3- 0B status bit 7 bit 6 bit 3 0D bit 1 bit 3 bit 2 bit 1 bit 0	ntrol buffer (HP commands) C (keyboard request SerViCe port) ear processing, dome n Interface Link = async. serial inputs 0-7) 

bit 7 = bit 6 = interrupt request flag interrupt request \_\_\_\_\_ peridoc interrupt flag

bit 4 = bit 3-0 update interrupt flag reserved OD status register D bit 7 = 1 Real-Time Clock has power bit 6-0 reserved diagnostics status byte 0E diagnostics status byte bit 7 = 0 RTC lost power bit 6 = 1 CMOS RAM checksum bad bit 5 = 1 invalid configuration information at POST bit 4 = 1 memory size error at POST bit 3 = 1 fixed disk/adapter failed initialization bit 2 = 1 CMOS RAM time found invalid bit 1 = 1 adapters do not match configuration (EISA) bit 0 = 1 time out reading an adapter ID (EISA) shutdown status byte 00 = normal execution of POST 01 = chip set initialization for real mode reentry 0F 01 = chip set initialization for real mode reer 04 = jump to bootstrap code 05 = issue an EDI an JMP to Dword ptr at 40:67 06 = JMP to Dword ptrv at 40:67 without EDI 07 = return to INTI5/87 (block move) 08 = return to INTI5/87 (block move) OA = JMP to Dword ptr at 40:67 without EOI OB = return IRETS through 40:67 08 = return IALIS through 40:67 diskette drive type for A: and B: bit 7-4 drive type of drive 0 bit 3-0 drive type of drive 1 = 0000 no drive = 0001 360K 10 = 0010 1M2 = 0011 720K = 0100 = 0100 1M44 = 0101-1111 reserved reserved / AMI Extended CMOS setup (AMI Hi-Flex BIOS) bit 7 = 1 Typematic Rate Programming bit 6-5 = 00 Typematic Rate Delay 250 mSec bit 4-0 = 00011 Typematic Rate 21.8 Chars/Sec fixed disk drive type for drive 0 and drive 1 bit 7-4 drive type of drive 0 bit 3-0 drive type of drive 1 if either of the inbles equals 0F, then bytes 19 an IA are valid reserved / AMI Extended CMOS setup (AMI Hi-Flex BIOS) bit 7 = 1 Mouse Support Option 1M44 11 12 13 reserved / AMI Extended CMOS setup (AMI Hi-Flex BIOS) bit 7 = 1 Mouse Support Option bit 6 = 1 Above 1 MB Memory Test disable bit 5 = 1 Memory Test Tick Sound disable bit 4 = 1 Memory Parity Error Check enable bit 3 = 1 Hit <ESC> Message Display disabled bit 2 = 1 Hit <ESC> Message Display disabled bit 1 = 1 Wait For <F1> If Any Error enabled bit 0 = 1 System Boot Up Num Lock is On equiument byte equipment byte bit 7-6 diskette drives installed = 00 1 drive installed = 01 2 drives installed 14 = 10 reserved = 10 reserved = 11 reserved bit 5-4 primary display = 00 adapter card with option ROM = 01 40\*25 color = 10 80\*25 color = 11 monochrome bit 3-2 reserved bit 1 = 1 coprocessor installed (non-Weitek) bit 0 diskette drive avaliable for boot LSB of systemn base memory in Kb LSB of systemn base memory in Kb MSB of systemn base memory in Kb LSB of total extended memory in Kb MSB of total extended memory in Kb drive C extension byte drive D extension byte 16 17 18 19 1 A 1B-27 reserved 1B/1C word to 82335 RC1 roll compare register at [24] (Phoenix) 1D/1E word to 82335 RC2 roll compare register at [26] (Phoenix) HP-Vectra checksum over 29-2D 28 29-2D reserved 29-20 reserved 29/2A word to Intel 82335 CCO compare register at [28](Phoenix) 2B/2C word send to 82335 CC1 compare register at [2A] (Phoenix) AMI Extended CMOS setup (AMI Hi-Flex BIOS) (Phoenix BIOS checks for the values AA or CC) bit 7 = 1 Weitek Processor Absent bit 6 = 1 Floppy Drive Seek At Boot disabled bit 5 = 1 System Boot Up Speed is high bit 3 = 1 Cache Memory enabled bit 2 = 1 Internal Cache Memory <1> bit 1-0 reserved CMOS LSE checksum over 10-2D CMOS LSE checksum over 10-2D (Phoenix) 2D 2E 2F CMOS LSB checksum over 10-2D LSB of extended memory found above 1Mb at POST date century in BCD 30 31 32 3 information flags bit4 = bit4 from CPU register CR0 (Phoenix) this bit is only known as INTEL RESERVED 34-3F reserved bit4 bit5 (Phoenix BIOS) 34 
 3D/3E word to 82335 MCR memory config register at [22](Phoenix)

 3D
 bit3
 base memsize 512/640 (Phoenix)

bit 5 =

alarm interrupt flag

4

		<pre>3E bit7 = 1 relocate enable (Phoenix) bit1 = 1 shadow video enable (Phoenix) bit0 = 1 shadow BIOS enable (Phoenix)</pre>			<pre>bit 3 = 1 terminal count on channel 7 bit 2 = 1 terminal count on channel 6 bit 1 = 1 terminal count on channel 5 bit 0 = 1 terminal count on channel 4</pre>
		User Definable Drive Parameters are also stored in CMOS RAM:	OODO	w	DMA channel 4-7 command register (ISA, EISA) bit 7 = 1 DACK sense active high
		AMI (386sx BIOS 1989) first user definable drive (type 47)			= 0 DACK sense active low
		1B L cylinders 1C H cylinders			<pre>bit 6 = 1 DREQ sense active high = 0 DREQ sense active low</pre>
		1D heads			bit 5 = 1 extended write selection
		1E L Write Precompensation Cylinder			= 0 late write selection
		1F H Write Precompensation Cylinder 20 ??			<pre>bit 4 = 1 rotating priority = 0 fixed priority</pre>
		21 L cylinders parking zone			bit 3 = 1 compressed timing
		22 H cylinders parking zone 23 sectors			= 0 normal timing bit 2 = 0 enable controller
		25 sectors			bit $2 = 0$ enable controller bit $1 = 1$ enable memory-to-memory transfer
		AMI (386sx BIOS 1989) second user definable drive (type 48)			bit 0
		24 L cylinders 25 H cylinders	00D2	w	DMA channel 4-7 write request register (ISA, EISA)
		26 heads	0052	-	
		27 L Write Precompensation Cylinder 28 H Write Precompensation Cylinder	00D4	W	DMA channel 4-7 write single mask register (ISA, EISA) bit 7-3 reserved
		29 ??			bit 2 = 0 clear mask bit
		2A L cylinders parking zone			= 1 set mask bit
		2B H cylinders parking zone 2C sectors			<pre>bit 1-0 = 00 channel 4 select = 01 channel 5 select</pre>
		20 3600013			= 10 channel 6 select
		Phoenix (386BIOS v1.10.03 1988) 1st user definable drv (type48)			= 11 channel 7 select
		20 L cylinders 21 H cylinders	00D6	w	DMA channel 4-7 mode register (ISA, EISA)
		22 heads			bit $7-6 = 00$ demand mode
		23 L Write Precompensation Cylinder			= 01 single mode = 10 block mode
		24 H Write Precompensation Cylinder 25 L cylinders parking zone			= 10 block mode = 11 cascade mode
		26 H cylinders parking zone			bit 5 = 0 address increment select
		27 sectors			<pre>= 1 address decrement select bit 4 = 0 autoinitialisation disable</pre>
		Phoenix (386BIOS v1.10.03 1988) 2nd user definable drv (type49)			= 1 autoinitialisation enable
		(when PS/2-style password option is not used)			bit 3-2 = 00 verify operation
		35 L cylinders 36 H cylinders			<pre>= 01 write to memory = 10 read from memory</pre>
		37 heads			= 11 reserved
		<ul><li>38 L Write Precompensation Cylinder</li><li>39 H Write Precompensation Cylinder</li></ul>			<pre>bit 1-0 = 00 channel 4 select = 01 channel 5 select</pre>
		34 L cylinders parking zone			= 10 channel 6 select
		3B H cylinders parking zone 3C sectors			= 11 channel 7 select
		SC Sectors	00D8	w	DMA channel 4-7 clear byte pointer flip-flop (ISA, EISA)
				r	DMA channel 4-7 read temporary register (ISA, EISA)
0080	W	Manufacturing Diagnostics port	00DA 00DC	w w	DMA channel 4-7 master clear (ISA, EISA) DMA channel 4-7 clear mask register (ISA, EISA)
			OODE	w	DMA channel 4-7 write mask register (ISA, EISA)
0080-0	008F	DMA page registers (74612)			
0080	r/w	extra page register (temporary storage)	00F0-0	0FF	coprocessor (808780387)
	r/w r/w	DMA channel 2 address byte 2 DMA channel 3 address byte 2	00F0	w	math coprocessor clear busy latch
0083	r/w	DMA channel 1 address byte 2	00F1	w	math coprocessor reset
0084	r/w	extra page register	00F8 00FA		opcode transfer
0085 0086	r/w r/w	extra page register extra page register		r/w r/w	opcode transfer opcode transfer
0087	r/w	DMA channel 0 address byte 2			-
0088 0089	r/w r/w	extra page register DMA channel 6 address byte 2			Adaptec 154xB/154xC SCSI adapter.
0089	r/w	DMA channel 7 address byte 2 DMA channel 7 address byte 2	0150 0	100	alternate address at 0134, 0230, 0234, 0330 and 0334
0089	r/w	DMA channel 5 address byte 2			
008C 008D	r/w r/w	extra page register extra page register			Adaptec 154xB/154xC SCSI adapter.
008E	r/w	extra page register			alternate address at 0130, 0230, 0234, 0330 and 0334
008F	r/w	DMA refresh page register			
			0140-0	14F	SCSI (alternate Small Computer System Interface) adapter
00A0-0	00AF	PIC 2 (Programmable Interrupt Controller 8259)			(1st at 0340-034F)
00A00	r/w	NMI mask register (XT)			
0040			0178-0	179	Power Management
00A0 00A1	r/w r/w	PIC 2 same as 0020 for PIC 1 PIC 2 same as 0021 for PIC 1 except for OCW1:	0178	w	index selection for data port
		bit 7 = 0 reserved	0179	r/w	power management data
		<pre>bit 6 = 0 enable fixed disk interrupt bit 5 = 0 enable correspondence execution interrupt</pre>			
		<pre>bit 5 = 0 enable coprocessor exception interrupt bit 4 = 0 enable mouse interrupt</pre>	0200-0	20F	Game port reserved I/O address space
		bit 3 = 0 reserved			Game port, eight identical addresses on some boards
		<pre>bit 2 = 0 reserved bit 1 = 0 enable redirect cascade</pre>	0201	r	read joystick position and status
		bit 0 = 0 enable real-time clock interrupt	0201	-	bit 7 status B joystick button 2 / D paddle button
					<pre>bit 6 status B joystick button 1 / C paddle button bit 5 status A joystick button 2 / B paddle button</pre>
		DMA 2 (second Direct Memory Access controller 8237)			bit 5 status A joystick button 2 / B paddle button bit 4 status A joystick button 1 / A paddle button
0007					bit 3 B joystick Y coordinate / D paddle coordinate
00C0 00C2	r/w r/w	DMA channel 4 memory address bytes 1 and 0 (low) (ISA, EISA) DMA channel 4 transfer count bytes 1 and 0 (low) (ISA, EISA)			bit 2 B joystick X coordinate / C paddle coordinate bit 1 A joystick Y coordinate / B paddle coordinate
00C4	r/w	DMA channel 5 memory address bytes 1 and 0 (low) (ISA, EISA)			bit 0 A joystick X coordinate / A paddle coordinate
0006	r/w	DMA channel 5 transfer count bytes 1 and 0 (low) (ISA, EISA)			fine institute from the both
00C8 00CA	r/w r/w	DMA channel 6 memory address bytes 1 and 0 (low) (ISA, EISA) DMA channel 6 transfer count bytes 1 and 0 (low) (ISA, EISA)		W	fire joysticks four one-shots
00CC	r/w	DMA channel 7 memory address byte 0 (low), then 1 (ISA, EISA)			
OOCE	r/w	DMA channel 7 transfer count byte 0 (low), then 1 (ISA, EISA)	0220-0	223	Sound Blaster / Adlib port
00D0	r	DMA channel 4-7 status register (ISA, EISA)	0220	r/w	Left speaker Status / Address port
		bit 7 = 1 channel 7 request	0221	W Traine	Left speaker Data port
		<pre>bit 6 = 1 channel 6 request bit 5 = 1 channel 5 request</pre>	0222	r/w	Right speaker Status / Address port Address:
		bit 4 = 1 channel 4 request			01 Enable waveform control

		02 Timer #1 data	0338		AdLib soundblaster card
		03 Timer #2 data			
		04 Timer control flags 08 Speech synthesis mode			SCSI (1st Small Computer System Interface) adapter
		20-35 Amplitude Modulation / Vibrato			(alternate at 0140-014F)
		40-55 Level key scaling / Total level 60-75 Attack / Decay rate			
		80-95 Sustain / Release rate	0370-0	0377	FDC 2 (2nd Floppy Disk Controller) first FDC at 03F0
		AO-B8 Octave / Frequency Number CO-C8 Feedback / Algorithm			(8272, 8272A, NEC765) (82072, 82077AA for perpendicular recording at 2.8Mb)
		E0-F5 Waveform Selection			
0223	W	Right speaker Data port	0370 0370	r r	diskette Extra High Density controller board jumpers (AT) diskette controller status A (PS/2, PS/2 model 30)
SeeAls	o: 0388-0	389	0371	r	diskette controller status B (PS/2, PS/2 model 30)
			0372 0374	w r	diskette controller DOR (Digital Output Register) diskette controller main status register
		Soundblaster PRO and SSB 16 ASP	0374	W	diskette controller datarate select register
			0375 0376		diskette controller command/data register (2nd FIXED disk controller data register)
0220-0	22F	Soundblaster PRO 2.0	0377	r	diskette controller DIR (Digital Input Register)
			0377	w	select register for diskette data transfer rate
		Soundblaster PRO 4.0			
0220 0220		left FM status port left FM music register address port (index)	0378-0	037A	parallel printer port, same as 0278 and 03BC
	r/w	left FM music data port	0378	w .	data port
0222 0222		right FM status port right FM music register address port (index)	0379 037A	r/w r/w	status port control port
		right FM music data port			
0224 0225	w r/w	mixer register address port (index) mixer data port			Sound Blaster / Adlib port
0226	w	DSP reset			-
	r w	FM music status port FM music register address port (index)	0388	r/w	Both Speakers Status / Address port Address:
0229	w	FM music data port			01 Enable waveform control
	r w	DSP read data (voice I/O and Midi) DSP write data / write command			02 Timer #1 data 03 Timer #2 data
022C	r	DSP write buffer status (bit 7)			04 Timer control flags
022E	r	DSP data available status (bit 7)			08 Speech synthesis mode 20-35 Amplitude Modulation / Vibrato
		The FM music is accessible on 0388/0389 for compatibility.			40-55 Level key scaling / Total level
					60-75 Attack / Decay rate 80-95 Sustain / Release rate
		Adaptec 154xB/154xC SCSI adapter.			A0-B8 Octave / Frequency Number
		alternate address at 0130, 0134, 0230, 0330 and 0334			CO-C8 Feedback / Algorithm EO-F5 Waveform Selection
			0389	w	Data port
0234-03	237	Adaptec 154xB/154xC SCSI adapter. alternate address at 0130, 0134, 0230, 0330 and 0334	Seells	so: 0220-0	2001
		alternate address at 0150, 0154, 0250, 0550 and 0554	Deexis	. 0220 0	5225
		parallel printer port, same as 0378 and 03BC			Soundblaster PRO FM-Chip
					Soundblaster 16 ASP FM-Chip
0278 0279	w r/w	data port status port			
02.111	r/w	control port	03B0-0	)3BF	MDA (Monochrome Display Adapter based on 6845)
			03B0-0 03B0	)3BF	MDA (Monochrome Display Adapter based on 6845)
		control port	03B0 03B1	)3BF	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5
		control port	03B0 03B1 03B2	)3BF	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4
 02B0-0	2DF	control port alternate EGA, primary EGA at 03C0	03B0 03B1		MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA)
02B0-02 02E8-02	2DF 2EF	control portalternate EGA, primary EGA at 03C0	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B4 MDA CRT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5
02B0-03	2DF 2EF	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8	03B0 03B1 03B2 03B3 03B4		MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 384. registers C-F may be read
02B0-02 02E8-02 02E8-02	2DF 2EF 2EF	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (O-11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 3B4. registers C-F may be read 00 horizontal total
02B0-03 02E8-03 02E8-03 02E8-03 02E8 02E8	2DF 2EF 2EF	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 384. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal spipajed 03 horizontal spipajed
02B0-0: 02E8-0: 02E8-0: 02E8-0: 02E8-0: 02E8 02E8 02E8	2DF 2EF 2EF r w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask	03B0 03B1 03B2 03B3 03B4	w	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 mDA CRT index register (EGA/VGA) selects which register (CEGA/VGA) selects which register (EGA/VGA) selected by port 384, registers C-F may be read 00 horizontal total 01 horizontal displayed 02 horizontal sync position 03 horizontal sync pulse width</pre>
02B0-03 02E8-03 02E8-03 02E8-03 02E8 02E8	2DF 2EF 2EF r w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 384. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal spipajed 03 horizontal spipajed
02B0-02 02E8-02 02E8-02 02E8 02E8 02E8 02E8 02E8 02E8 02E8 02	2DF 2EF 2EF r w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 384. registers C-F may be read 00 horizontal total 01 horizontal displayed 02 horizontal sync position 03 horizontal total 04 vertical total 05 vertical displayed 06 vertical sync position
02B0-03 02E8-03 02E8-03 02E8-03 02E8 02E8 02E8 02E8 02E8 02E8	2DF 2EF 2EF r w w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 S514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC write index	03B0 03B1 03B2 03B3 03B4	w	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (CEGA/VGA) selects which register (EGA/VGA) selected by port 3B4. registers C-F may be read 00 horizontal total 01 horizontal sync pulse width 04 vertical total 05 vertical displayed</pre>
02E0-0: 02E8-0: 02E8-0: 02E8-0: 02E8 02E8 02E8 02EA 02EB 02EC 02ED	2DF 2EF 2EF w w w w w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 S514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC write index	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 3B4. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync position 03 horizontal sync position 04 vertical total 05 vertical total 06 vertical total 07 vertical sunc positon 07 vertical sunc positon 08 interlace mode 09 maximum scan lines
02E0-0: 02E8-0: 02E8-0: 02E8-0: 02E8 02E8 02E8 02EA 02EB 02EC 02ED	2DF 2EF 2EF w w w w w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC vrite index DAC data	03B0 03B1 03B2 03B3 03B4	w	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 mDA CRT index register (EGA/VGA) selects which register (CO-11h) is to be accessed through 3B5 mDA CRT data register (EGA/VGA) selected by port 3B4, registers C-F may be read 00 horizontal total 01 horizontal displayed 02 horizontal sync pulse width 04 vertical displayed 06 vertical sync position 07 vertical sunc pulse width 08 interlace mode</pre>
0280-03 0228-03 0228-03 0228 0228 0228 0228 0228 0228 0228 02	2DF 2EF 7 2EF 4 4 4 4 4 4 4 4 4 2 2FF 2 2 5 7 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 5 4 5 4 5 4 5 4 5 4 5 4 5 4 5	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 B514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC vrite index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 0384 same as 0385 same as 0385 MDA CRT index register (EGA/VGA) selects which register (COA/VGA) selects which register (CEGA/VGA) selected by port 384. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync position 03 horizontal sync position 03 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync position 07 vertical sync position 08 interlace mode 09 maximum scan lines 04 cursor start 05 cursor end 06 start address high
0280-0: 0228-0: 0228-0: 0228-0: 0228 027 027 027 027 027 027 027 027	2DF 2EF 2EF w w w w w 2EF w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC write index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 3B4. registers C-F may be read 00 horizontal total 01 horizontal displayed 02 horizontal sync position 03 horizontal sync position 04 vertical total 05 vertical tisplayed 06 vertical sinc position 07 vertical sunc pulse width 08 interlace mode 09 maximum scan lines 04 cursor start 05 cursor end
0280-0: 0288-0: 0288-0: 0288-0: 0288 0288 0288 0280	2DF 2EF 2EF w w w w w w w z 2FF w r r/w r/w r/w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC vrite index DAC write index DAC write index Transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, high byte when DLAB=0	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 0384 same as 0385 same as 0385 MDA CRT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 385 MDA CRT data register (EGA/VGA) selected by port 384. registers C-F may be read 00 horizontal total 01 horizontal total 01 horizontal sync position 03 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync position 07 vertical sync position 08 interlace mode 09 maximum scan lines 04 cursor start 08 cursor start 09 start address low 00 start address low 01 cursor location low
0280-00 0288-00 0288-00 0288-00 0288 0288	2DF 2EF w w w w w 2FF w r r/w r/w r/w r/w r/w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC and index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 interrupt enable register Van DLAB=0 interrupt identification register	03B0 03B1 03B2 03B3 03B4	w	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 3B4. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync position 03 horizontal sync position 03 horizontal sync position 04 vertical total 05 vertical total 05 vertical sinc pulse width 08 interlace mode 09 maximum scan lines 04 cursor start 05 cursor location high 06 cursor location low 07 cursor location low 08 cursor location low
02280-00 02283-00 02283-00 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02273 0273 0273 02743 02274 02274	2DF 2EF 2EF v w w w w w v v v v v v v v v v v v v	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC write index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 interrupt emable register when DLAB=1 interrupt identification register line control register line control register	0380 0381 0382 0383 0384 0385	w	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B4 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selects which register (CEGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selects dup port 3B4. registers C-F may be read 00 horizontal displayed 02 horizontal displayed 03 horizontal displayed 04 vertical total 05 vertical sync position 05 vertical sync position 06 vertical sync position 07 vertical sunc pulse width 08 interlace mode 09 maximum scan lines 04 cursor start 06 cursor location high 07 cursor location low 10 light pen high 11 light pen low same as 03B4</pre>
02E8-0: 02E8-0: 02E8-0: 02E8 02E8 02E8 02E8 02E8 02E0 02E0 02E0	2DF 2EF 22F v v v v v v v v v v v v v v v v v	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC read index DAC vrite index DAC vrite index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, high byte when DLAB=1 divisor latch, high byte when DLAB=1 interrupt enable register when DLAB=1 interrupt enable register line status register line status register line status register	03B0 03B1 03B2 03B4 03B5 03B5	ч г/ч	MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (D-11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selected by port 3B4. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync pulse vidth 04 vertical total 05 vertical displayed 06 vertical sync pulse vidth 07 vertical sync pulse vidth 08 interlace mode 09 maximum scan lines 04 cursor start 05 cursor location high 00 start address low 10 cight pen high 11 light pen low same as 03B5
02280-00 02283-00 02283-00 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02283 02273 0273 0273 02743 02274 02274	2DF 2EF 2EF w w w w w w w w w w w w w w w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 6514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC read index DAC read index DAC vrite index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 interrupt enable register line control register modem control register modem control register line status register scratch register	0380 0381 0382 0383 0384 0385	w	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CAT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5 MDA CAT data register (CEGA/VGA) selects dup port 3B4. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync pulse width 03 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync position 07 vertical sync position 07 vertical sync position 08 interlace mode 09 maximu scan lines 00 cursor start 00 start address high 00 start address high 10 light pen high 11 light pen how same as 03B4 same as 03B5 MDA node control register bit 7 not used</pre>
	2DF 2EF v v v v v v v v v v v v v	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC read index DAC transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, new byte man blaB=0 interrupt identification register line control register modem control register scratch register	03B0 03B1 03B2 03B4 03B5 03B5	ч г/ч	MDA (Monochrome Display Adapter based on 6845) same as 0384 same as 0385 same as 0385 MDA CRT index register (EGA/VGA) selects which register (CDA/VGA) selected by port 384, registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync position 03 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync position 07 vertical sync position 08 interlace mode 09 maximum scan lines 04 cursor start 08 cursor location high 00 start address low 10 Light pen high 11 Light pen low same as 0385 MDA mode control register bit 6 not used
	2DF 2EF r w w w w w w w z z z z r r w w w w w w w w w w w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC read index DAC trais serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 interrupt enable register modem control register modem control register scratch register Soundblaster 16 ASP MPU-Midi	03B0 03B1 03B2 03B4 03B5 03B5	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selects dby port 384, registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync pulse width 03 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync pulse width 08 interlace mode 09 maximum scan lines 00 cursor start 08 cursor end 00 start address low 01 light pen high 11 light pen low same as 03B4 mMA mode control register bit 7 not used bit 6 ent used bit 6 ent used bit 6 makemed address low 01 light pen low 02 same as 03B5</pre>
	2DF 2EF 2EF w w w w w w z z ZFF w r r r r r r r w w w w w w w w w w w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC read index DAC transmitter holding register receiver buffer register transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, low stater when divisor latch	03B0 03B1 03B2 03B4 03B5 03B5	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (DeA/VGA) selects dup port 384, registers C-F may be read 00 horizontal displayed 01 horizontal displayed 02 horizontal sync position 03 horizontal sync position 04 vertical sync position 05 vertical sync position 06 vertical sync position 07 vertical sync position 07 vertical sync position 08 interlace mode 09 maximum scan lines 04 cursor start 08 cursor end 00 start address high 00 start address low 00 E cursor location high 01 light pen high 11 light pen nivs same as 03B4 same as 03B4 same as 03B5 MDA mode control register bit 7 not used bit 5 enable blink bit 4 not used bit 5 vide enable</pre>
	2DF 2EF 2EF w w w w w w z z ZFF w r r r r r r r w w w w w w w w w w w w w	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC read index DAC trais serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 interrupt enable register modem control register modem control register scratch register Soundblaster 16 ASP MPU-Midi	03B0 03B1 03B2 03B4 03B5 03B5	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selects dup port 384, registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync pulse width 03 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync pulse width 08 interlace mode 09 maximum scan lines 00 cursor start 08 cursor end 00 start address low 06 cursor location high 07 cursor location high 09 ilight pen high 11 light pen low same as 03B4 same as 03B5 MDA mode control register bit 7 not used bit 6 ent used bit 6 enable blink bit 4 not used</pre>
0280-0: 0228-0: 0227-0: 0300-0: 030	2DF 2EF r w w w w w z z z z r/w r/w r/w r/w r/w r/w r/w s 301 31F	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC read index DAC write index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 interrupt enable register line control register line status register line status register scratch register Soundblaster 16 ASP MPU-Midi prototype cards Periscope hardware debugger	03B0 03B1 03B2 03B4 03B5 03B5	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CAT index register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CAT data register (D=01h) is to be accessed through 3B5 MDA CAT data register (D=01h) is to be accessed through 3B5 MDA CAT data register (D=01h) is to be accessed through 3B5 MDA CAT data register (D=01h) is to be accessed through 3B5 MDA CAT data register (D=01h) is to be accessed through 3B5 MDA CAT data register (D=01h) is to be accessed through 3B5 MDA CAT data register (D=01h) is to be accessed through 3B5 MDA cat accessed through 3B5 MDA cat address position 07 vertical sunc pulse width 08 interlace mode 09 maximum scan lines 04 cursor start 05 cursor location high 00 start address high 00 start address high 10 ilight pen high 11 light pen how same as 03B5 MDA mode control register bit 7 not used bit 6 not used bit 6 not used bit 4 not used bit 4 not used bit 3 videe enable bit 2 not used bi</pre>
	2DF 2EF r w w w w 2FF w r r/w r/w r/w r/w r/w solution 301	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 6514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC read index DAC vrite index DAC vrite index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, high byte when DLAB=1 interrupt enable register line control register line status register scratch register Soundblaster 16 ASP MPU-Midi prototype cards	03B0 03B1 03B2 03B4 03B5 03B5	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (DeA/VGA) 0 horizontal total 0 horizontal total 0 horizontal sync position 0 horizontal sync position 0 horizontal sync position 0 horizontal sync position 0 vertical total 0 evertical total 0 evertical sync position 0 vertical sync position 0 vertical sync position 0 vertical sync position 0 vertical sync position 0 for start address high 0 start address high 0 start address high 0 for cursor location high 0 for cursor location high 11 light pen high 11 light pen high 11 light pen lov same as 03B5 MDA mode control register bit 7 not used bit 5 enable blink bit 4 not used bit 5 videe enable bit 2 not used bit 5 not used bit 1 not used bit 2 not used bit 2 not used bit 2 not used bit 5 not used bit 2 not used bit 1 not used bit 2 not used bit 5 not use</pre>
	2DF 2EF r w w w w 2FF w r r/w r/w r/w r/w r/w solution 301	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC arta serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, low byte when DLAB=0 interrupt identification register line control register Soundblaster 16 ASP MPU-Midi prototype cards Periscope hardware debugger MDDI interface	03B0 03B1 03B2 03B4 03B5 03B6 03B7 03B8	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CAT index register (EGA/VGA) selects which register (D-11h) is to be accessed through 3B5 MDA CAT data register (EGA/VGA) selected by port 3B4. registers C-F may be read 0 horizontal total 0 horizontal total 0 horizontal sync position 0 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync pulse width 07 vertical sunc pulse width 08 interlace mode 09 maximu scan lines 04 cursor start 09 doint address high 00 start address high 01 light pen high 11 light pen low same as 03B4 same as 03B5 MDA control register bit 7 not used bit 6 not used bit 6 not used bit 1 not used bit 1 not used bit 1 not used bit 1 not used bit 0 high resolution mode cursor location mode cursor location mode cursor location mode cursor start 0 if you satt address is you set to the for the start width 0 if you set to used bit 1 not used bit 1 not used bit 1 not used bit 1 not used bit 0 high resolution mode cursor start solution mode cursor location mode cursor location mode cursor start bit 7 not used bit 0 high resolution mode cursor start cursor start cursor start cursor start cursor location log cursor location</pre>
	2DF 2EF r w w w w 22F v r z r/w r/w r/w r/w s 301 331	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC write index DAC write index DAC data serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, high byte when DLAB=1 divisor latch, register scrach register scrach register Soundblaster 16 ASP MPU-Mid1 prototype cards Periscope hardware debugger	03B0 03B1 03B2 03B4 03B5 03B5 03B5 03B6 03B7 03B8	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B4 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selects which register (CEGA/VGA) selects which register (CEGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (CEGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (EGA/VGA) selects which register (D=11h) is to be accessed through 3B5 MDA CRT data register (D=11h) is to be accessed through 3B5 MDA crutoral sync position 0 horizontal sync position 0 horizontal sync position 0 vertical total 0 to vertical total 0 to vertical total 0 vertical sunc pulse width 0 is interlace mode 0 maximum scan lines 0 a cursor start 0 do ursor start 0 do ursor location high 0 for cursor location high 0 for cursor location high 1 1 light pen high 1 1 light pen high 1 1 light pen low 3 same as 03B5 MDA mode control register bit 7 not used bit 6 not used bit 6 not used bit 4 not used bit 6 not used bit 7 (MSD says) if this bit changes within 8000h reads then bit 6-4 = 000 = adapter is Hercules + </pre>
0280-0: 0228-0: 0300-0: 030	2DF 2EF r w w w w w w z z z z y r r/w r/w r/w r/w r/w s 301 331 333	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC ata serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 serial port register line control register line status register Soundblaster 16 ASP MPU-Midi prototype cards Periscope hardware debugger MIDI interface Adaptec 154xE/154xC SCSI adapter. default address. alternate address at 0130, 0134, 0230, 0234 and 0334	03B0 03B1 03B2 03B4 03B5 03B6 03B7 03B8	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B4 same as 03B5 same as 03B5 MDA CRT index register (EGA/VGA) selects which register (DEA/VGA) 0 horizontal displayed 2 horizontal displayed 2 horizontal displayed 2 horizontal sync position 3 horizontal displayed 3 horizontal displayed 3 horizontal displayed 3 horizontal sync position 3 horizontal displayed 3 horizontal displayed 3 horizontal sync position 3 tertical sync position 4 tertical sync position 5 tertica</pre>
	2DF 2EF r w w w w w w z z z z y r r/w r/w r/w r/w r/w s 301 331 333	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC ata serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 divisor latch, low byte when blaB=1 divisor la	03B0 03B1 03B2 03B4 03B5 03B6 03B7 03B8	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 03B4 same as 03B5 same as 03B5 MDA CAT index register (EGA/VGA) selects which register (CDA/VGA) selects which register (CDA/VGA) selects which register (CDA/VGA) selected by port 384. registers C-F may be read 00 horizontal total 01 horizontal total 02 horizontal sync pulse width 03 horizontal sync pulse width 04 vertical total 05 vertical displayed 06 vertical sync position 07 vertical sunc pulse width 08 interlace mode 09 maximu scan lines 04 cursor start 06 cursor location high 07 cursor location high 08 cursor location high 10 light pen high 11 light pen how same as 03B5 MDA collection register bit 7 not used bit 6 not used bit 6 not used bit 1 not used bit 0 high resolution mode reserved for color select register on color adapter CAT status register EGA/VGA: input status 1 register bit 7.4 (MSD says) if this bit changes with 8000 neads then bit 6-4 = 000 = adapter is Hercules in Color 01 = Color color is Hercules in Color 01 = adapter is Hercules in Color 01</pre>
0280-0; 02283-0; 02283-0; 02283-0; 02283-0; 02284-0; 02284-0; 02280 02285 028	2DF 2EF 2EF 2 2 2 2 2 2 2 2 2 2 2 2 2	control port alternate EGA, primary EGA at 03C0 serial port, same as 02F8, 03E8 and 03F8 8514/A and compatible video cards (e.g. ATI Graphics Ultra) display status horizontal total DAC mask DAC read index DAC ata serial port, same as 02E8, 03E8 and 03F8 transmitter holding register receiver buffer register divisor latch, low byte when DLAB=1 serial port register line control register line status register Soundblaster 16 ASP MPU-Midi prototype cards Periscope hardware debugger MIDI interface Adaptec 154xE/154xC SCSI adapter. default address. alternate address at 0130, 0134, 0230, 0234 and 0334	03B0 03B1 03B2 03B4 03B5 03B6 03B7 03B8	ч г/ч	<pre>MDA (Monochrome Display Adapter based on 6845) same as 0384 same as 0385 same as 0384 same as 0385 MDA CRT index register (EGA/VGA) selects which register (D-11h) is to be accessed through 385 MDA CRT data register (EGA/VGA) selects which register (CGA/VGA) selects which register on color adapter bit 7 (MSD says) if this bit changes within 800ch reads ther bit 2 = adapter is Hercules* 101 = adapter is Hercules* 101 = adapter is Hercules </pre>

					= 1 memory access without interfering with display
O3BA	w	EGA/VGA feature control register	O3DA	w	EGA/VGA feature control register
03BB		reserved for light pen strobe reset	03DB	v	clear light pen latch
		parallel printer port, same as 0278 and 0378	03DC	r/w	preset light pen latch
03BC	w	data port	03DF		CRT/CPU page register (PCjr only)
03BD	r/w	status port bit 7 = 0 busy			serial port, same as 02E8, 02F8 and 03F8
		bit 6 = 0 acknowledge			
		bit 5 = 1 out of paper bit 4 = 1 printer is selected			FDC 1 (1st Floppy Disk Controller) second FDC at 0370
		bit 3 = 0 error bit 2 = 0 IRQ has occurred			(8272, 8272A, NEC765) (82072, 82077AA for perpendicular recording at 2.8Mb)
		bit 1-0 reserved			
03BE	r/w	control port	03F0	r	diskette EHD controller board jumper settings (82072AA) bit 7-6 drive 3
		bit $7-5$ reserved bit $4 = 1$ enable IRQ			bit 5-4 drive 2 bit 3-2 drive 1
		bit 3 = 1 select printer			bit 1-0 drive 0
		bit 2 = 0 initialize printer bit 1 = 1 automatic line feed			= 00 1.2Mb = 01 720Kb
		bit 0 = 1 strobe			= 10 2.8Mb = 11 1.4Mb
 03BF	r/w		03F0	_	
U3BF	r/w	Hercules configuration switch register bit 7-2	03F0	r	diskette controller status A (PS/2) bit 7 interrupt pending
		<pre>bit 1 = 0 disables upper 32K of graphics mode buffer 1 enables upper 32K of graphics mode buffer</pre>			bit 6 -DRV2 second drive installed bit 5 step
		bit 0 = 0 prevents graphics mode			bit 4 -track 0
		1 allows graphics mode			bit 3 head 1 select bit 2 -index
		EGA (1st Enhanced Graphics Adapter) alternate at 02C0			bit 1 -write protect bit 0 +direction
03C0	(r)/w	EGA VGA ATC index/data register	03F0	r	diskette controller status A (PS/2 model 30)
03C1	r	VGA other attribute register	Joru	-	bit 7 interrupt pending
03C2	r W	EGA VGA input status 0 register VGA miscellaneous output register			bit 6 DRQ bit 5 step F/F
03C3	r/w	VGA video subsystem enable (see also port 46E8h) for IBM, motherboard VGA only			bit 4 -track 0 bit 3 head 1 select
03C4	w	EGA TS index register			bit 2 +index
0305	r/w w	VGA sequencer index register EGA TS data register			bit 1 +write protect bit 0 -direction
03C6	r/w r/w	VGA other sequencer register VGA PEL mask register	03F1		diskette controller status B (PS/2)
03C0	r/w	VGA PEL address read mode	03F1	1	bit 7-6 =1 reserved
03C8	r r/w	VGA DAC state register VGA PEL address write mode			<pre>bit 5 drive select (0=A:, 1=B:) bit 4 write data</pre>
03C9 03CA	r/w w	VGA PEL data register EGA graphics 2 position register			bit 3 read data bit 2 write enable
	r	VGA feature control register			bit 1 motor enable 1
0300	w r	EGA graphics 1 position register VGA miscellaneous output register			bit 0 motor enable 0
03CE	w	EGA GDC index register	03F1	r	diskette controller status B (PS/2 model 30) bit 7 -DRV2 second drive installed
03CF	r/w w	VGA graphics address register EGA GDC data register			bit 6 -DS1
	r/w	VGA other graphics register			bit 5 -DSO bit 4 write data F/F
		CGA (Color Graphics Adapter)			bit 3 read data F/F bit 2 write enable F/F
					bit 1 -DS3
03D0 03D1		same as 03D4 same as 03D5			bit 0 -DS2
03D2 03D3		same as 03D4 same as 03D5	03F2	w	diskette controller DOR (Digital Output Register) bit 7-6 reserved on PS/2
03D4	w	CRT (6845) index register (EGA/VGA) selects which register (0-11h) is to be accessed through 3B5			bit 7 = 1 drive 3 motor enable bit 6 = 1 drive 2 motor enable
03D5	w	CRT (6845) data register (EGA/VGA)			bit 5 = 1 drive 1 motor enable
		selected by port 3B4. registers C-F may be read (for registers see at 3B5)			<pre>bit 4 = 1 drive 0 motor enable bit 3 = 1 diskette DMA enable (reserved PS/2)</pre>
03D6		same as 03D4			bit 2 = 1 FDC enable (controller reset)
03D7 03D8	r/w	same as O3D5 CGA mode control register (except PCjr)			= 0 hold FDC at reset bit 1-0 drive select (0=A 1=B)
		bit 7-6 not used bit 5 = 1 blink enabled	03F3		tape drive register (on the 82077AA)
		bit 4 = 1 640*200 graphics mode bit 3 = 1 video enabled			bit 7-2 reserved, tri-state bit 1-0 tape select
		bit 2 = 1 monochrome signal			= 00 none, drive 0 cannot be a tape drive.
		<pre>bit 1 = 0 text mode = 1 320*200 graphics mode</pre>			= 01 drive1 = 10 drive2
		bit 0 = 0 40*25 text mode = 1 80*25 text mode			= 11 drive3
0202			03F4	r	diskette controller main status register
03D9	r/w	CGA palette register bit 7-6 not used			<pre>bit 7 = 1 RQM data register is ready</pre>
		<pre>bit 5 = 0 active color set: red, green brown = 1 active color set: cyan, magenta, white</pre>			<pre>bit 6 = 1 transfer is from controller to system</pre>
		bit 4 intense colors in graphics, background colors text			bit 5 = 1 non-DMA mode
		bit 3 intense border in 40*25, intense background in 320*200, intense foreground in 640*200			<pre>bit 4 = 1 diskette controller is busy bit 3 = 1 drive 3 busy (reserved on PS/2)</pre>
		bit 2 red border in 40*25, red background in 320*200, red foreground in 640*200			bit $2 = 1$ drive 2 busy (reserved on PS/2) bit $1 = 1$ drive 1 busy (= drive is in seek mode)
		bit 1 green border in 40*25, green background in			bit 0 = 1 drive 0 busy (= drive is in seek mode)
		320*200, green foreground in 640*200 bit 0 blue border in 40*25, blue background in 320*200,			Note: in non-DMA mode, all data transfers occur through port 03F5h and the status registers (bit 5 here
		blue foreground in 640*200			indicates data read/write rather than than command/status read/write)
O3DA	r	CGA status register EGA/VGA: input status 1 register			
		bit 7-4 not used bit 3 = 1 in vertical retrace	03F4	W	<pre>diskette controller data rate select register bit 7 = 1 S/W reset</pre>
		<pre>bit 2 = 1 light pen switch is off bit 1 = 1 positive edge from light pen has set trigger</pre>			bit 6 = 1 power down bit 5 = 0 reserved
		bit 1 = 1 positive edge from fight pen has set trigger bit 0 = 0 do not use memory			bit 5 = 0 reserved bit 4-2 write precompensation, 000 default
		-			

		bit 1-0 data rate = 00 500 Kb/s							1 head select 3 enable bit 2 = 1 disk reset enable
		= 01 300 Kb/s	s (MFM)						0 disk reset disable
		= 10 250 Kb/s = 11 1 Mb/s							<pre>bit 1 = 0 disk initialization enable     1 disk initialization disable</pre>
									bit 0 reserved
03F5	r	diskette command/data r bit 7-6 last comm					03F7	r	diskette controller DIR (Digital Input Register, PC/AT mode)
		= 00 command	terminat	ted successfu	illy				bit 7 = 1 diskette change
		= 01 command = 10 invalid			Ly				bit 6-0 tri-state on FDC
		= 11 terminat bit 5 = 1 seek comp	ed abnor	rmally by cha	ange	in ready signal			bit 6 FIXED DISK write gate bit 5 FIXED DISK head select 3 / reduced write current
		bit 4 = 1 equipment		occurred aft	er ei	ror			bit 4 FIXED DISK head select 2
		bit 3 = 1 not ready bit 2 = 1 head numb		ntormunt					bit 3 FIXED DISK head select 1 bit 2 FIXED DISK head select 0
		bit 1-0 = 1 unit sele	ect (O=A	1=B )					bit 1 FIXED DISK drive 1 select
		(on PS/2	01=A 1	10=B)					bit 0 FIXED DISK drive 0 select
		status register 1 (ST1)					03F7	r	diskette controller DIR (Digital Input Register, PS/2 mode)
		bit 7 end of cyli bit 6 = 0	.nder; se	ector# greate	er ti	en sectors/track			bit 7 = 1 diskette change bit $6-3 = 1$
		bit 5 = 1 CRC error i bit 4 = 1 overrun	in ID or	data field					bit 2 datarate select1 bit 1 datarate select0
		bit 3 = 0							bit 0 = 0 high density select (500Kb/s, 1Mb/s)
		bit 2 = 1 sector ID n bit 1 = 1 write prote			mite		confli	cts with	h bit 0 FIXED DISK drive 0 select
		bit 0 = 1 ID address			*1104	2		CCS WICH	
		status register 2 (ST2)	,				03F7	r	<pre>diskette controller DIR (Digital Input Register, PS/2 model 30) bit 7 = 0 diskette change</pre>
		bit 7 = 0							bit 6-4 = 0
		<pre>bit 6 = 1 deleted Dat bit 5 = 1 CRC error i</pre>		ss Mark deteo	cted				bit 3 -DMA gate from DOR register bit 2 NOPREC from CCR register
		bit 4 = 1 wrong cylin	nder dete						bit 1 datarate select1
		bit 3 = 1 scan comman bit 2 = 1 scan comman							bit 0 datarate select0
		bit 1 = 1 bad cylinde	er, ID no	ot found			03F7	w	configuration control register (PC/AT, PS/2)
		bit 0 = 1 missing Dat	a Addres	ss Mark					bit 7-2 reserved, tri-state bit 1-0 = 00 500 Kb/S mode
		status register 3 (ST3) bit 7 fault statu		1					= 01 300 Kb/S mode = 10 250 Kb/S mode
		bit 6 write prote	ect stati						= 11 reserved
		bit 5 ready statu bit 4 track zero					03F7	w	configuration control register (PS/2 model 30)
		bit 3 two sided s	status si				0011	-	bit 7-3 reserved, tri-state
		bit 2 side select bit 1-0 unit select							bit 2 NOPREC (has no function. set to 0 by hardreset) bit 1-0 = 00 500 Kb/S mode
0075									= 01 300 Kb/S mode
03F5	W	diskette command regist mostly multibyte comman							= 10 250 Kb/S mode = 11 reserved
		MFM = MFM mode	selecter	d opposite:	o Mi	mode			
		HDS = head sele	ect	u, oppoblice (		modor	03F8-03	FF	serial port (8250,8251,16450,16550), same as 02E8,02F8 and 03E8
		DS = drive sel MT = multi tra		ation			03F8	w	serial port, transmitter holding register, which contains the
		SK = skip dele			rk				character to be sent. Bit 0 is sent first.
		Command #	bytes	D7 6 5	4	3 2 1 0		r	bit 7-0 data bits when DLAB=0 (Divisor Latch Access Bit) receiver buffer register, which contains the received character
		read track	9	0 MFM 0 0 0 0	0 0	0 0 1 0 0 HDS DS1 DS0			Bit 0 is received first bit 7-0 data bits when DLAB=0 (Divisor Latch Access Bit)
		specify	3	0 0 0	0	0 0 1 1		r/w	divisor latch low byte when DLAB=1
		sense drive status	2	0 0 0	0	0 1 0 0 0 HDS DS1 DS0	03F9	r/w	divisor latch high byte when DLAB=1
		write data	9	MT MFM O	0	0 1 0 1	0010	r/w	interrupt enable register when DLAB=0
		read data	9	0 0 0 MT MFM SK	0	0 HDS DS1 DS0 0 1 1 0			bits 7-4 reserved bit 3 = 1 modem-status interrupt enable
				0 0 0	0	0 HDS DS1 DS0			bit 2 = 1 receiver-line-status interrupt enable
		recalibrate	2	0 0 0 0 0	0 0	0 1 1 1 0 0 DS1 DS0			<pre>bit 1 = 1 transmitter-holding-register empty interrupt enable bit 0 = 1 received-data-avail.int. enable (and 16550 timeout)</pre>
		sense interrupt status write deleted data	s 1 9	0 0 0 MT MFM 0	0 0	1 0 0 0 1 0 0 1		-	- 16550 will interrupt if data exists in the FIFO and isn't read
			-	0 0 0	0	0 HDS DS1 DS0			within the time it takes to receive four bytes or if no data is
		read ID	2	0 MFM 0 0 0 0		1 0 1 0 0 HDS DS1 DS0			received within the time it takes to receive four bytes
		read deleted data	9	MT MFM SK	0	1 1 0 0	03FA	r	interrupt identification register. Information about a pending
		format track	10	0 0 0 0 MFM 0	0	0 HDS DS1 DS0 1 1 0 1			interrupt is stored here. When the ID register is addressed, the highest priority interrupt is held, and no other interrupts
		dumping th	1	0 0 0	0 0	0 HDS DS1 DS0 1 1 1 0			are acknowledged until the CPU services that interrupt. bit 7-6 = 00 reserved on 8250, 8251, 16450
		dumpreg ** seek	3	0 0 0	0	1 1 1 1			= 11 if FIFO queues are enabled (16550 only)
		version **	1	0 0 0	0 1	0 HDS DS1 DS0 0 0 0 0			bit $5-4 = 0$ reserved bit $3 = 0$ reserved 8250, 16450
		scan equal *	9	MT MFM SK	1	0 0 0 1			= 1 16550 timeout int. pending
		perpendicular mode **	2	0 0 0	0 1	0 HDS DS1 DS0 0 0 1 0			<pre>bit 2-1 identify pending interrupt with the highest priority = 11 receiver line status interrupt. priority=highest</pre>
				0 0 0	0	0 0 WGATE GAP			= 10 received data available register interrupt. pr.=second
		configure **	4	0 0 0	1 0	0 0 1 1 0 0 0 0			<pre>= 01 transmitter holding register empty interrupt. pr.=third = 00 modem status interrupt. priority=fourth</pre>
		verify	9	MT MFM SK	1	0 1 1 0			bit 0 = 0 interrupt pending. contents of register can be used
		scan low or equal *	9	EC 0 0 MT MFM MK	0 1	0 HDS DS1 DS0 1 0 0 1			as a pointer to the appropriate int.service routine 1 no interrupt pending
		scan high or equal *	9	O O O MT MFM MK	0 1	0 HDS DS1 DS0 1 1 0 1		-	- interrupt pending flag uses reverse logic, 0=pending, 1=none
				0 0 0	0	0 HDS DS1 DS0		-	interrupt will occur if any of the line status bits are set
		relative seek **	3	1 DIR 0 0 0 0	0 0	1 1 1 1 0 HDS DS1 DS0		-	- THRE bit is set when THRE register is emptied into the TSR
		BEWARE: not every inva * Note: the scan comm					03FA	w	16650 FCR (FIFO Control Register) bit $7-6 = 00$ 1 byte
		** Note: EHD controlle							= 01 4 bytes
03F6		reserved on FDC							= 10 8 bytes = 11 14 bytes
03F6	r/w	FIXED disk controller d	data reg	ister					bit $5-4 = 00$ reserved bit $3 = 1$ change RXRDY TXRDY pins from mode 0 to mode 1
552.0	-/ -	bit 7-4 reserved							bit 2 = 1 clear XMIT FIFO
		bit 3 = 0 reduce writ	e curren	nt					bit 1 = 1 clear RCVR FIFO

		bit 0 = 1 enab	ble clear XMIT and RCVR FIFO queues			bit 0 = 1	force data-terminal-ready active
		- bit 1 when set th	in order to write to other FCR bits ne RCVR FIFO is cleared and this bit is reset ft register is not cleared	03FD	r	line status bit $7 = 0$ bit $6 = 1$	
		- bit 2 when set th	ne XMIT FIFO is cleared and this bit is reset ft register is not cleared			bit 5 = 1	transmitter holding register empty. Controller is ready toaccept a new character to send. break interrupt. the received data input is held in
03FB	r/w	line control regis bit 7 = 1 diviso	ster or latch access bit (DLAB)			D1t 4 = 1	break interrupt. the received data input is held in in the zero bit state longer than the time of start bit + data bits + parity bit + stop bits.
		enable	ver buffer, transmitter holding, or interrupt e register access				framing error. the stop bit that follows the last parity or data bit is a zero bit.
		state	reak enable. serial ouput is forced to spacing and remains there.				parity error. Character has wrong parity overrun error. a character was sent to the receiver
		bit 4 = 1 even p	parity parity select 7 enable				buffer before the previous character in the buffer could be read. This destroys the previous character.
		1 even r data w	number of ones are sent and checked in the word bits and parity bit umber of ones are sent and checked			bit 0 = 1	
		bit 2 = 0 one st	top bit	03FE	r	modem statu:	s register
		1 zero s	stop bit			bit 7 = 1	data carrier detect
		bit 1-0 00 word 1	length is 5 bits			bit 6 = 1	ring indicator
		01 word 1	length is 6 bits			bit 5 = 1	data set ready
		10 word 1	length is 7 bits			bit 4 = 1	clear to send
		11 word 1	length is 8 bits			bit 3 = 1	delta data carrier detect
						bit 2 = 1	trailing edge ring indicator
03FC	r/w	modem control regi	ister			bit 1 = 1	delta data set ready
		bit 7-5 = 0 rese	erved			bit 0 = 1	delta clear to send
		bit 4 = 1 loopba	ack mode for diagnostic testing of serial port				
		output	t of transmitter shift register is looped back			- bits 0-3 are	e reset when the CPU reads the MSR
		to rec	ceiver shift register input. In this mode			- bit 4 is the	e Modem Control Register RTS during loopback test
		transm	nitted data is received immediately so that			- bit 5 is the	e Modem Control Register DTR during loopback test
		the CF	PU can verify the transmit data/receive data			- bit 6 is the	e Modem Control Register OUT1 during loopback test
			L port paths.			- bit 7 is the	e Modem Control Register OUT2 during loopback test
			iary user-designated output 2				
			iary user-designated output 1	03FF	r/w	scratch reg	ister
		bit 1 = 1 force	request-to-send active				

#### Credits

- Chuck Proctor <71534.2302@CompuServe.COM>.
- Richard W. Watson <73042.1420@CompuServe.COM>.
- Some of the information in this list was extracted from Frank van Gilluwe's *The Undocumented PC*, a must-have book for anyone programming down to the "bare metal" of a PC.
- Some of the information in this list from the shareware version of Dave Williams' DOSREF, v3.0.
- $\bullet~8514/\mathrm{A}$  hardware ports found in FractInt v18.0 source file FR8514A.ASM
- Compaq QVision info from the COMPAQ QVision Graphics System Technical Reference Guide, second edition (October 1993). Compaq part number 073A/0693.

## Chapter 2

# Data sheets

The following data sheets document the chips installed on Eos systems.

- i8259 Programmable Interrupt Controller
- NS16550 Unisersal Asynchronous Receiver/Transmitter with FIFOs
- i8253 Programmable Interval Timer
- DS12887 Real Timer Clock
- MC14469 Addressable Asynchronous Receiver/Transmitter (AART)