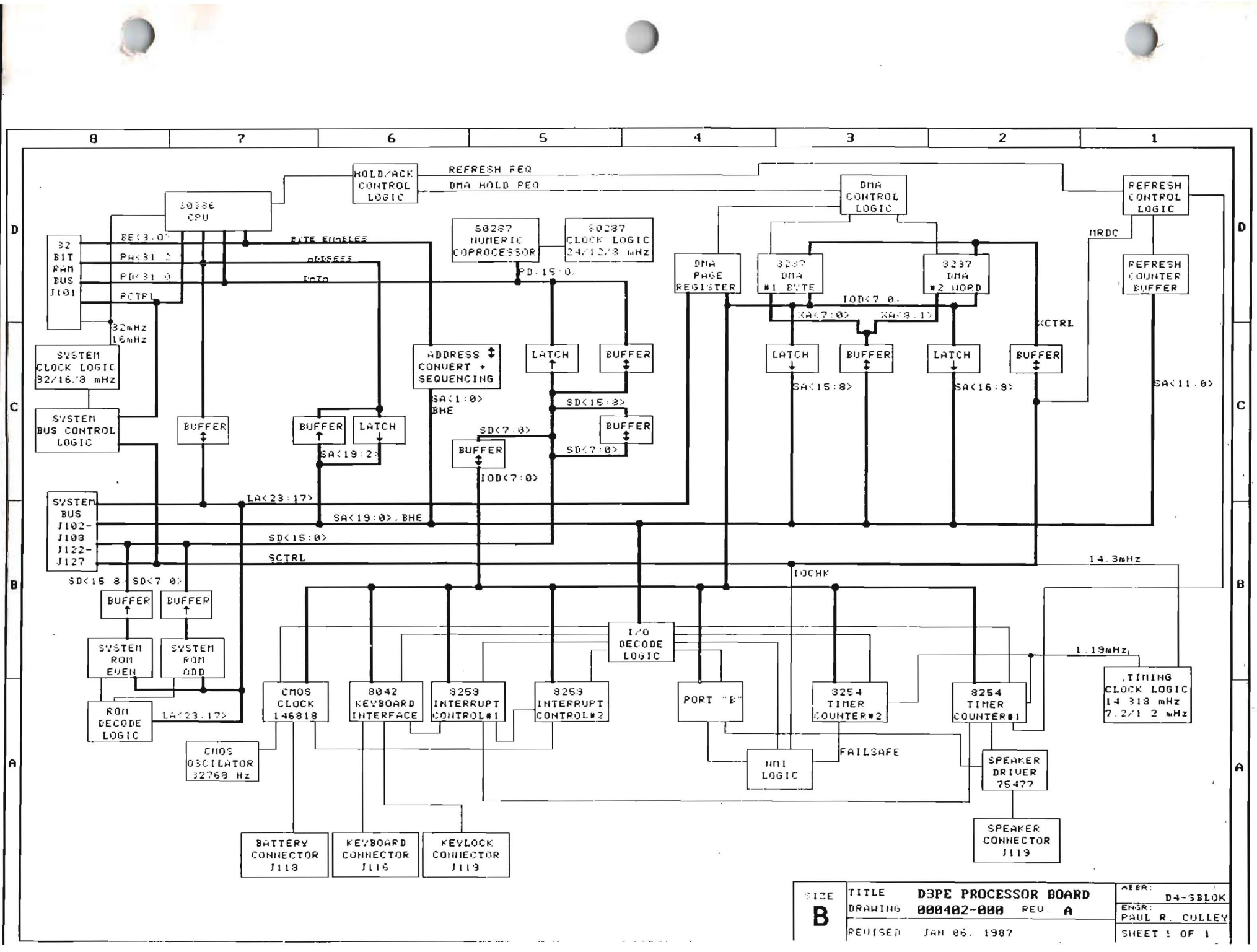

HOLD/ACK CONTROL LOGIC
REFRESH REQ
DMA HOLD REQ
80386 CPU
DMA CONTROL LOGIC
REFRESH CONTROL LOGIC
32 BIT RAM BUS J101
BE<3:0>
PH<31:2>
PD<31:0>
PCTRL
BYTE ENABLES
ADDRESS
DATA
80287 NUMERIC COPROCESSOR
80287 CLOCK LOGIC 24/12/8 mHz
PD<15:0>
DMA PAGE REGISTER
8237 DMA #1 BYTE
8237 DMA #2 WORD
IOD<7:0>
XA<7:0>
XA<8:1>
MRDC
REFRESH COUNTER BUFFER
SCTRL
32mHz
16mHz
SYSTEM CLOCK LOGIC 32/16/8 mHz
ADDRESS CONVERT + SEQUENCING
LATCH
BUFFER
SA<1:0>
BHE
SD<15:8>
SD<7:0>
SA<15:8>
SA<16:9>
SA<11:0>
SYSTEM BUS CONTROL LOGIC
BUFFER
LATCH
SA<19:2>
SYSTEM BUS J102-J108 J122-J127
LA<23:17>
SA<19:0>, BHE
SD<15:0>
SCTRL
SD<15:8>, SD<7:0>
IOCHK
14.3mHz
SYSTEM ROM EVEN
SYSTEM ROM ODD
ROM DECODE LOGIC
LA<23:17>
I/O DECODE LOGIC
1.19mHz
CMOS CLOCK 146818
8042 KEYBOARD INTERFACE
8259 INTERRUPT CONTROL#1
8259 INTERRUPT CONTROL#2
PORT "B"
8254 TIMER COUNTER#2
8254 TIMER COUNTER#1
TIMING CLOCK LOGIC 14.318 mHz 7.2/1.2 mHz
CMOS OSCILLATOR 32768 Hz
NMI LOGIC
FAILSAFE
SPEAKER DRIVER 75477
SPEAKER CONNECTOR J119
BATTERY CONNECTOR J118
KEYBOARD CONNECTOR J116
KEYLOCK CONNECTOR J119
SIZE B
TITLE D3PE PROCESSOR BOARD
DRAWING 000402-000 REV. A
REVISED JAN 06, 1987
ABER: D4-SBLOK
ENGR: PAUL R. CULLEY
SHEET 1 OF 1

1)W1 AND CR4 SILKSCREEN SHOULD BE AS SHOWN

2)TRACE WIDTH MINIMUM FOR SIGNALS +12V, +12VA IS 0.05 INCH IN TWO LAYERS OR 0.1 INCH.

3)TRACE WIDTH MINIMUM FOR SIGNALS -5V, -12V, +F1, +F2, +KB, -KB IS 0.05 INCH.

4)NETS WITH A NAME BEGINNING IN 'Z' MUST BE LESS THAN 2 INCHES LONG TOTAL TRACE LENGTH

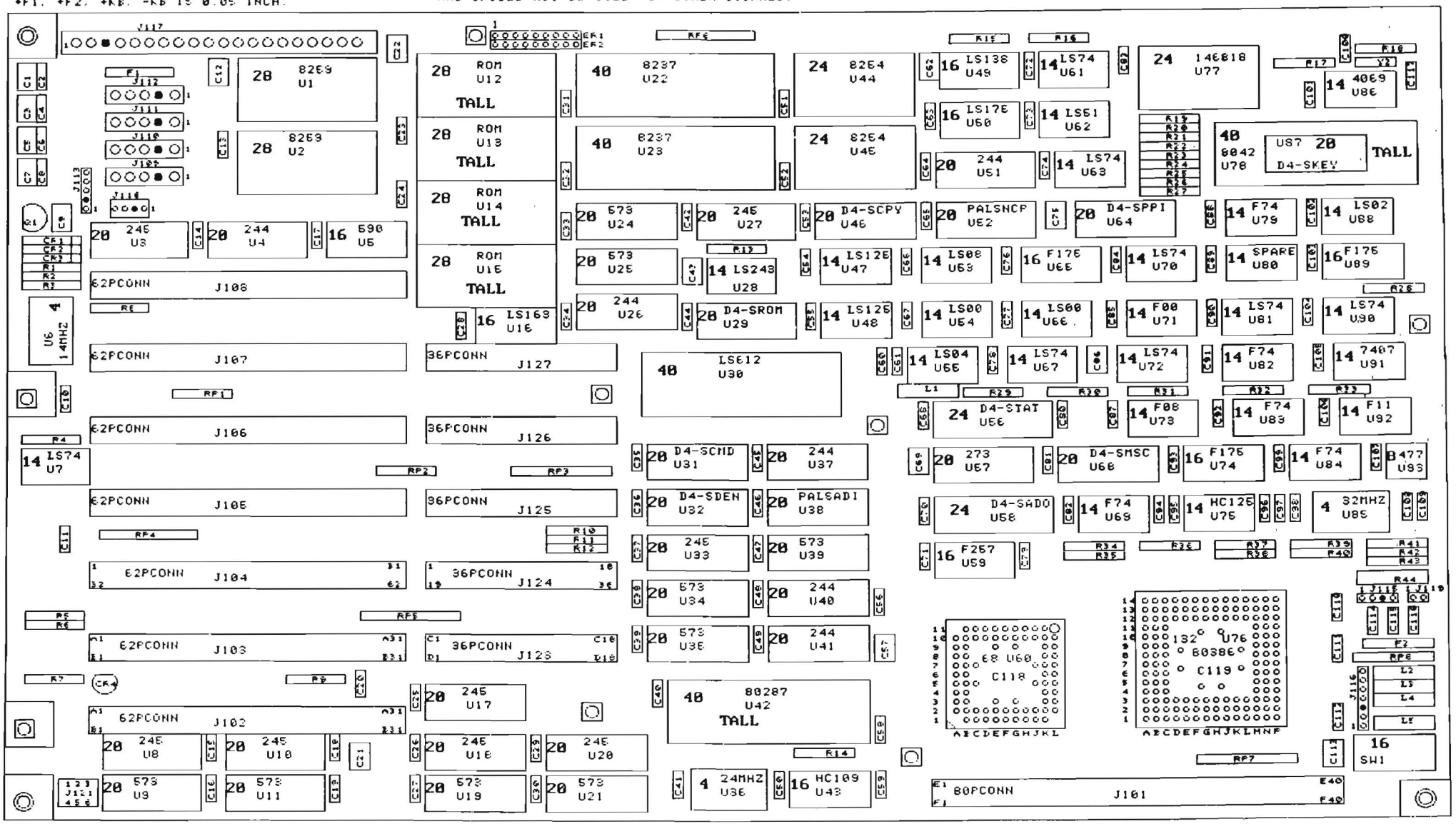
5)SIGNAL +5V AND GND ARE POWER PLANES AND SHOULD NOT BE USED FOR OTHER SIGNALS.

6)J109-113, J115-118 KEYS MUST NOT BE DRILLED BUT PADS MUST BE PRESENT

7)POLARIZED AND DECOUPLING CAPS SHOULD BE VERTICAL AND HAVE "+" UP.

8)SEE LAYOUT DETAIL FOR U86,U36,U85 HOOKUPS

9)ALL AXIAL DEVICES SHOULD BE HORIZONTAL.



LAYOUT-DP3E REV X

ASSY 000558 PCB 000560

REVISED JULY 25, 1986

D4 PAGE DRAM BOARD REV X3

On Vcc and Gnd connections to power planes for P101 and P121, use one feedthrough per gold finger. Do NOT put a thermal relief on power plane.

Traces with net names beginning in "Z" should be less than two inches total trace length

All Caps should have the Vcc pin down.

Route the board with normal size pads then reduce to sizes shown below.

Sizes are as follows	holes	pads	Pwr plane CLEARs
Radial devices	0.040	0.064	0.070
Axial devices	0.038	0.056	0.062
ICs	0.036	0.054	0.062
SIP resistors	0.038	0.056	0.062
J301 J302 E123	0.038	0.056	0.062
VIAs	0.025	0.044	0.050

J301, J302 are 40 pin headers, 2 rows of 20 on a 0.1 inch grid.

E123 is a nine pin header on a 0.1 inch grid.

No components in area cut by dotted line .....

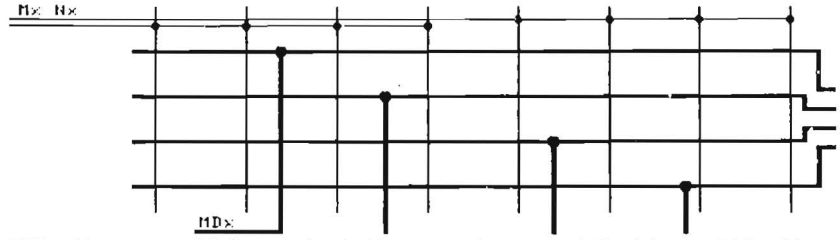
No traces or components in area cut by solid line. ———

Areas around three tooling holes in corners should be clear of etch for 0.2 inch diameter around hole.

Areas around board mounting bracket holes (at end) should be clear of etch 0.175 inch from hole center and to edge of board. (area is rectangular)

No components hole centers should be closer than 0.300 inch to top of board or 0.400 inch to bottom of board. These areas can be used for routing.

The flow of lines to the memory array should go as shown below:



RASx lines should lay out similar to the Mx and Nx lines. CASx lines should be similar to the MDx lines

Pads on ICs should be round, except for pin 1 which should be square. Please route the memory array such that the traces are as short as possible (use 45 degree routing or lay in by hand and repeat)

All ICs should have pin 1 at left when viewed as shown below.

The following text needs to appear on the top side of the board

ASSY 000413-[ ]
SERIAL [ ] BOXES ARE 0.200 X 0.700 AREA CLEAR OF SOLDER MASK

The following text can appear anywhere that it can be read.

COPYRIGHT COMPAQ COMPUTER 1986
BOARD 000415-001 REV X3
DIAGRAM 000414-000
MADE IN U.S.A

From IC hole center to VIA center, minimum distance is 0.10 inch, outside of IC body sides only (lead clinch).

From axial devices hole center to VIA center, minimum distance is 0.150 inch, inside of axial body only.

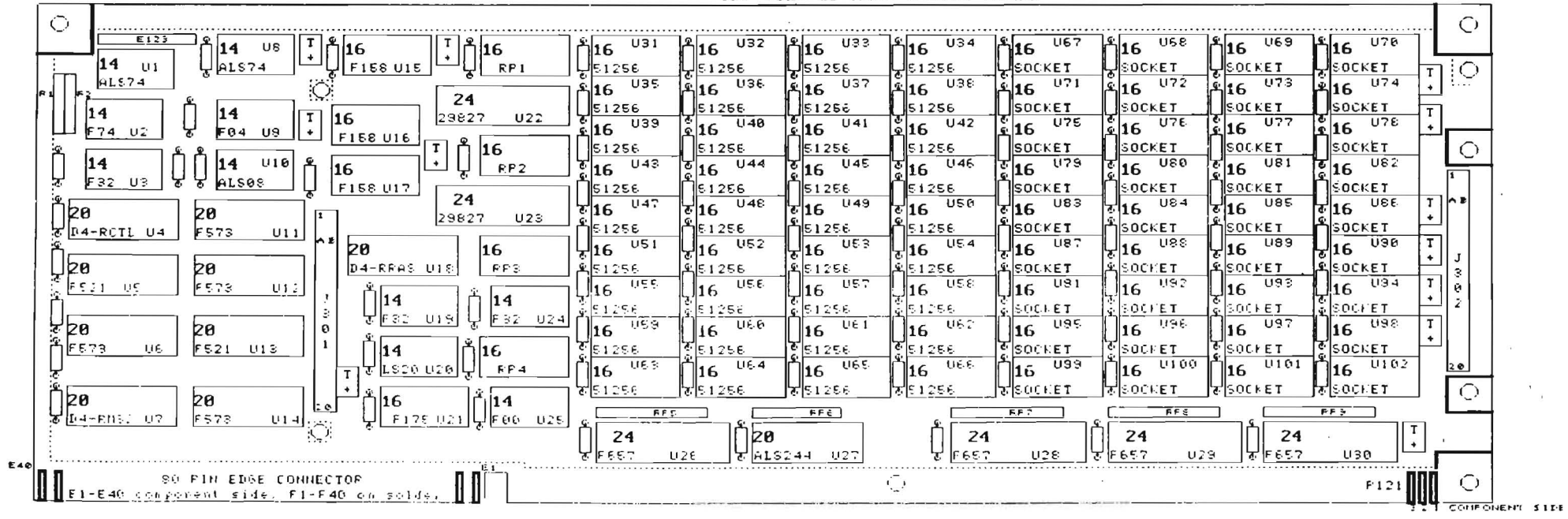
From radial devices hole center to VIA center, min distance is 0.150 inch outside of radial body only

Note the addition of P121 to the layout. See the mecanincal drawing for exact placement.

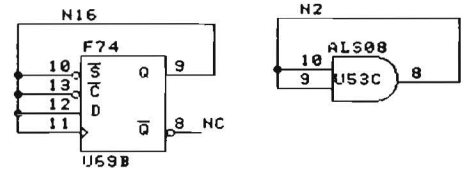
Caps in memory array must be centered between ICs and 0.125 min from end of RAM ICs (holes)

Caps out of memory array should be a min of 0.150 from end of ICs

TOP VIEW OF MAIN MEMORY BOARD



SPARE PARTS



DIP14
U80

UNUSED REF DESIGNATORS

Y1

PCB PART NUMBER 000560
ASSY PART NUMBER: 000558

APPROVALS	DATE
DRAWN PAUL R. CULLEY	
CHECKED	
COG ENGR	
ENGR	
ENGR	
MFG	
QA	
OTHER	
OTHER	

COMPAQ™ COMPUTER CORPORATION

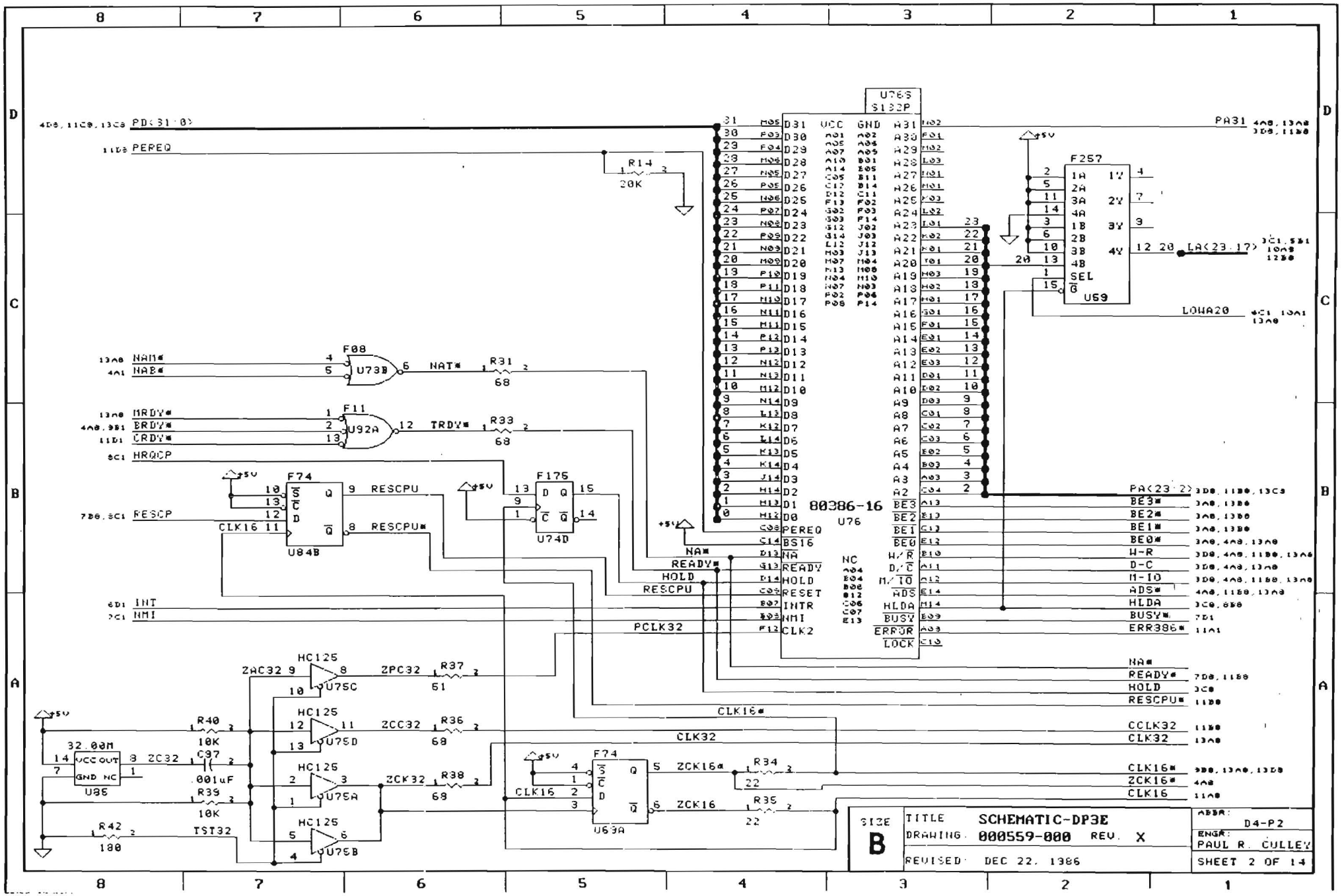
TITLE:

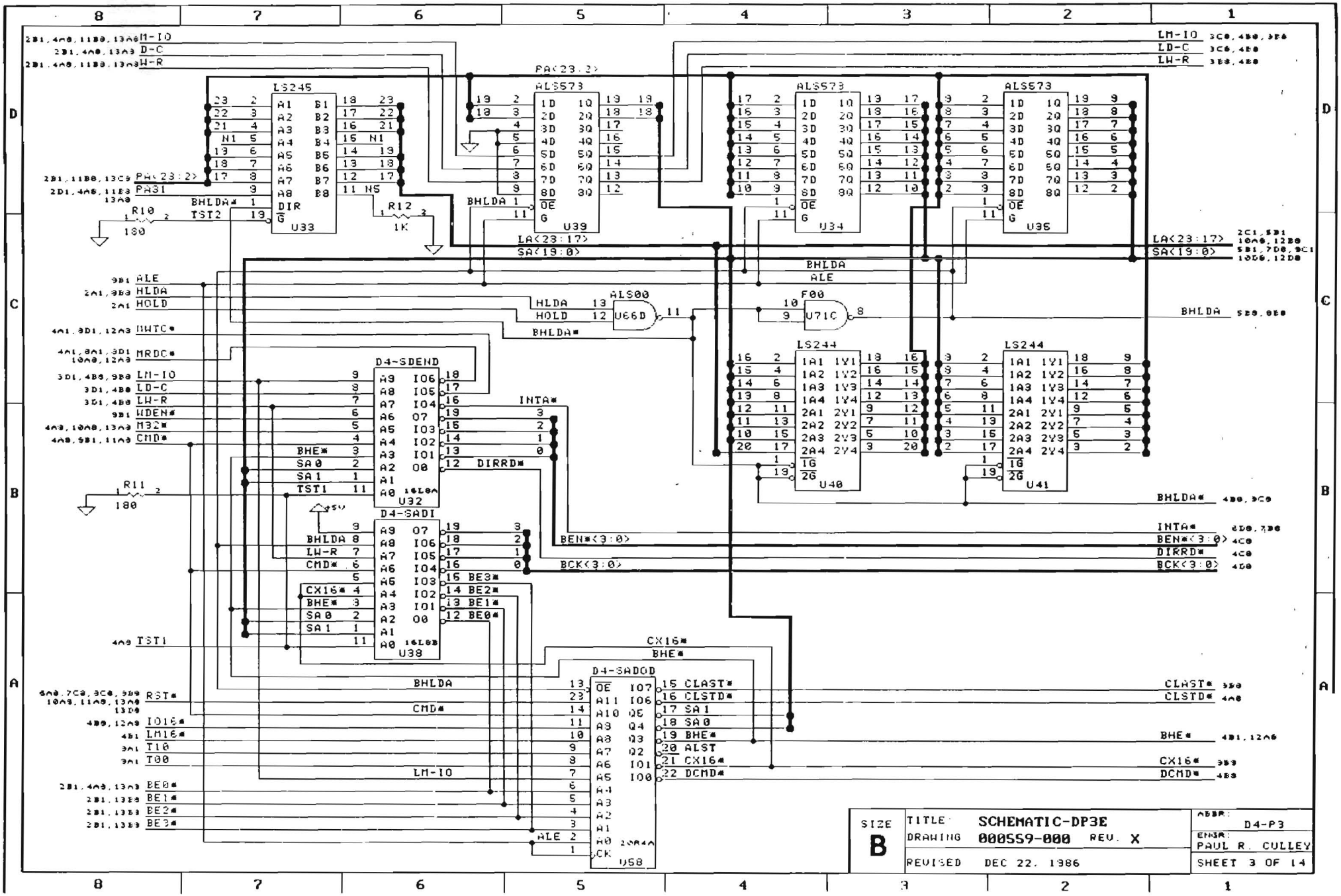
D4 MOTHER BOARD SCHEMATIC

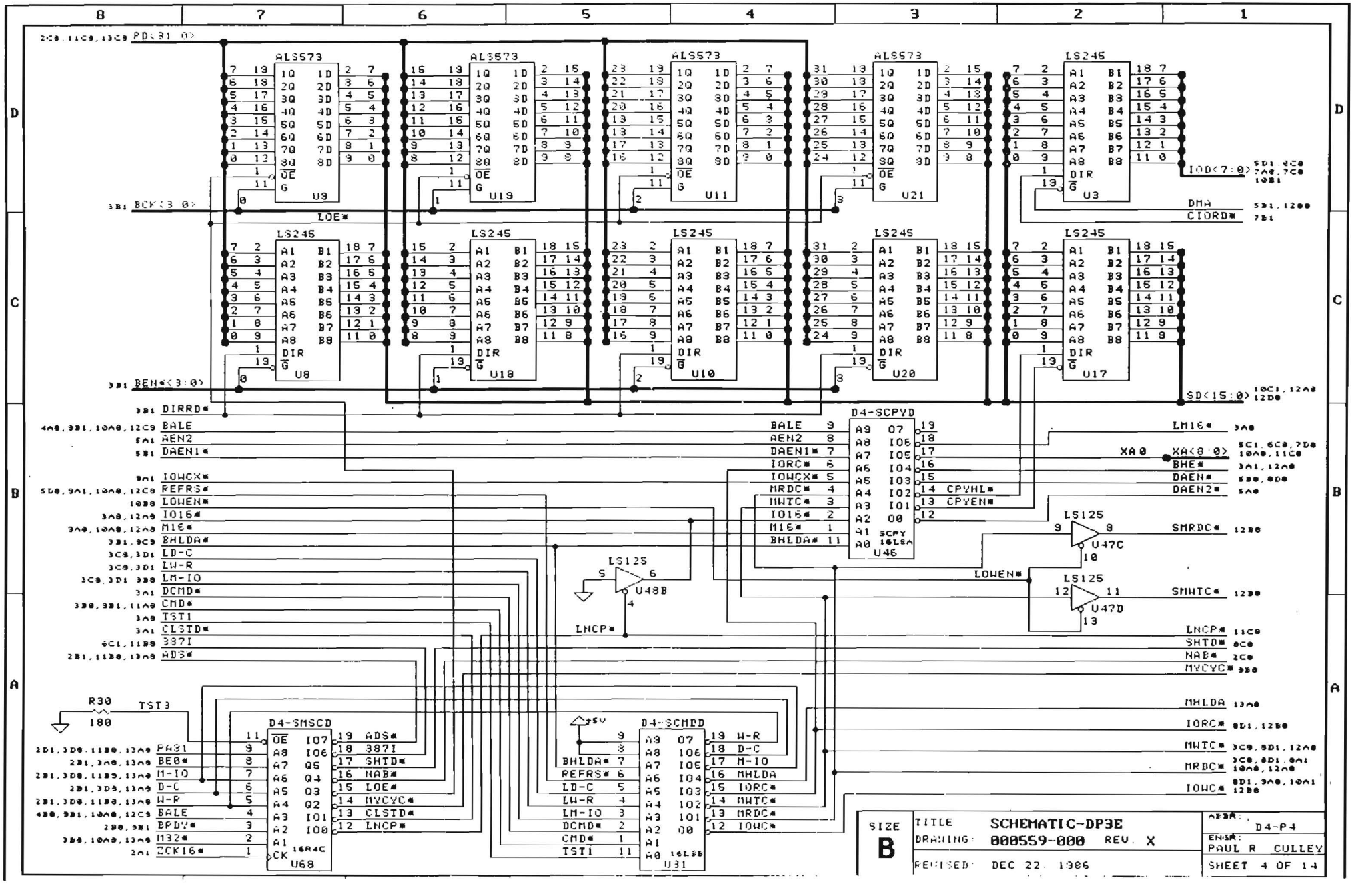
SIZE	CODE IDENT NO	DRAWING NO.	REV
B	1716	000559-000	X

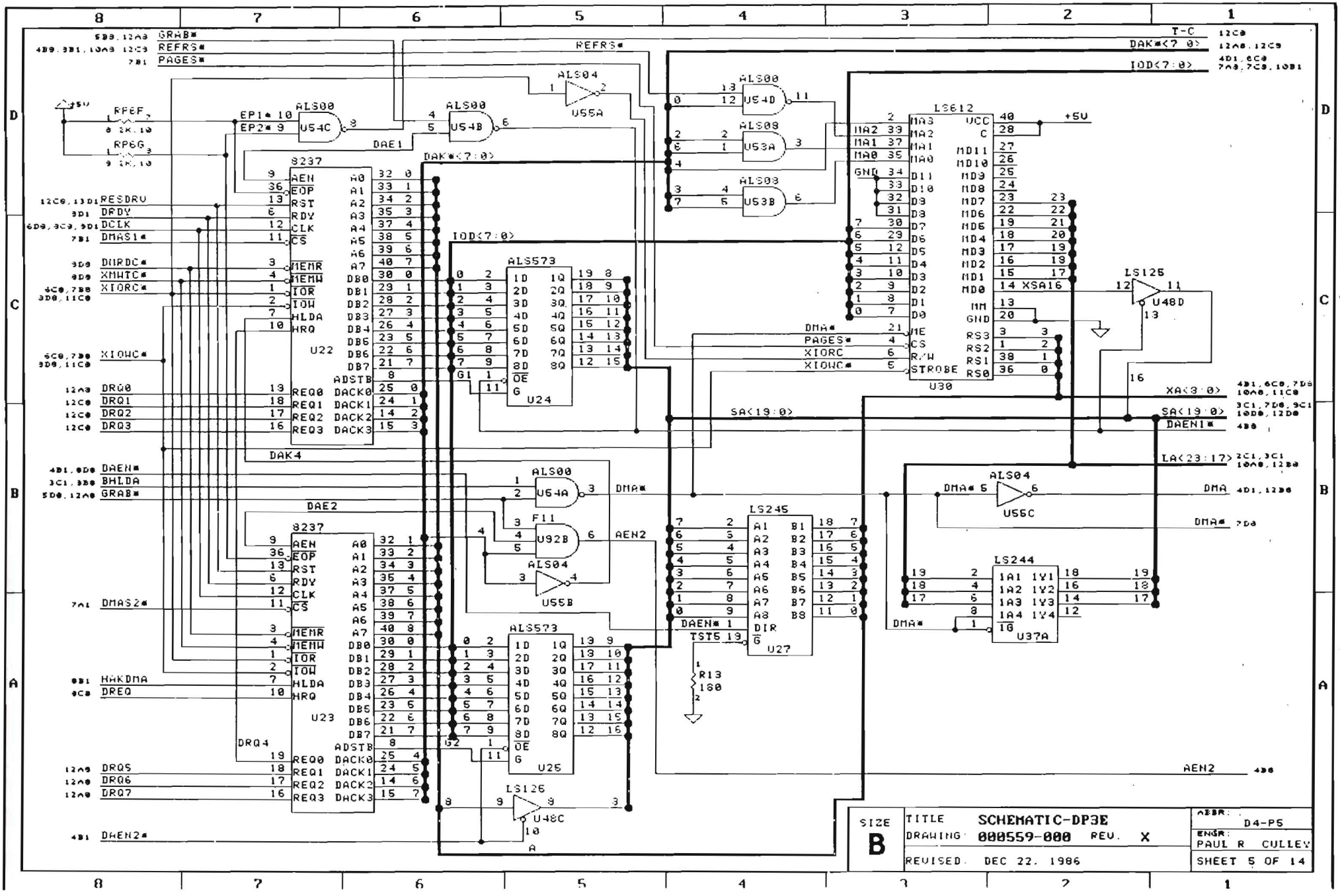
REVISED: DEC 22, 1986 SHEET 1 OF 14

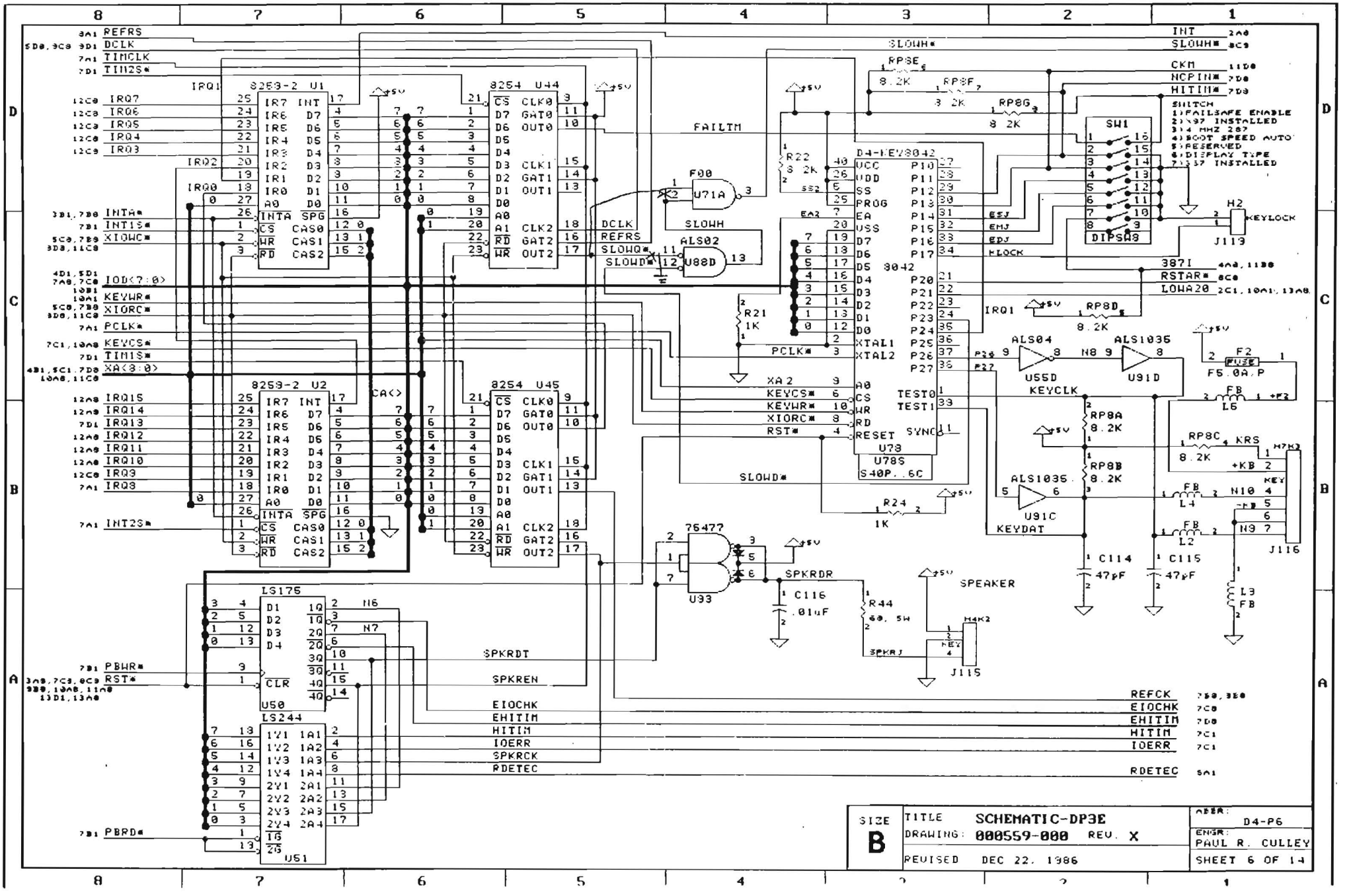
REFERENCE DESIGNATOR		APPLICATION	
HIGHEST USED	NOT USED	NEXT ASSY	USED ON

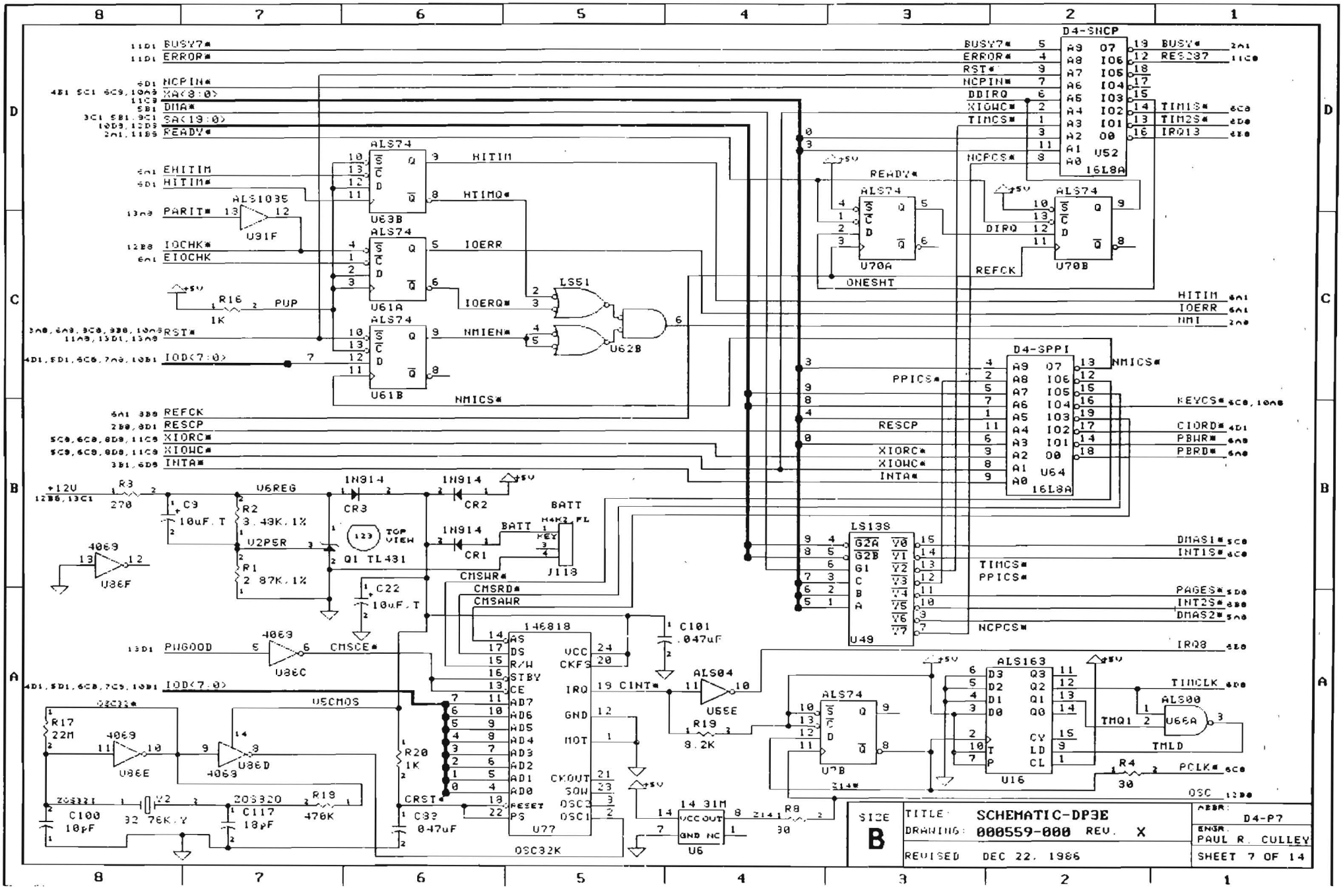

U76
S132P
80386-16
U76
PD<31:0>
PEREQ
R14
20K
PA31
LA<23:17>
LOWA20
F257
U69
NAM#
NAB#
F08
U73B
NAT#
R31
68
MRDY#
BRDY#
CRDY#
F11
U92A
TRDY#
R33
68
HRQCP
F74
U84B
RESCPU
RESCPU#
RESCP
CLK16
F175
U74D
NA#
READY#
HOLD
RESCPU
INT
NMI
PCLK32
HC125
U75C
ZAC32
ZPC32
R37
51
U75D
ZCC32
R36
68
U75A
ZCK32
R38
68
U75B
TST32
R42
180
R40
10K
R39
10K
32.00M
U86
ZC32
C37
.001uF
F74
U69A
CLK16
ZCK16#
R34
22
ZCK16
R35
22
CLK16#
CCLK32
CLK32
PA<23:2>
BE3#
BE2#
BE1#
BE0#
W-R
D-C
M-IO
ADS#
HLDA
BUSY#
ERR386#
SIZE
B
TITLE SCHEMATIC-DP3E
DRAWING 000559-000 REV. X
REVISED DEC 22, 1986
ABBR: D4-P2
ENGR: PAUL R. CULLEY
SHEET 2 OF 14

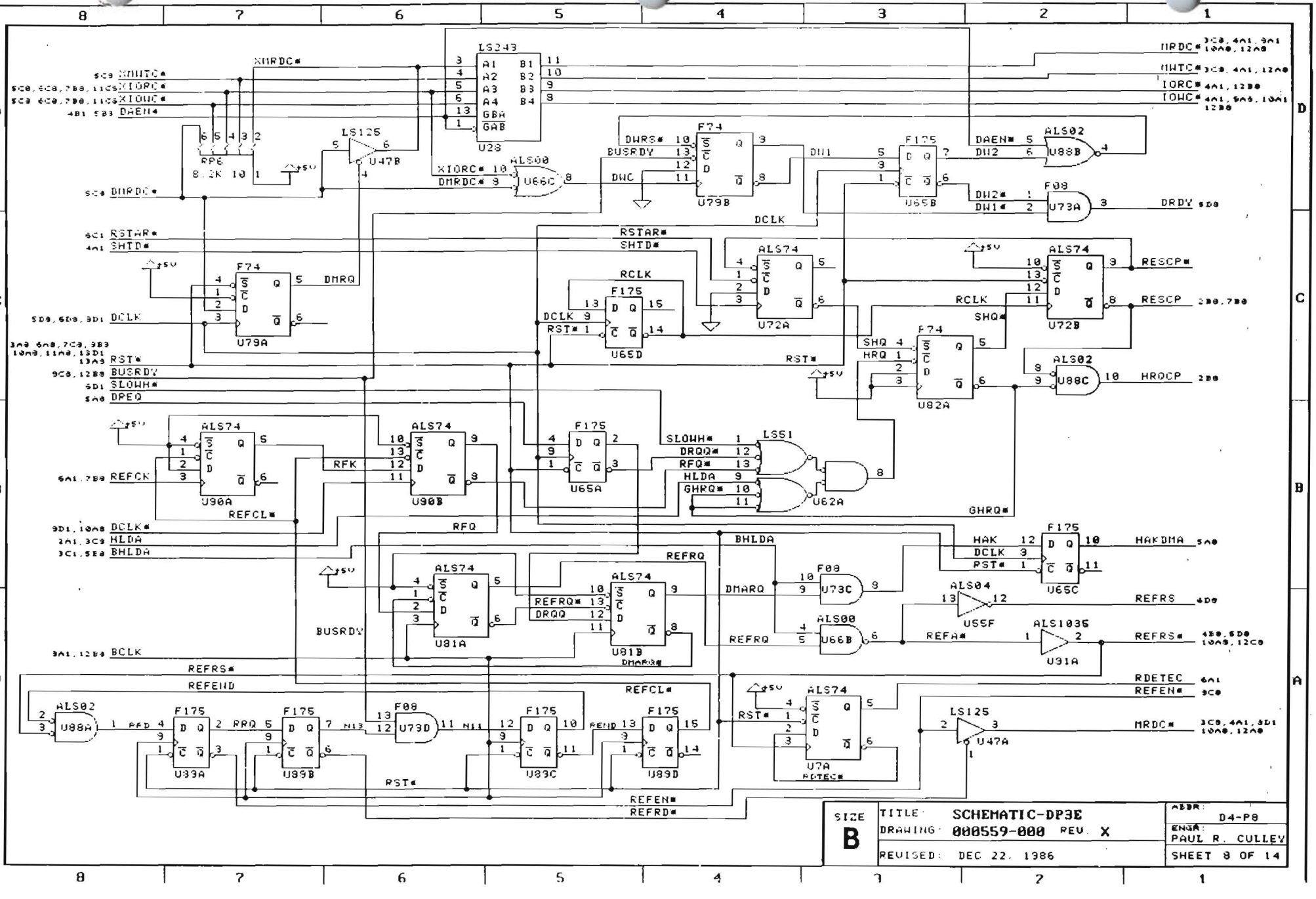

M-IO
D-C
W-R
PA<23:2>
LS245
U33
ALS573
U39
U34
U35
R10
180
R12
1K
R11
180
LA<23:17>
SA<19:0>
BHLDA
ALE
HLDA
HOLD
BHLDA*
ALS00
U66D
F00
U71C
MWTC*
MRDC*
LM-IO
LD-C
LW-R
MDEN*
M32*
CMD*
LS244
U40
U41
D4-SDEND
U32
D4-SADI
U38
INTA*
DIRRD*
BEN*<3:0>
BCK<3:0>
BHE*
SA0
SA1
TST1
CX16*
BE3*
BE2*
BE1*
BE0*
D4-SADOD
U58
CLAST*
CLSTD*
ALST
DCMD*
RST*
IO16*
LM16*
T10
T00
ALE
CK
SIZE
B
TITLE: SCHEMATIC-DP3E
DRAWING 000559-000 REV. X
REVISED DEC 22, 1986
ABBR: D4-P3
ENGR: PAUL R. CULLEY
SHEET 3 OF 14


8
7
6
5
4
3
2
1
D
C
B
A
PD<31:0>
ALS573
U9
U19
U11
U21
LS245
U3
IOD<7:0>
DMA
CIORD#
BCK<3:0>
LOE#
U8
U18
U10
U20
U17
SD<15:0>
BEN#<3:0>
DIRRD#
BALE
AEN2
DAEN1#
IOWCX#
REFRS#
LOWEN#
IO16#
M16#
BHLDA#
LD-C
LW-R
LM-IO
DCMD#
CMD#
TST1
CLSTD#
387I
ADS#
D4-SCPYD
U46
LM16#
XA<8:0>
XA0
BHE#
DAEN#
DAEN2#
LS125
U47C
U47D
U48B
SMRDC#
SMWTC#
LOWEN#
LNCP#
SHTD#
NAB#
MYCYC#
MHLDA
IORC#
MWTC#
MRDC#
IOWC#
R30
180
TST3
D4-SMSCD
U68
D4-SCMDD
U31
+5V
PA31
BE0#
M-IO
D-C
W-R
BALE
BPDV#
M32#
ZCK16#
ADS#
387I
SHTD#
NAB#
LOE#
MYCYC#
CLSTD#
LNCP#
BHLDA#
REFRS#
LD-C
LW-R
LM-IO
DCMD#
CMD#
TST1
SIZE
B
TITLE
SCHEMATIC-DP3E
DRAWING:
000559-000
REV. X
REVISED:
DEC 22, 1986
ASSY:
D4-P4
ENGR:
PAUL R CULLEY
SHEET 4 OF 14

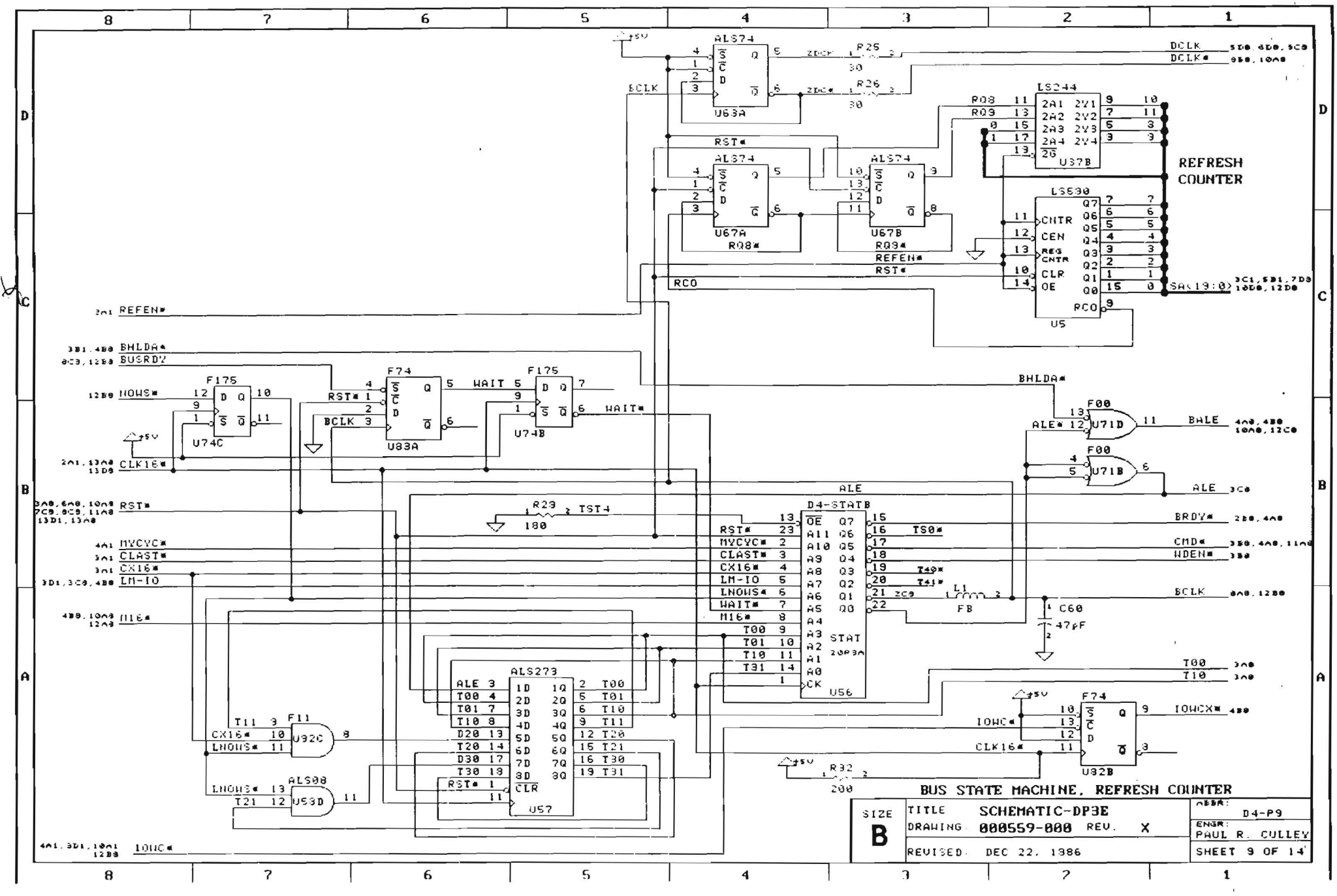

GRAB#
REFRS#
PAGES#
T-C
DAK#<7:0>
IOD<7:0>
+5V
RPEF
RP6G
EP1# 10
EP2# 9
ALS00
U54C
U54B
U54D
U53A
U53B
ALS04
U55A
DAE1
DAK#<7:0>
8237
U22
U23
RESDRV
DRDY
DCLK
DMAS1#
DMRDC#
XMWTC#
XIORC#
XIOWC#
DRQ0
DRQ1
DRQ2
DRQ3
DAK4
DAEN#
BHLDA
GRAB#
DAE2
DMAS2#
HAKDMA
DREQ
DRQ4
DRQ5
DRQ6
DRQ7
DAEN2#
ALS573
U24
U25
IOD<7:0>
LS612
U30
DMA#
PAGES#
XIORC
XIOWC#
LS125
U48D
XA<3:0>
SA<19:0>
DAEN1#
LA<23:17>
DMA
ALS00
U54A
F11
U92B
ALS04
U55B
AEN2
LS245
U27
DAEN# 1
TST5 19
R13
180
ALS04
U55C
LS244
U37A
U48C
AEN2
SIZE
B
TITLE SCHEMATIC-DP3E
DRAWING 000559-000 REV. X
REVISED DEC 22, 1986
ABBR: D4-P5
ENGR: PAUL R CULLEY
SHEET 5 OF 14


REFRS
DCLK
TIMCLK
TIM2S#
IRQ1
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
IRQ2
IRQ0
8259-2 U1
8254 U44
INTA#
INT1S#
XIOWC#
IOD<7:0>
KEYWR#
XIORC#
PCLK#
KEYCS#
TIM1S#
XA<8:0>
IRQ15
IRQ14
IRQ13
IRQ12
IRQ11
IRQ10
IRQ9
IRQ8
8259-2 U2
8254 U45
CA<>
INT2S#
FAILTM
F00
U71A
SLOWH
ALS02
U88D
SLOWD#
DCLK
REFRS
SLOWH#
R22
8.2K
R21
1K
D4-KEY8042
U78
U78S
S40P..6C
XA2
KEYCS#
KEYWR#
XIORC#
RST#
PCLK#
R24
1K
SLOWD#
RP8E
8.2K
RP8F
8.2K
RP8G
8.2K
SW1
DIPSW8
SWITCH
1)FAILSAFE ENABLE
2)387 INSTALLED
3)4.77 MHZ 287
4)BOOT SPEED AUTO
5)RESERVED
6)DISPLAY TYPE
7)387 INSTALLED
H2
KEYLOCK
J119
INT
SLOWH#
CKM
NCPIN#
HITIM#
387I
RSTAR#
LOWA20
IRQ1
RP8D
8.2K
ALS04
U55D
ALS1035
U91D
F2
FUSE
F5.0A,P
KEYCLK
FB
L5
RP8A
8.2K
RP8C
8.2K
KRS
+KB
RP8B
8.2K
ALS1035
U91C
KEYDAT
FB
L4
FB
L2
C114
47pF
C115
47pF
L3
FB
J116
76477
U33
SPKRDR
C116
.01uF
R44
SPEAKER
J115
LS175
U50
LS244
U51
N6
N7
PBWR#
RST#
PBRD#
SPKRDT
SPKREN
EIOCHK
EHITIM
HITIM
IOERR
SPKRCK
RDETEC
REFCK
EIOCHK
EHITIM
HITIM
IOERR
RDETEC
SIZE
B
TITLE SCHEMATIC-DP3E
DRAWING: 000559-000 REV. X
REVISED DEC 22, 1986
ABER: D4-P6
ENGR: PAUL R. CULLEY
SHEET 6 OF 14


D4-SNCP
D4-SPPI
ALS74
LS138
ALS163
ALS04
ALS00
LS51
146818
OSC32K
BUSY7*
ERROR*
NCPIN*
XA<8:0>
DMA*
SA<19:0>
READY*
EHITIM
HITIM*
PARIT*
IOCHK*
EIOCHK
RST*
IOD<7:0>
REFCK
RESCP
XIORC*
XIOWC*
INTA*
HITIM
IOERR
NMI
NMICS*
PPICS*
KEYCS*
CIORD*
PBWR*
PBRD*
DMAS1*
INT1S*
TIMCS*
PAGES*
INT2S*
DMAS2*
IRQ8
TIMCLK
TMLD
PCLK*
OSC
NCPCS*
DIRQ
ONESHT
TIM1S*
TIM2S*
IRQ13
RES287
CMSHR*
CMSRD*
CMSWR
CMSCE*
PWGOOD
CINT*
USCMOS
CRST*
BATT
+12V
+5V
SIZE
B
TITLE: SCHEMATIC-DP3E
DRAWING: 000559-000 REV. X
REVISED DEC 22, 1986
ABBR: D4-P7
ENGR: PAUL R. CULLEY
SHEET 7 OF 14



SIZE	TITLE: SCHEMATIC-DP3E	ADDR: D4-P8
B	DRAWING: 000559-000 REV. X	ENGR: PAUL R. CULLEY
	REVISED: DEC 22, 1986	SHEET 8 OF 14


REFRESH COUNTER
BUS STATE MACHINE, REFRESH COUNTER
SIZE B
TITLE SCHEMATIC-DP3E
DRAWING 000559-000 REV. X
REVISED DEC 22, 1986
ENGR: PAUL R. CULLEY
SHEET 9 OF 14
D4-P9
REFEN#
BHLDA#
BUSRDY
NOWS#
RST#
MYCYC#
CLAST#
CX16#
LM-IO
M16#
IOWC#
BCLK
DCLK
DCLK#
ALE
BALE
BRDY#
CMD#
WDEN#
IOWCX#
WAIT#
TS0#
RCO
REFEN#
RST#
RQ08#
RQ09#
SA<19:0>
U5
U37B
U67A
U67B
U74B
U74C
U83A
U56
U57
U71B
U71D
U92C
U93D
U82B
C60
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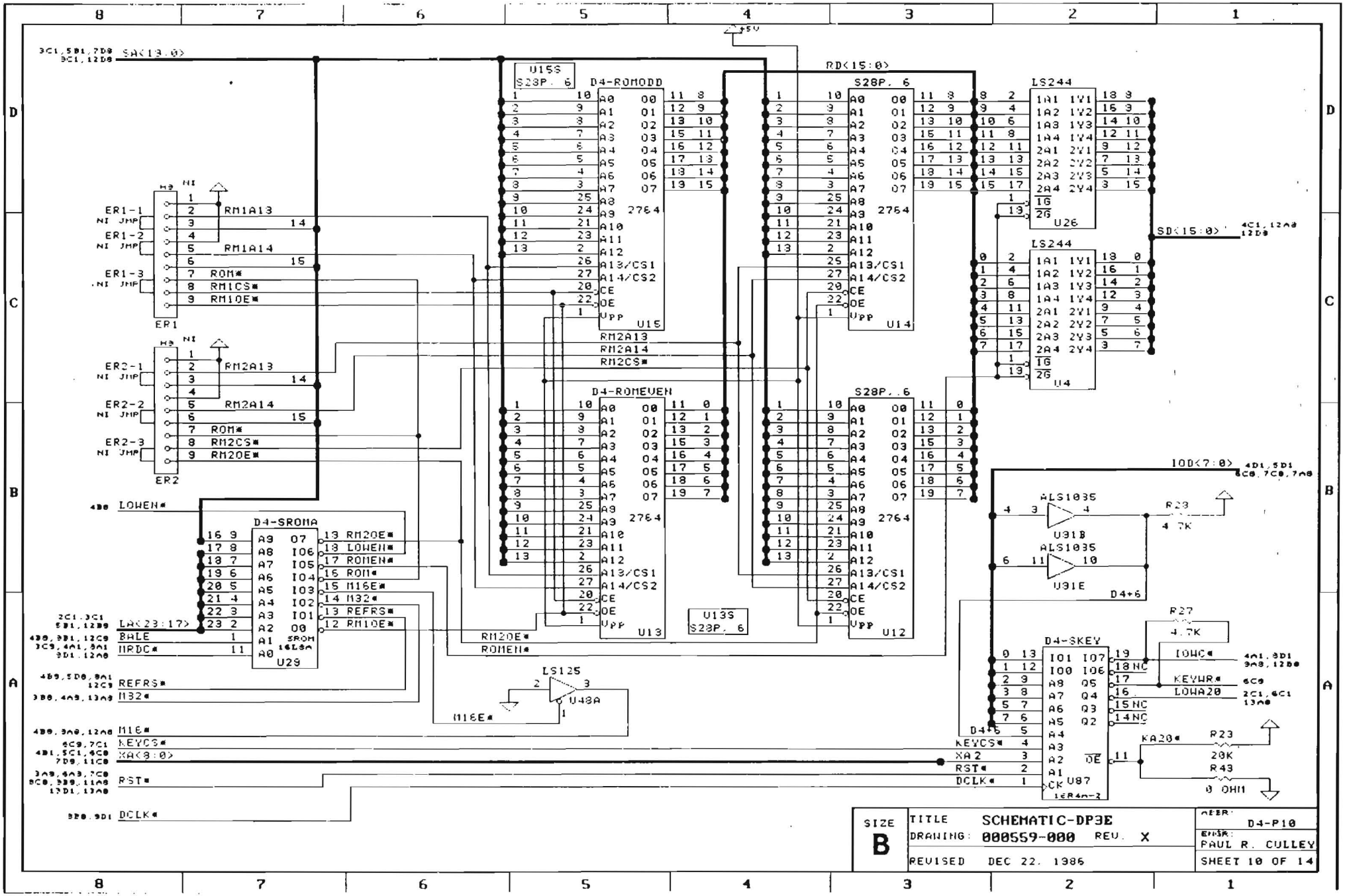
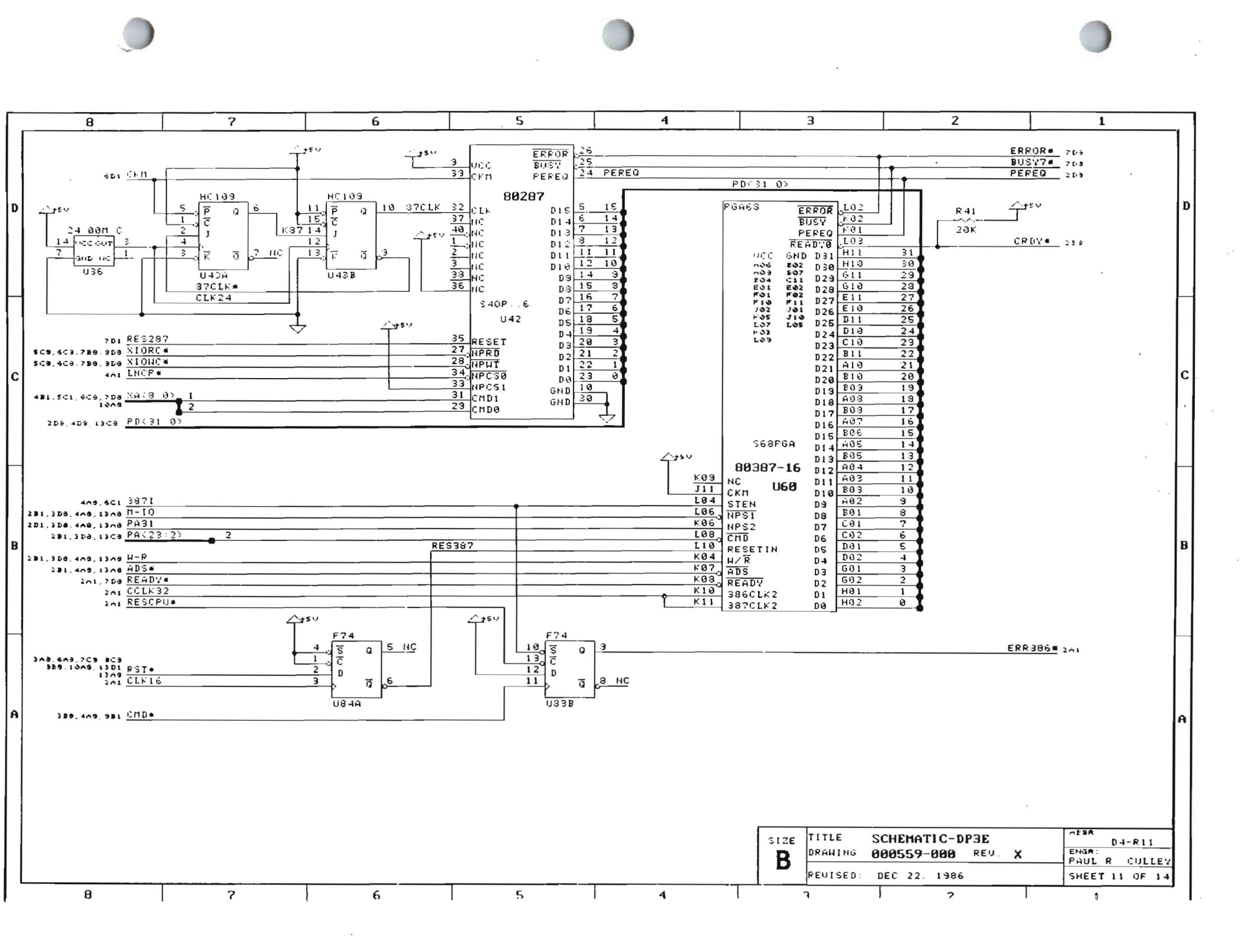
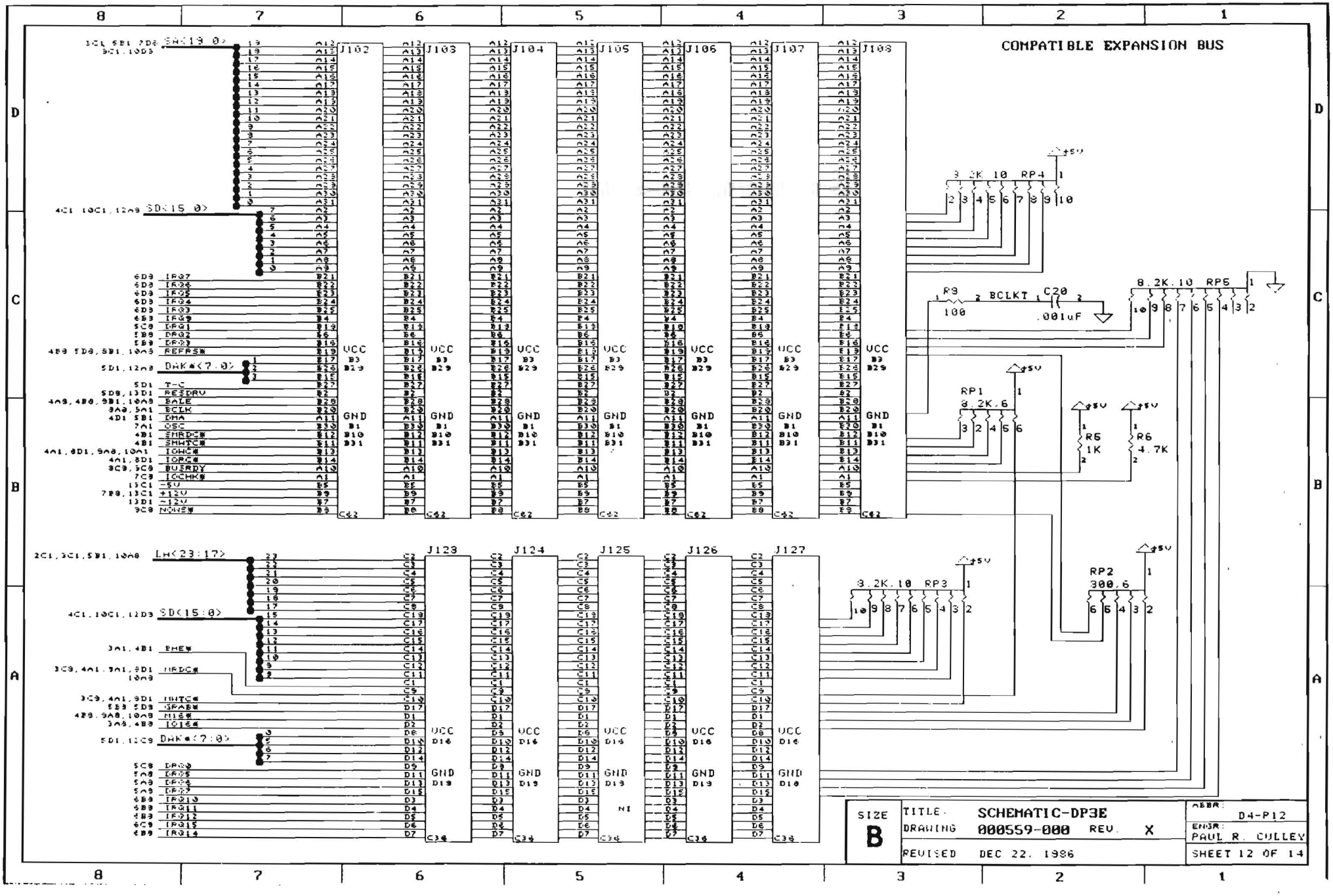
L1
FB
R25
R26
R29
R32
30
30
180
200

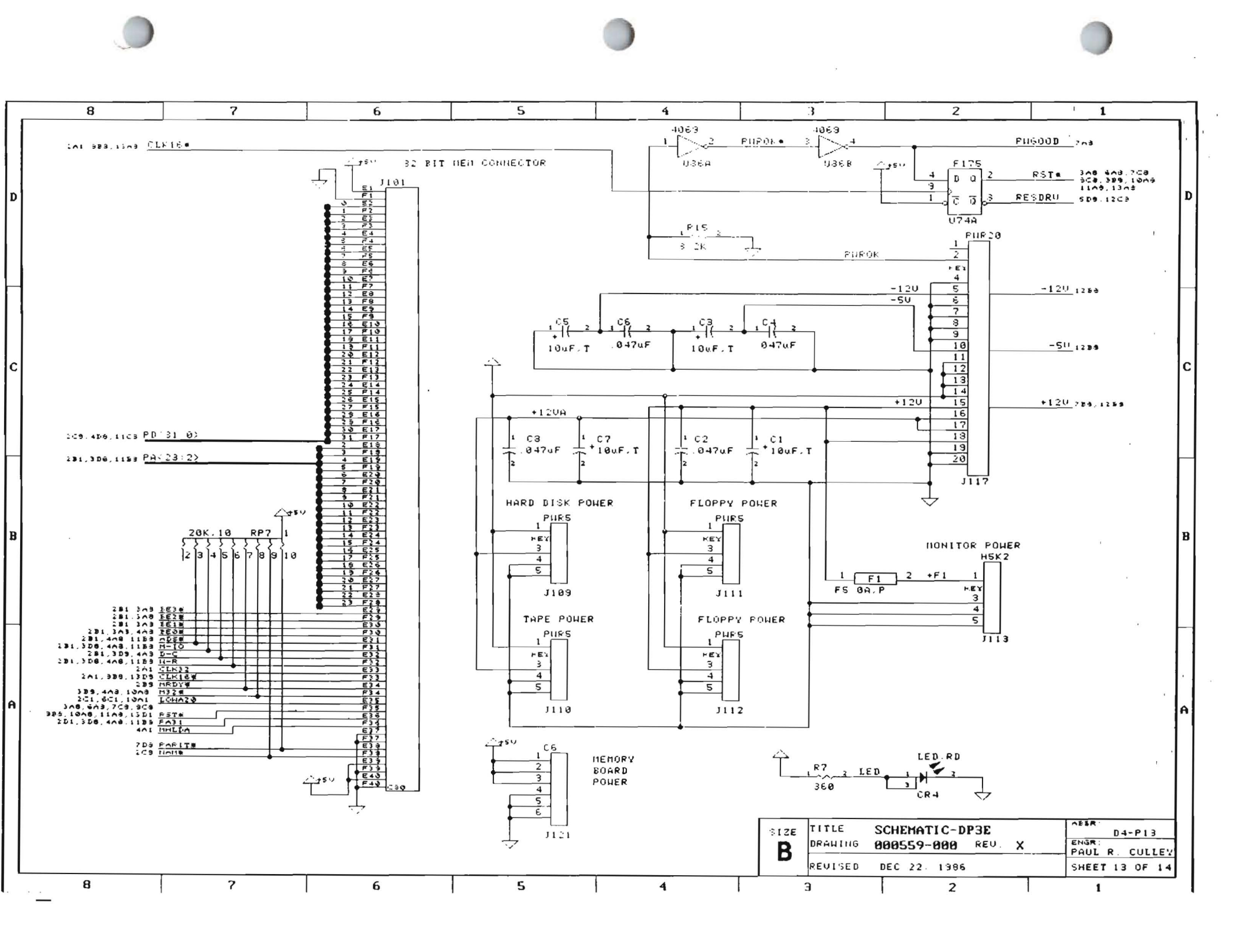


SIZE	TITLE	SCHEMATIC-DP3E	
B	DRAWING:	000559-000 REV. X	D4-P10
	REVISED	DEC 22, 1986	PAUL R. CULLEY
			SHEET 10 OF 14

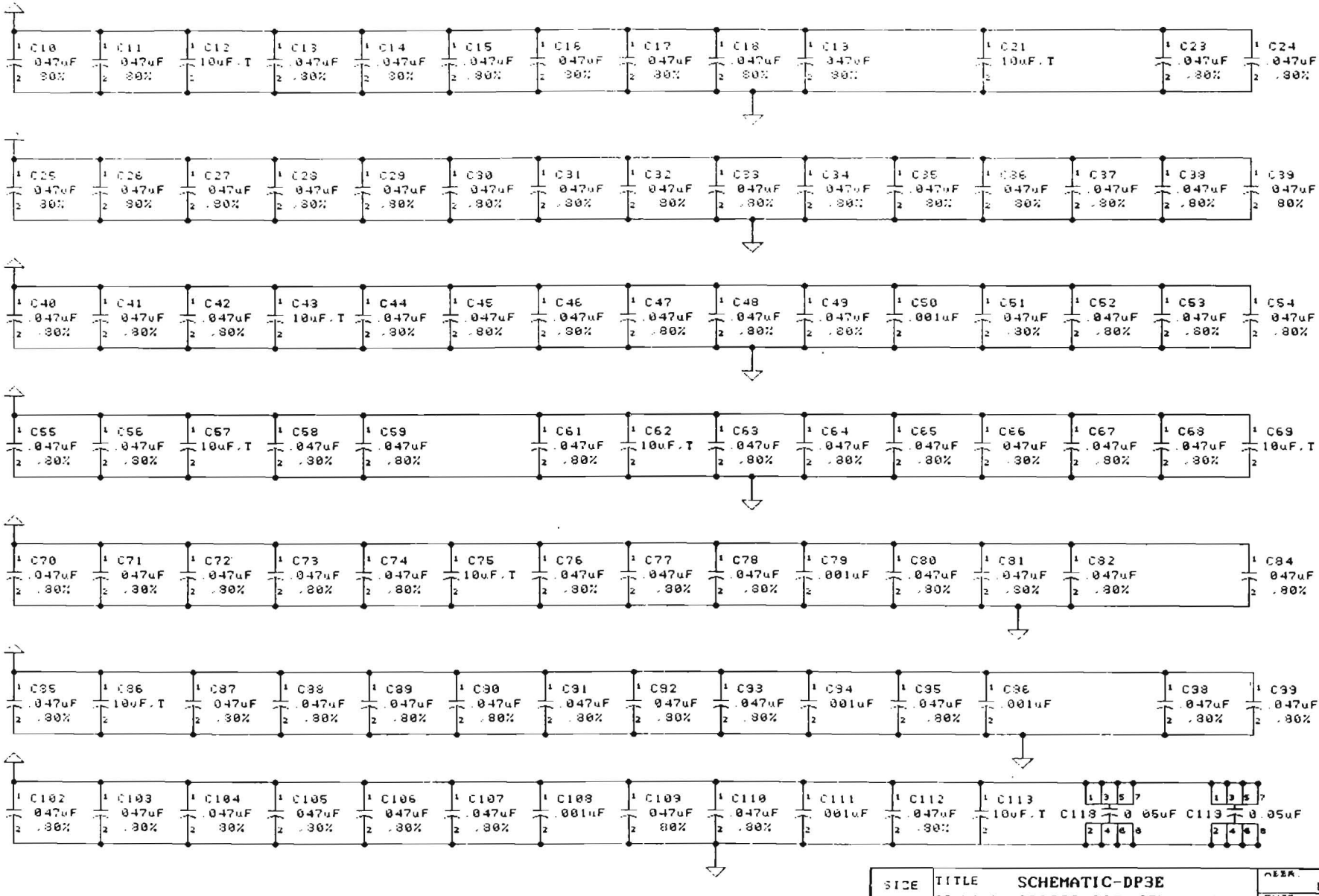

80287
U42
S40P..6
80387-16
U60
S68PGA
PGA68
HC109
U43A
U43B
24.00M C
U36
F74
U84A
U83B
R41
20K
PD<31:0>
RES387
ERROR
BUSY
PEREQ
READY
CKM
CLK24
37CLK
RESET
NPRD
NPWT
NPCS0
NPCS1
CMD1
CMD0
NC
STEN
NPS1
NPS2
CMD
RESETIN
ADS
386CLK2
387CLK2
RST
CLK16
CMD
ERR386
CRDY
SIZE
B
TITLE SCHEMATIC-DP3E
DRAWING 000559-000 REV. X
REVISED: DEC 22, 1986
DES: D4-R11
ENGR: PAUL R CULLEY
SHEET 11 OF 14



SIZE B	TITLE: SCHEMATIC-DP3E		ABBR: D4-P12
	DRAWING 000559-000	REV. X	ENGR: PAUL R. CULLEY
	REVISED DEC 22, 1986		SHEET 12 OF 14



SIZE B	TITLE SCHEMATIC-DP3E	ASSR: D4-P13
	DRAWING 000559-000 REV. X	ENGR: PAUL R. CULLEY
	REVISED DEC 22, 1986	SHEET 13 OF 14



THESE CAPACITORS SHOULD BE EVENLY DISTRIBUTED ABOUT THE BOARD WITH THE .047 AND 10uF VALUES MIXED UP

SIZE B	TITLE SCHEMATIC-DP3E	DES: D4-P14
	DRAWING 000559-000 REV. X	ENGR: PAUL R CULLEY
	REVISED: DEC 22, 1986	SHEET 14 OF 14

8	7	6	5	4	3	2	1

PCB PART NUMBER: 000415
ASSY PART NUMBER: 000413

APPROVALS	DATE
DRAWN: PAUL R. CULLEY	
CHECKED	
COG ENGR	
ENGR	
ENGR	
MFG	
QA	
OTHER	
OTHER	

COMPAQ™ COMPUTER CORPORATION

TITLE:

D4 PAGE DRAM BOARD SCHEMATIC

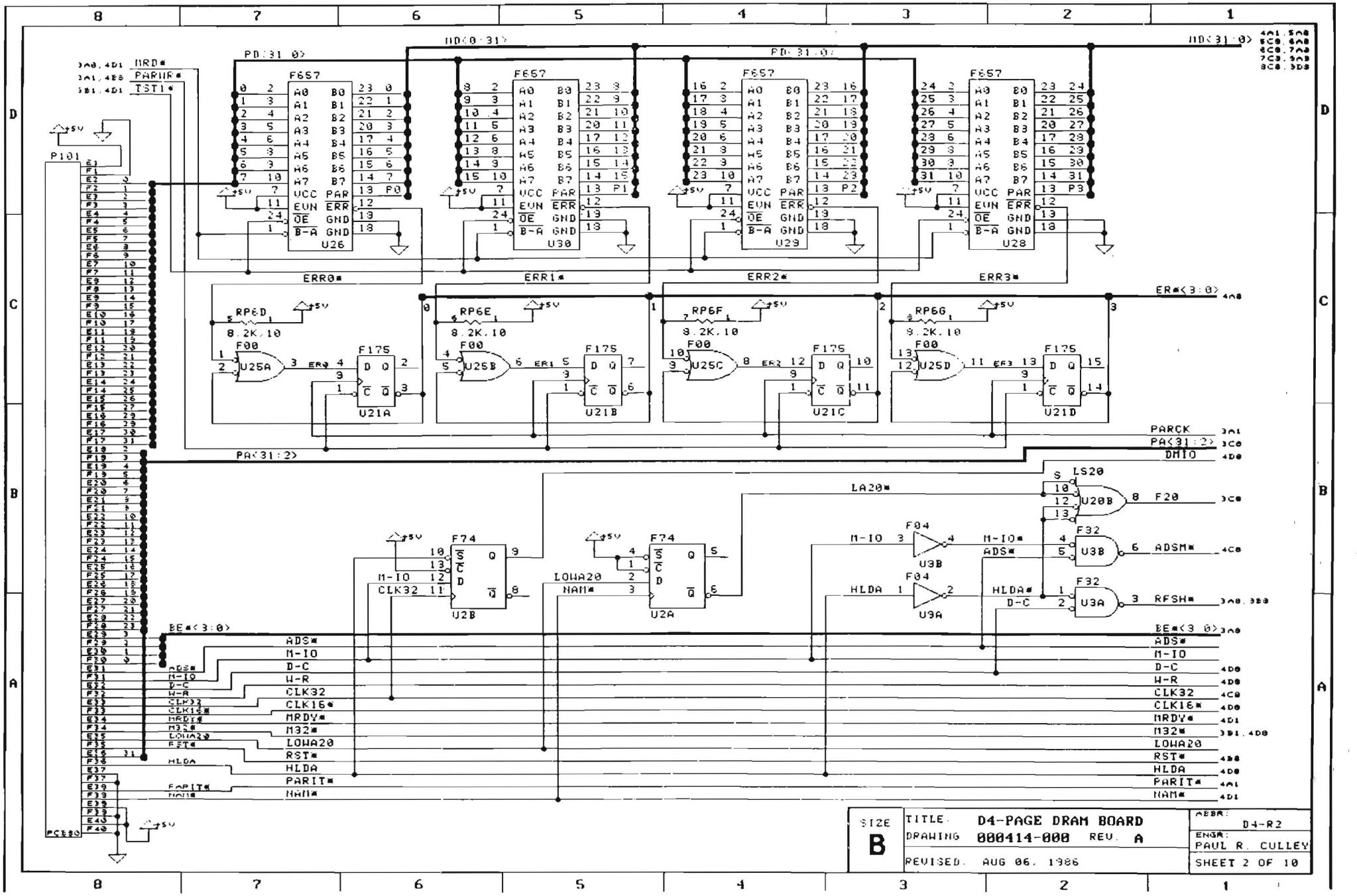
SIZE	CODE IDENT NO	DRAWING NO.	REV
B	1716	000414-000	A

REVISED AUG 06, 1986 — SHEET 1 OF 10

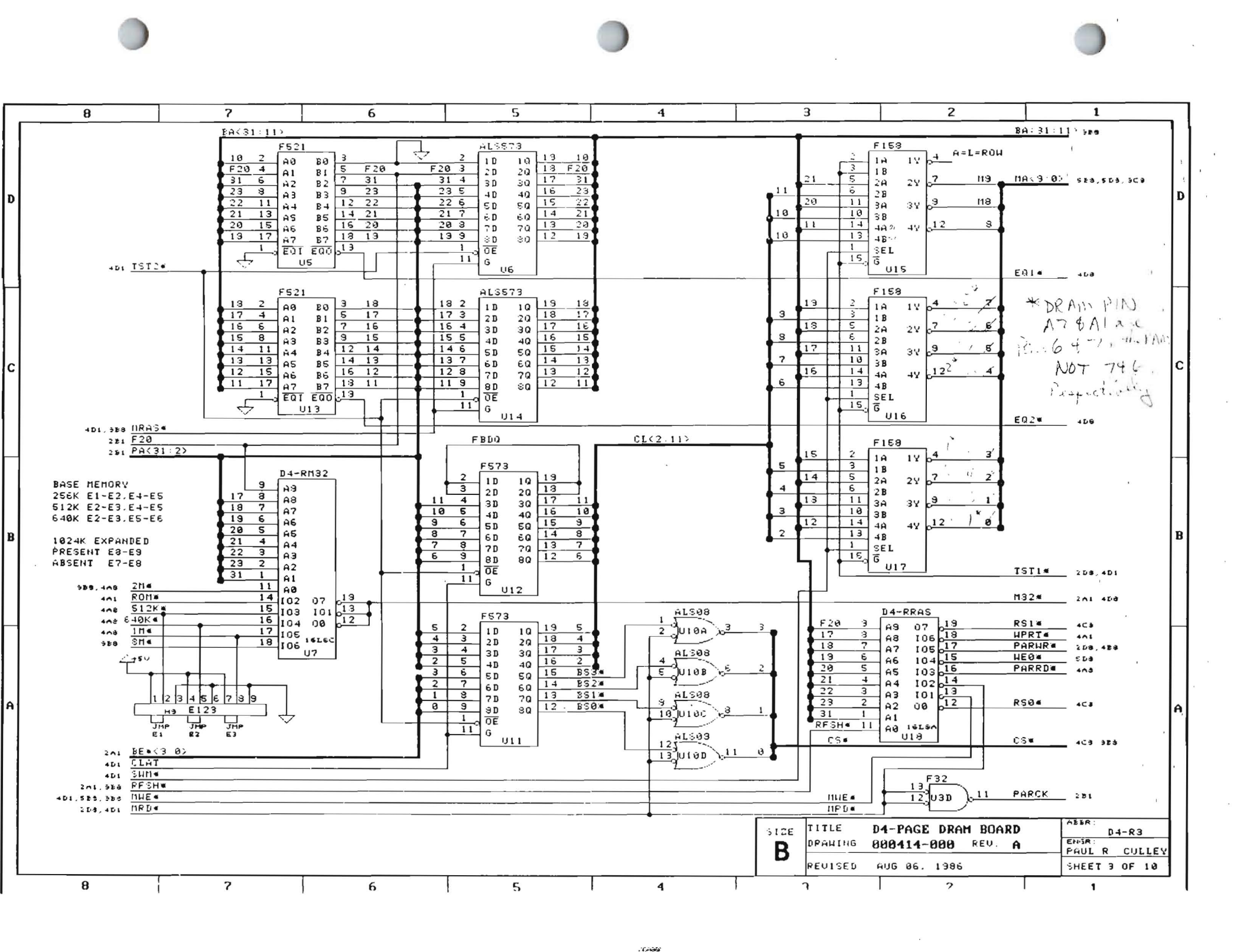
HIGHEST USED	NOT USED	NEXT ASSY	USED ON

REFERENCE DESIGNATOR — APPLICATION

8	7	6	5	4	3	2	1



SIZE B	TITLE: D4-PAGE DRAM BOARD	ABBR: D4-R2
	DRAWING 000414-000 REV. A	ENGR: PAUL R. CULLEY
	REVISED: AUG 06, 1986	SHEET 2 OF 10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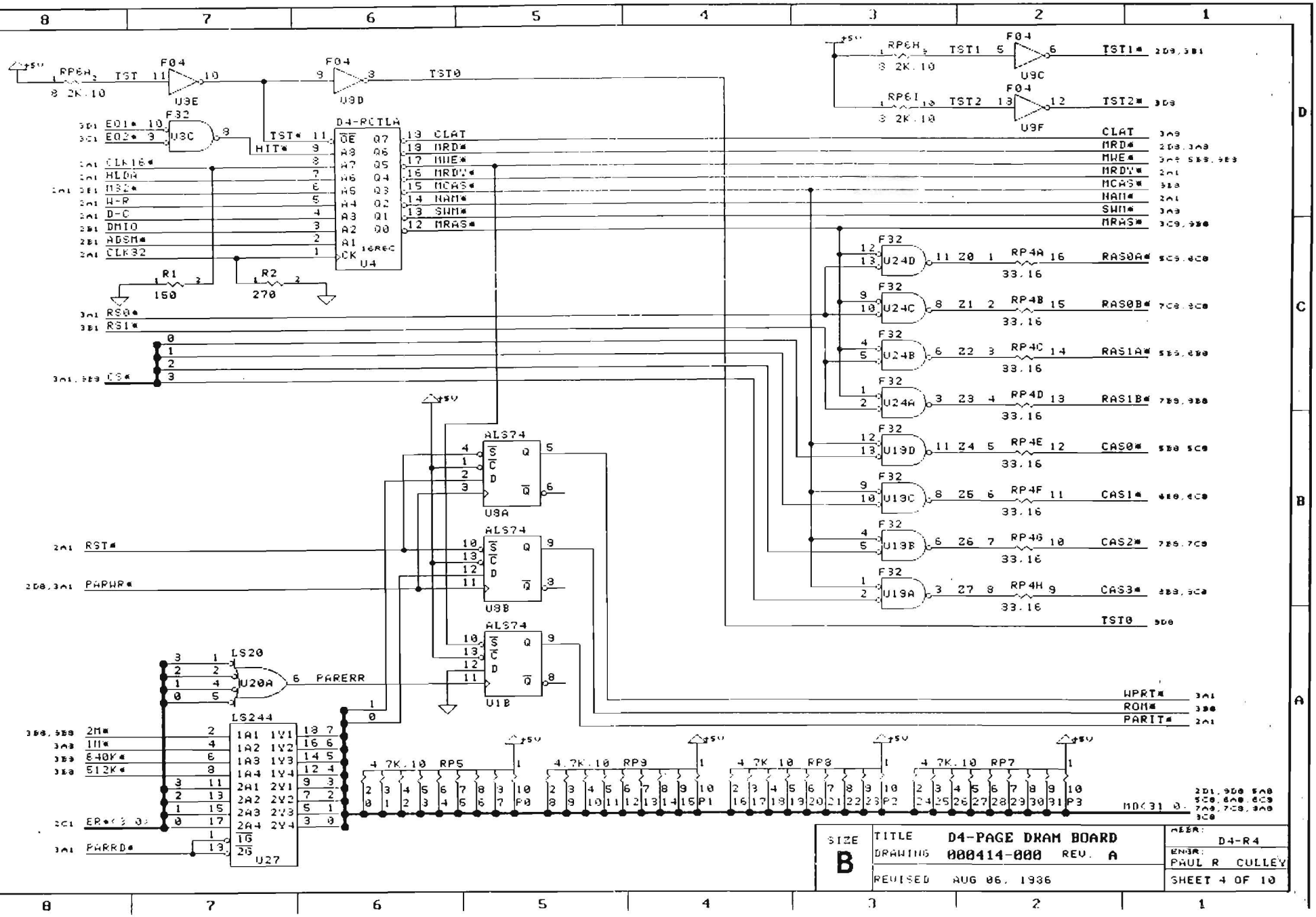
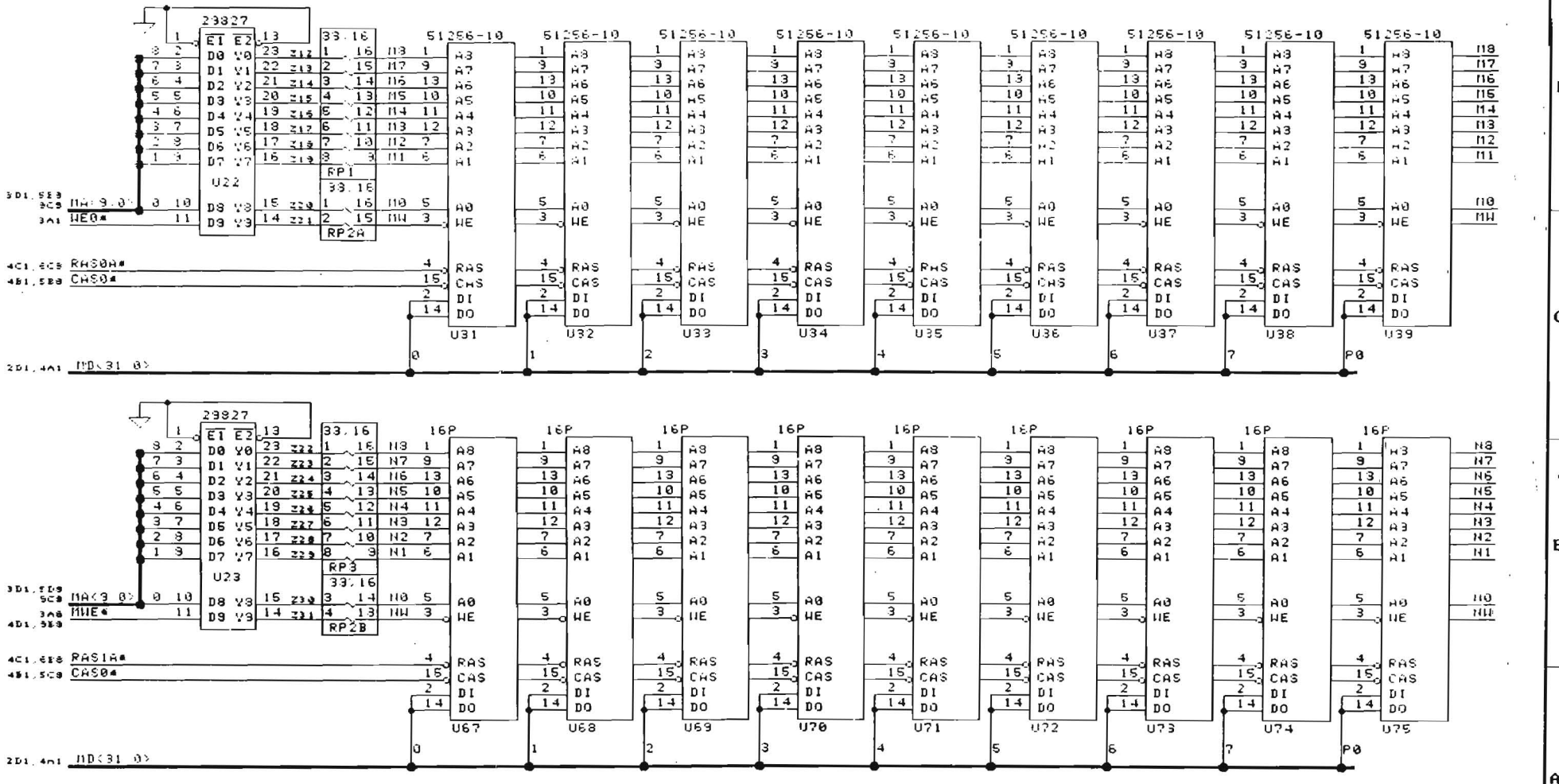
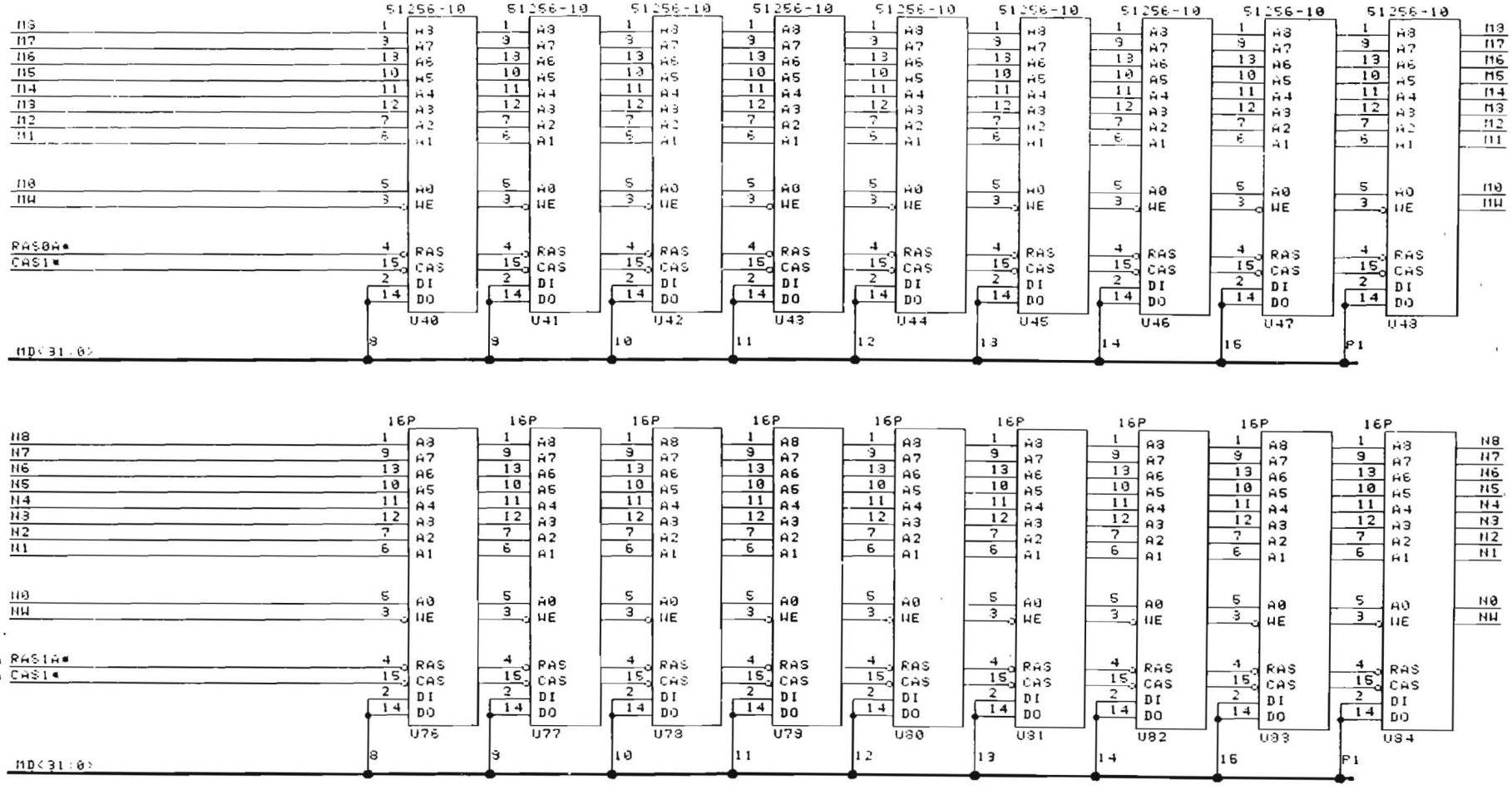
F521
U5
U13
AL3573
U6
U14
F158
U15
U16
U17
A=L=ROW
MA<9:0>
EQ1*
EQ2*
TST1*
M32*
TST2*
MRAS*
F20
PA<31:2>
FBDQ
F573
U12
U11
D4-RM32
U7
BASE MEMORY
256K E1-E2,E4-E5
512K E2-E3,E4-E5
640K E2-E3,E5-E6
1024K EXPANDED
PRESENT E8-E9
ABSENT E7-E8
2M*
ROM*
512K*
640K*
1M*
8M*
+5V
H9
E123
JMP E1
JMP E2
JMP E3
CL<2.11>
ALS08
U10A
U10B
U10C
ALS03
U10D
BS3*
BS2*
BS1*
BS0*
D4-RRAS
U18
RS1*
WPRT*
PARWR*
WE0*
PARRD*
RS0*
CS*
RFSH*
F32
U3D
PARCK
BE*<3 0>
CLAT
SWM*
RFSH*
MWE*
MRD*
SIZE
B
TITLE
D4-PAGE DRAM BOARD
DRAWING
000414-000
REV. A
REVISED
AUG 06, 1986
ABBR:
D4-R3
ENGR:
PAUL R CULLEY
SHEET 3 OF 10

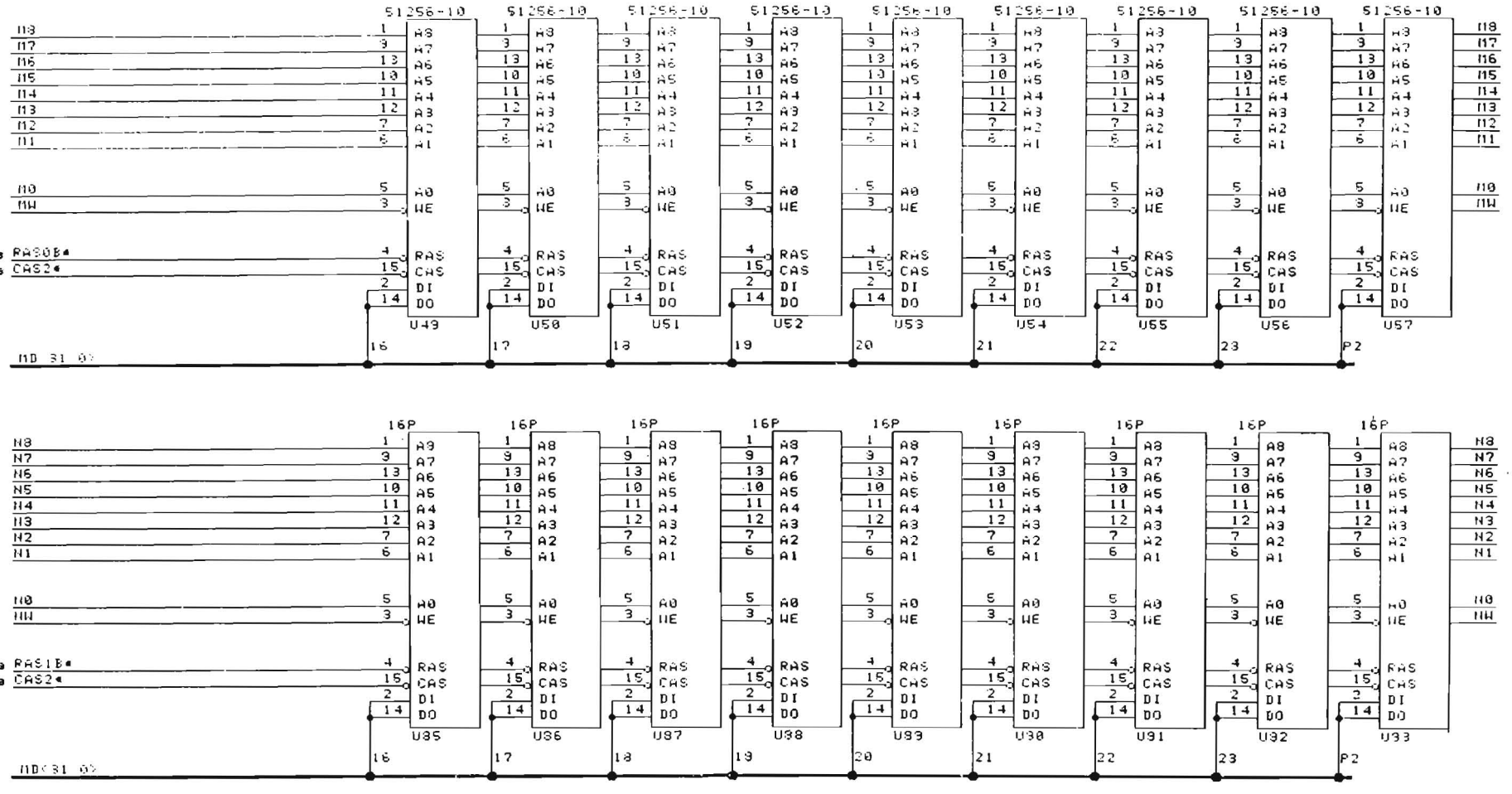

RP6H 8 2K.10
TST
F04 U3E
F04 U3D
TST0
F32 U3C
EQ1* EQ2*
HIT*
D4-RCTLR U4
TST*
CLK16*
HLDA
MS2*
W-R
D-C
DMIO
ADSM*
CLK32
CLAT
MRD*
MWE*
MRD'W*
MCAS*
NAM*
SWM*
MRAS*
R1 150
R2 270
RS0*
RS1*
CS*
RP6H TST1 F04 U9C TST1*
RP6I TST2 F04 U9F TST2*
F32 U24D RP4A 33.16 RAS0A*
F32 U24C RP4B 33.16 RAS0B*
F32 U24B RP4C 33.16 RAS1A*
F32 U24A RP4D 33.16 RAS1B*
F32 U19D RP4E 33.16 CAS0*
F32 U19C RP4F 33.16 CAS1*
F32 U19B RP4G 33.16 CAS2*
F32 U19A RP4H 33.16 CAS3*
TST0
ALS74 U8A
ALS74 U8B
ALS74 U1B
RST*
PAPWR*
LS20 U20A PARERR
LS244 U27
2M*
1M*
640K*
512K*
ER*
PARRD*
WPRT*
ROM*
PARIT*
4.7K.10 RP5
4.7K.10 RP9
4.7K.10 RP8
4.7K.10 RP7
MD<31:0>
SIZE B
TITLE D4-PAGE DRAM BOARD
DRAWING 000414-000 REV. A
REVISED AUG 06, 1986
D4-R4
PAUL R CULLEY
SHEET 4 OF 10



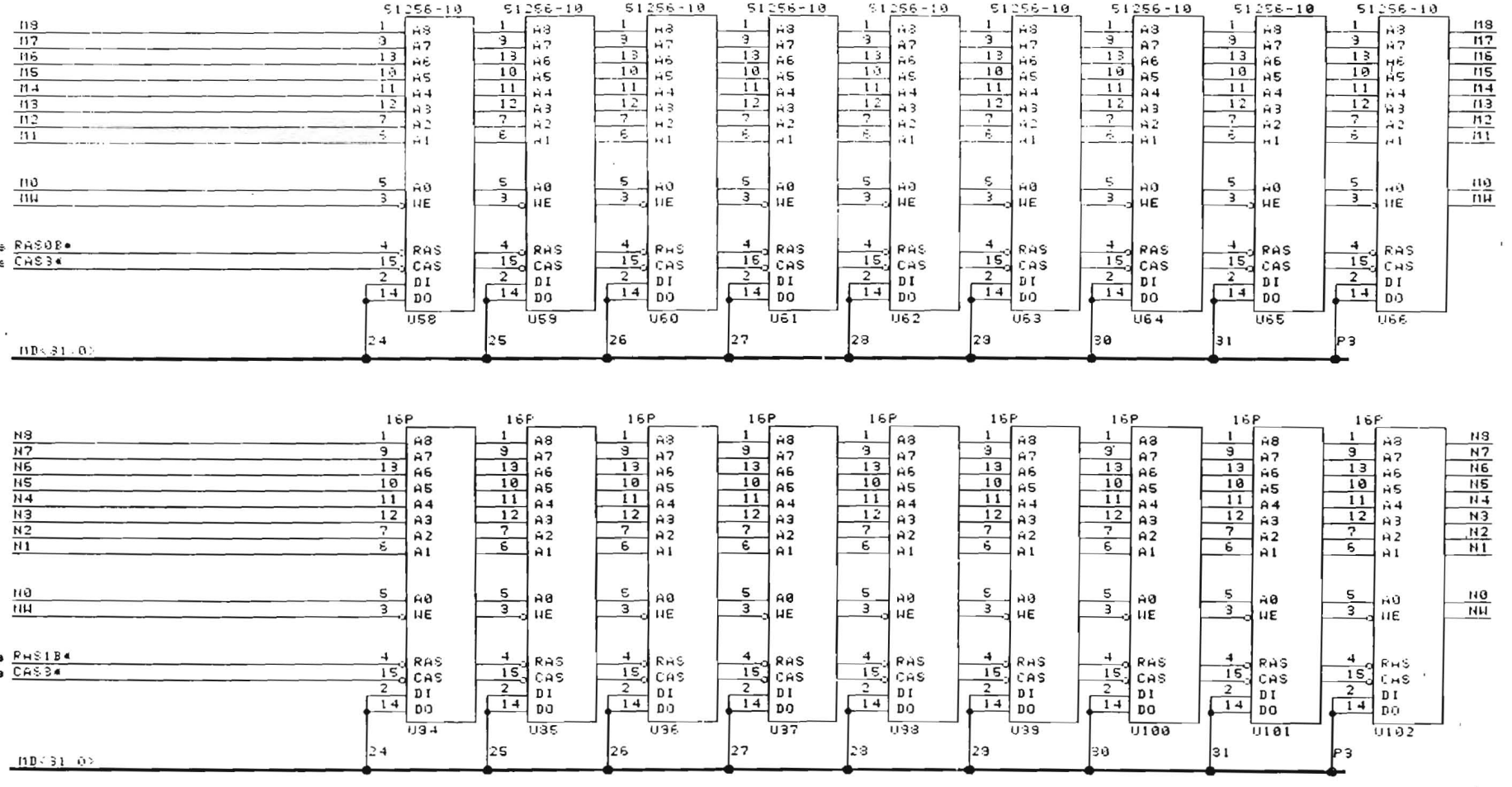
SIZE	TITLE: D4-PAGE DRAM BOARD	ASSY D4-RS
B	DRAWING: 000414-000 REV. A	ENGR: PAUL R. CULLEY
	REVISED: AUG 06, 1986	SHEET 5 OF 10



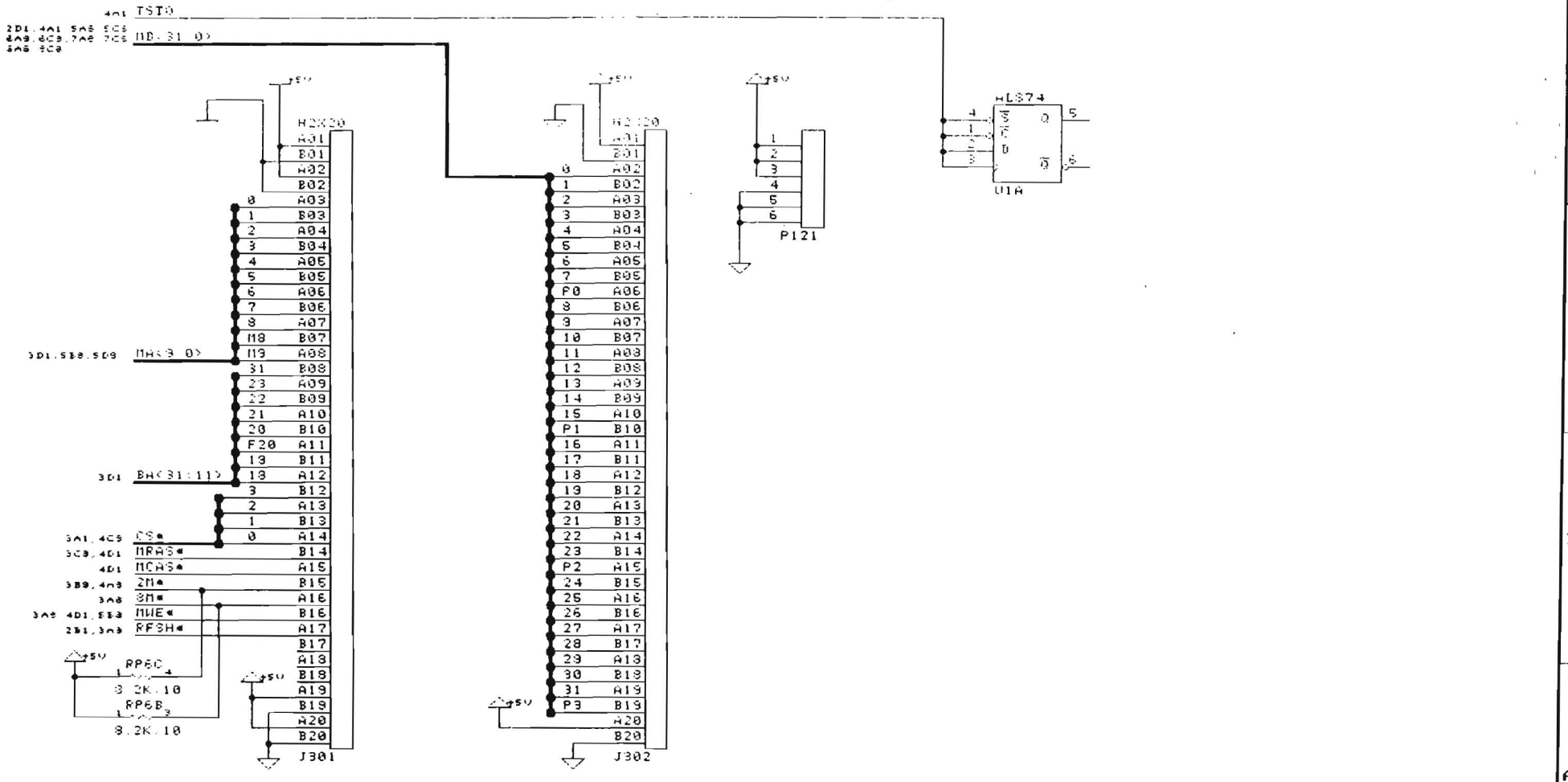
SIZE B	TITLE D4-PAGE DRAM BOARD		ASSY D4-PB
	DRAWING: 000414-000 REV. A		ENGR: PAUL R CULLEY
	REVISED: AUG 06, 1986		SHEET 6 OF 10



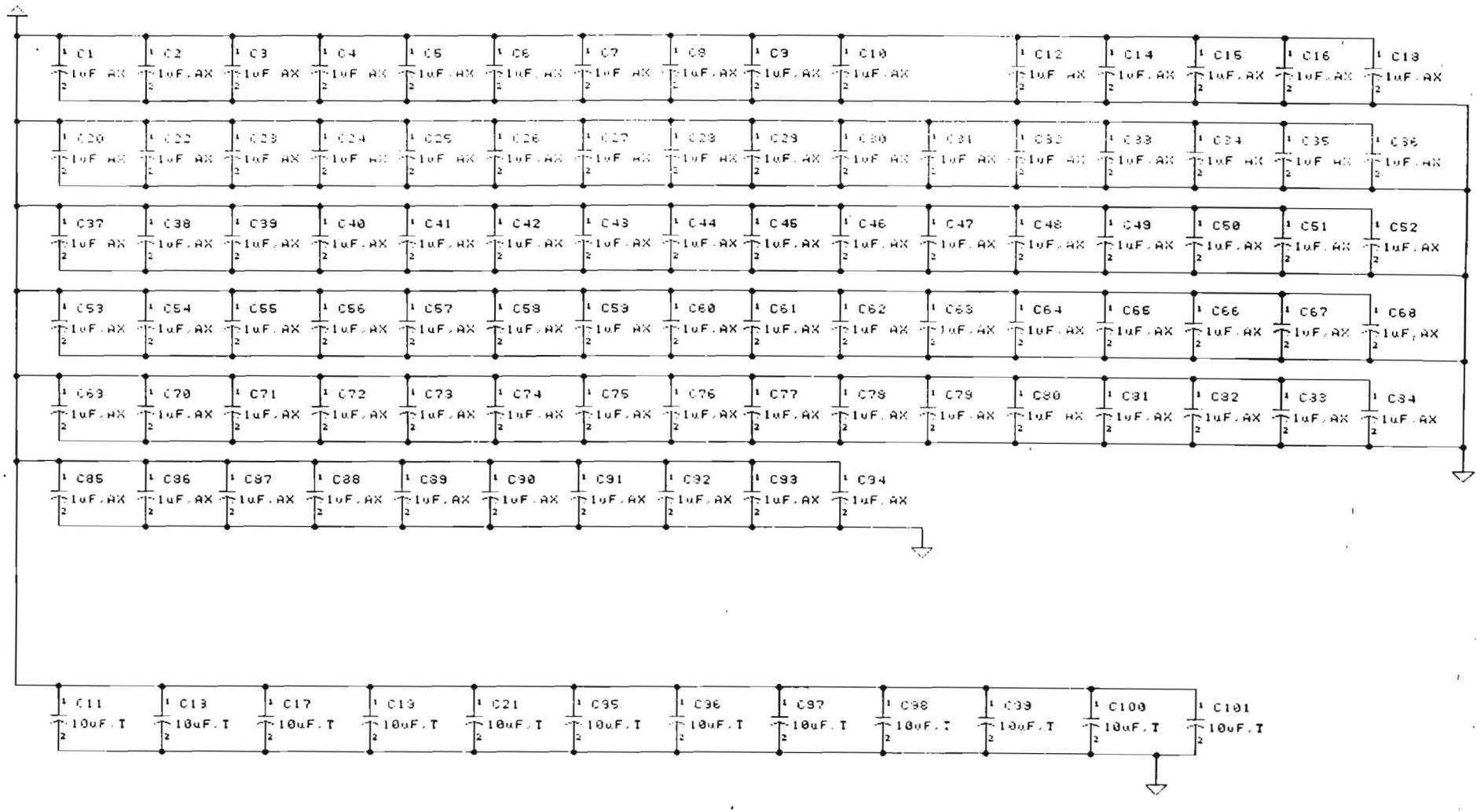
SIZE	TITLE	D4-PAGE DRAM BOARD	
B	DRAWING	000414-000 REV A	SHEET 7 OF 10
	REVISED. AUG 05. 1986	ENGR PAUL R CULLEY	



SIZE B	TITLE D4-PAGE DRAM BOARD		ABER D4-R8
	DRAWING 000414-000 REV. A		EPBR PAUL R. CULLEY
	REVISED AUG 06, 1986		SHEET 8 OF 10

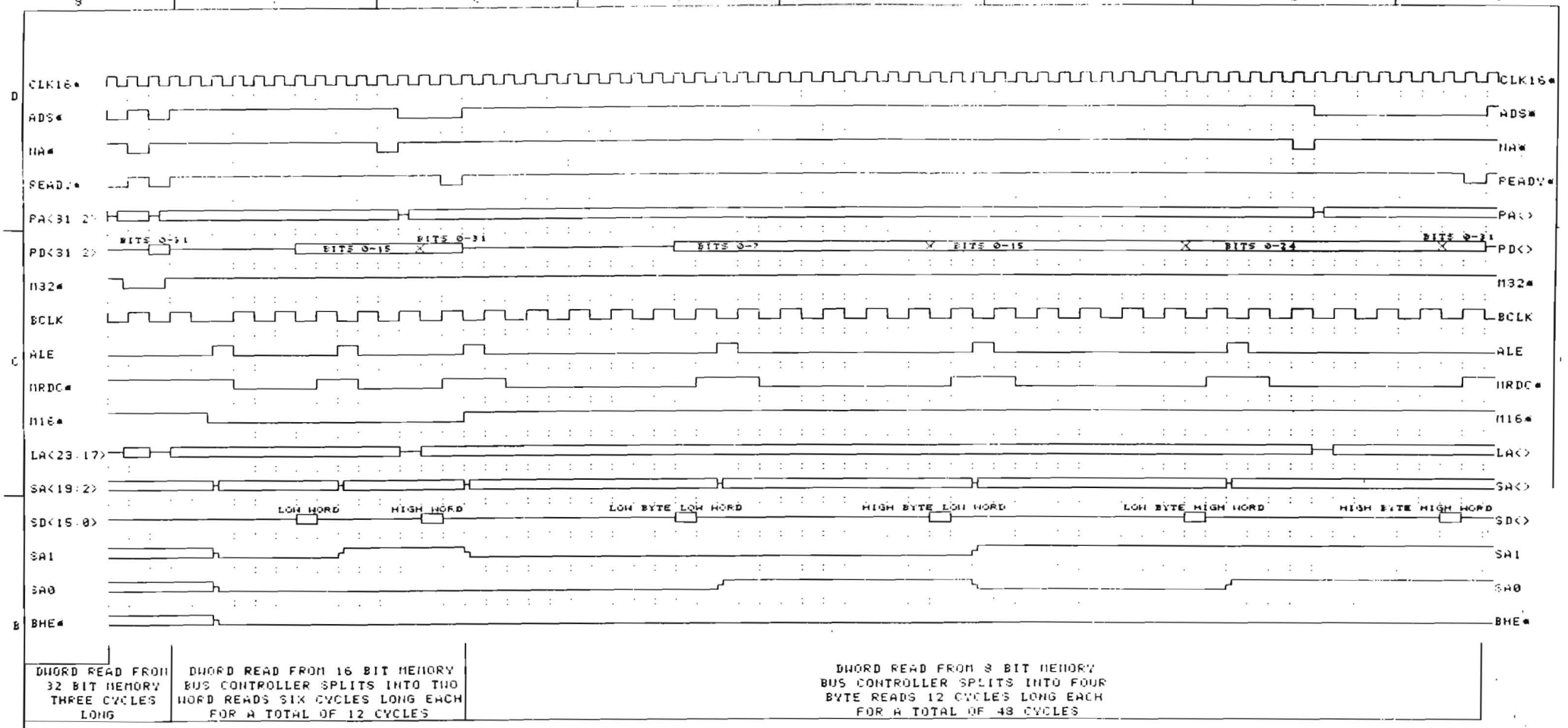


SIZE B	TITLE D4-PAGE DRAM BOARD	SHEET D4-R9
	DRAWING 000414-000 REV. A	ENGR: PAUL R CULLEY
	REVISED AUG 06, 1986	SHEET 9 OF 10



THESE CAPACITORS SHOULD BE EVENLY DISTRIBUTED ABOUT
THE BOARD WITH THE .047 AND 10uF VALUES MIXED UP

SIZE	TITLE	D4 PAGE DRAM BOARD	AREA: D4-R10
B	DRAWING	000414-000 REV A	ENGR: PAUL R. CULLEY
	REVISED	AUG 06, 1986	SHEET 10 OF 10

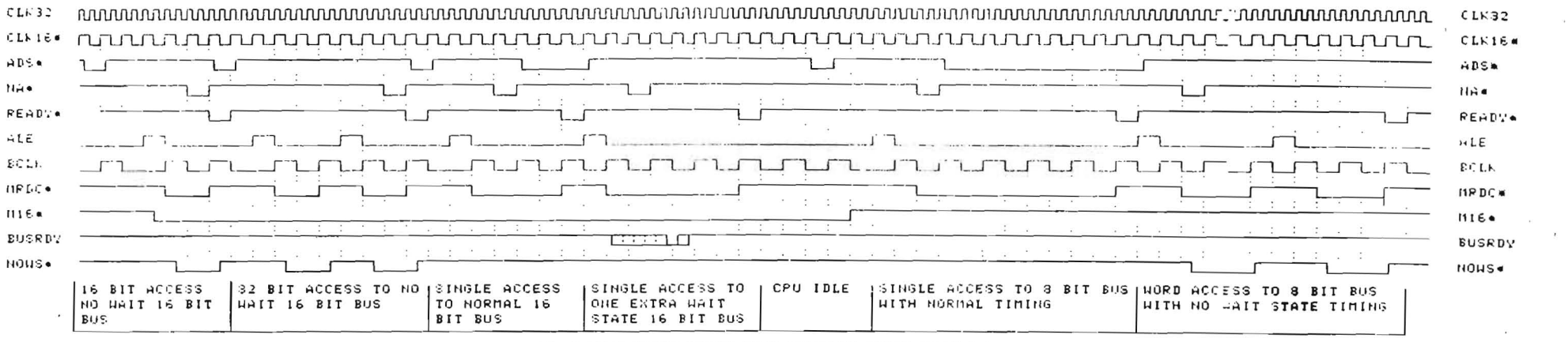


DWORD READ FROM 32 BIT MEMORY THREE CYCLES LONG

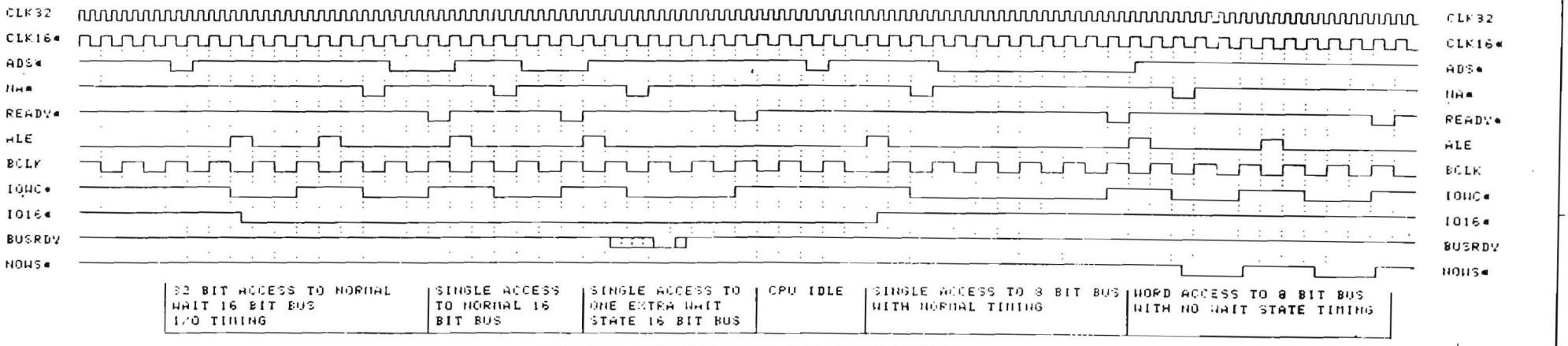
DWORD READ FROM 16 BIT MEMORY BUS CONTROLLER SPLITS INTO TWO WORD READS SIX CYCLES LONG EACH FOR A TOTAL OF 12 CYCLES

DWORD READ FROM 8 BIT MEMORY BUS CONTROLLER SPLITS INTO FOUR BYTE READS 12 CYCLES LONG EACH FOR A TOTAL OF 48 CYCLES

SIZE B	TITLE D4-SYSTEM TIMING	ABER D4-STIM1
	DRAWING 000???-000 REV. A	ENGR. PAUL R CULLEY
	REVISED: JUNE 17, 1986	SHEET 1 OF 2

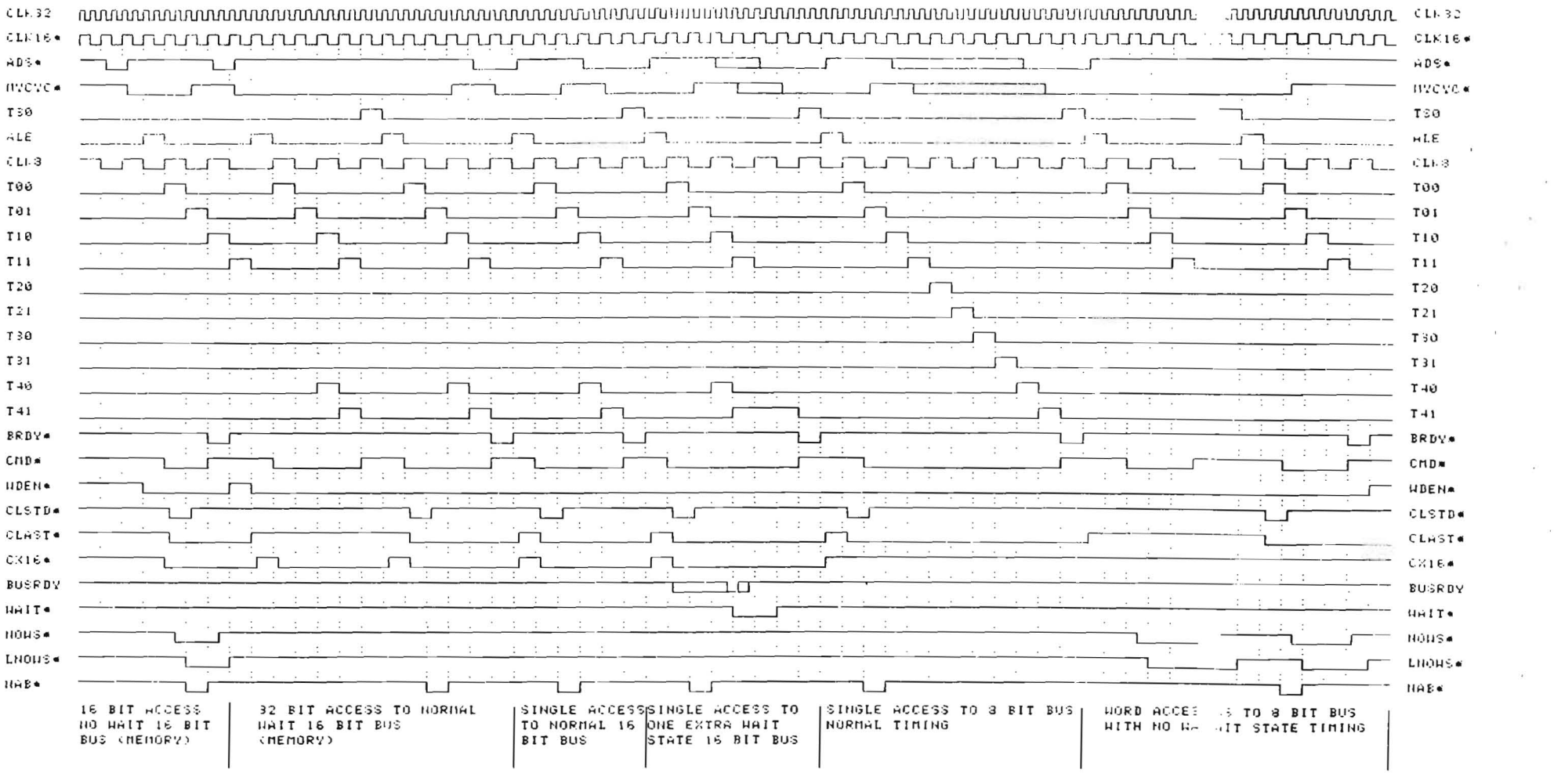


16/8 BIT EXPANSION BUS MEMORY READ TIMING



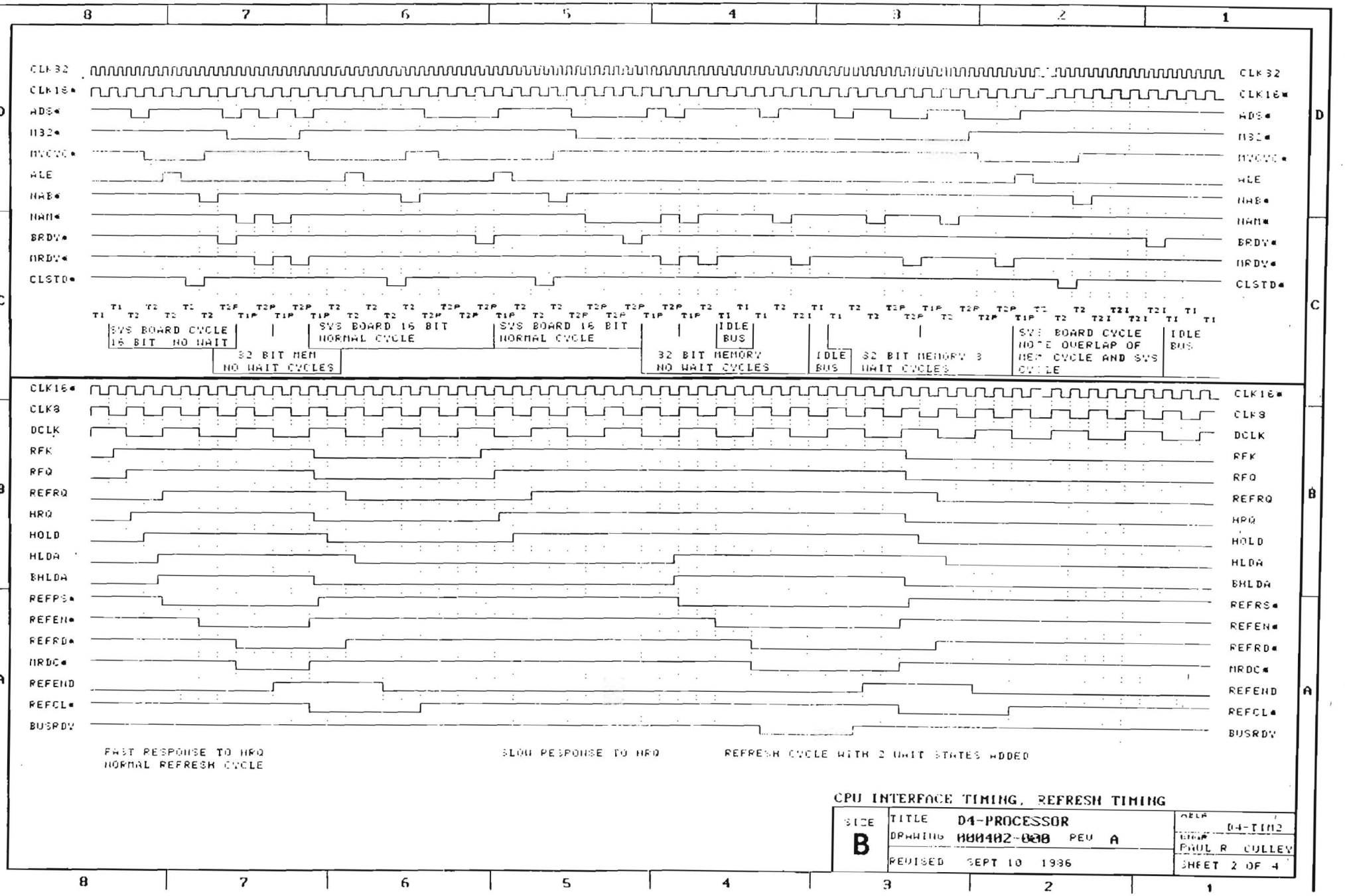
16/8 BIT EXPANSION BUS I/O WRITE TIMING

SIZE B	TITLE D4 SYSTEM TIMING	DESN D4-STIM2
	DRAWING 000???-000 REV A	DRWN PAUL R CULLEY
	REVISED JULY 02, 1986	SHEET 2 OF 2



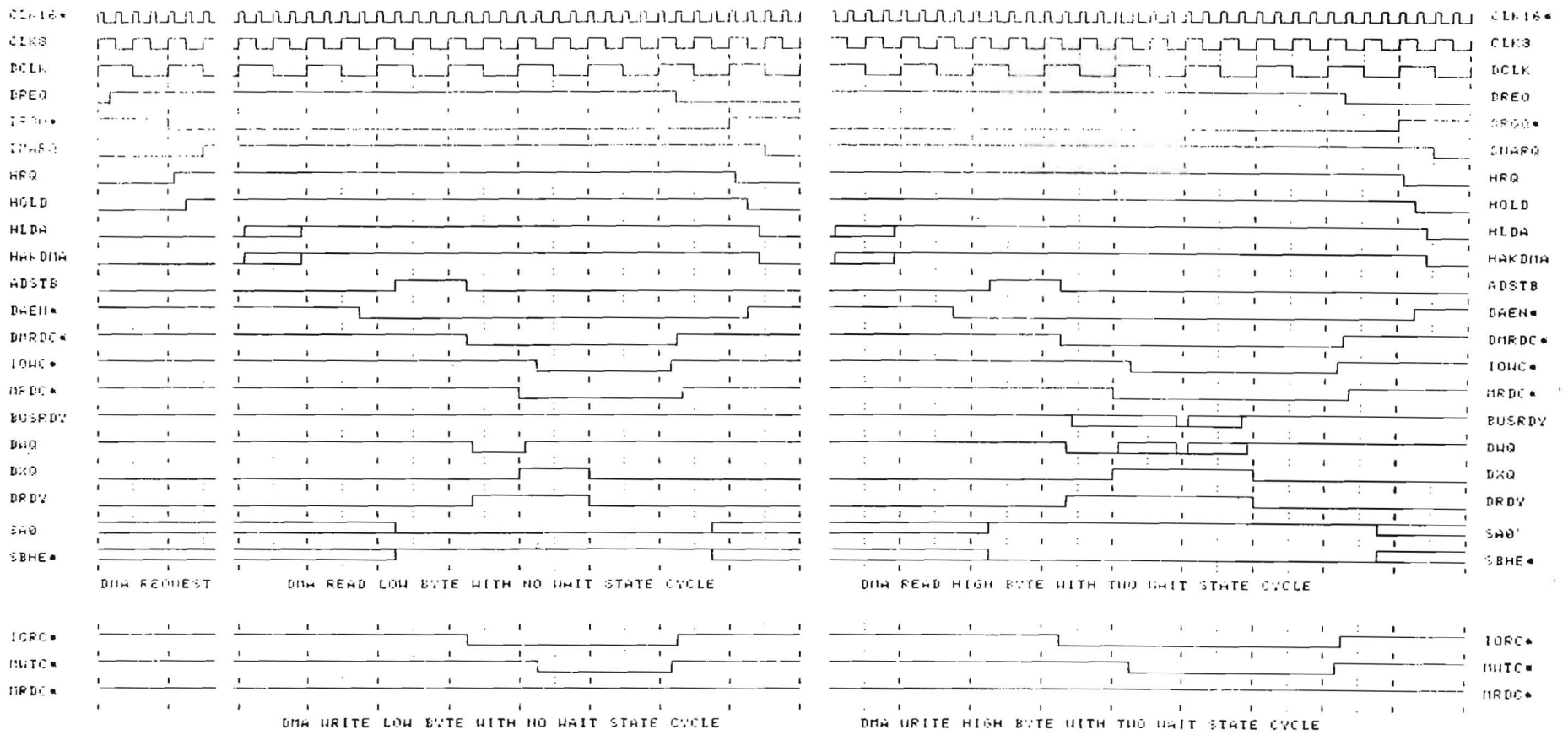
16/8 BIT (286) BUS STATE MACHINE TIMING MEMORY CYCLES

SIZE	TITLE	D4-PROCESSOR	USER: D4-TIM1
B	DRAWING	00040492-000 REV A	ENGR: PAUL R CULLEY
	REVISED:	SEPT 10, 1986	SHEET 1 OF 4



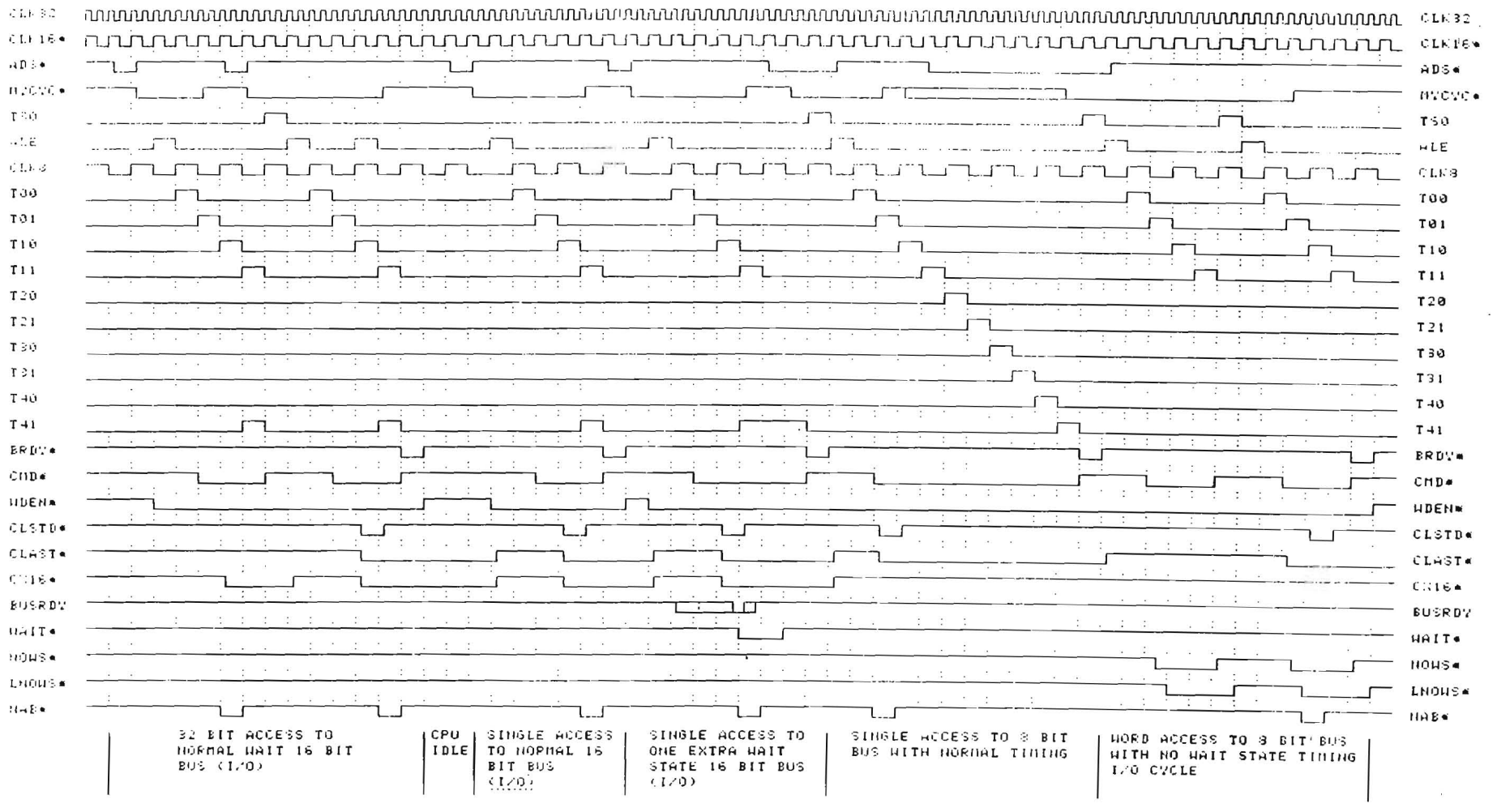
CPU INTERFACE TIMING, REFRESH TIMING

SIZE B	TITLE D4-PROCESSOR	FILE D4-TIM2
	DRAWING 000402-030 REV A	DRAWN PAUL R CULLEY
	REVISED SEPT 10 1986	SHEET 2 OF 4



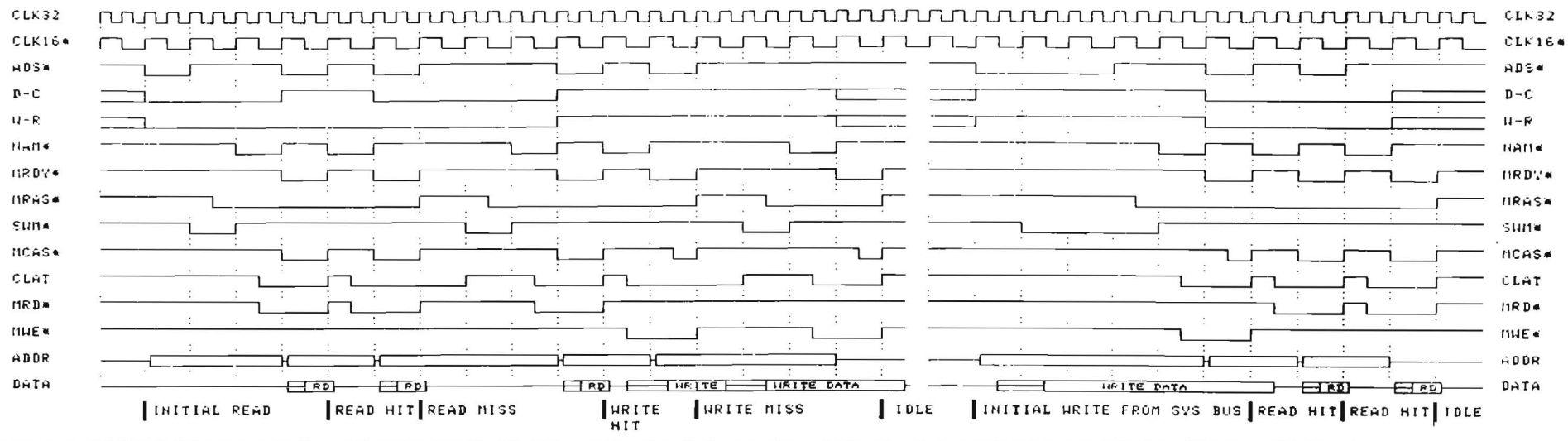
DMA SYSTEM TIMING

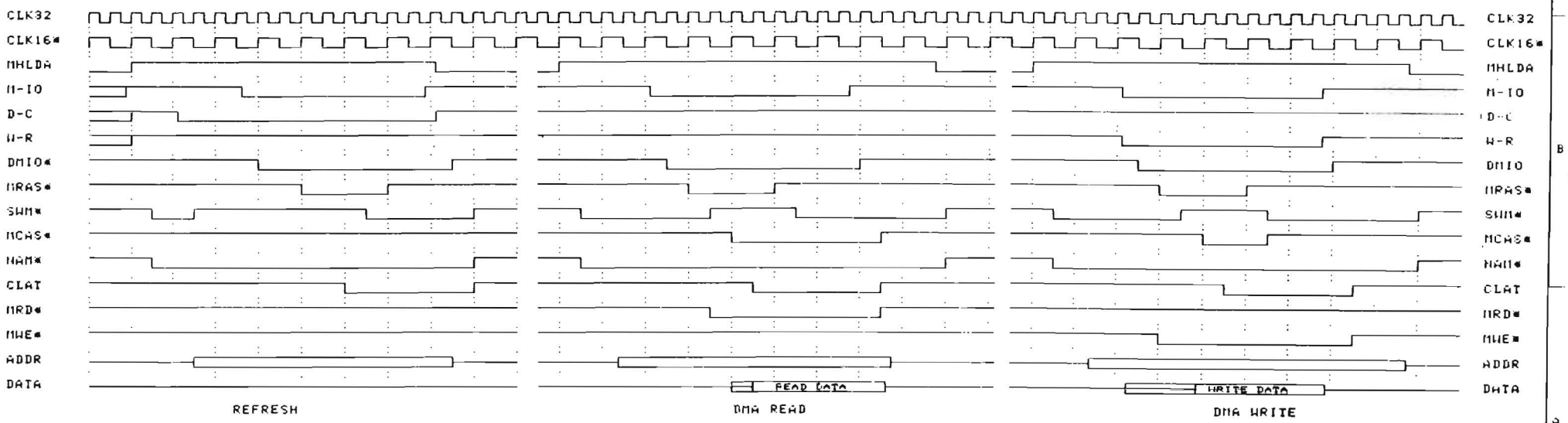
SIZE	TITLE	D4-PROCESSOR	REF	D4-TIM3
B	DRAWING	000402-000 REV A	ENGR.	PAUL R CULLEY
	REVISED	JULY 25, 1986		SHEET 3 OF 4



16/8 BIT (286) BUS STATE MACHINE TIMING I/O CYCLES

SIZE B	TITLE D4-PROCESSOR	APPR D4-TIM4
	DRAWING 000402-000 REV A	ENGR PAUL R CULLEY
	REVISED SEPT 10, 1996	SHEET 4 OF 4





SIZE B	TITLE: D4-PAGE DRAM TIMING	NUMBER: D4-RTIM
	DRAWING: 000414-000 REV A	ENGR: PAUL R CULLEY
	REVISED: SEPT 15, 1986	SHEET 1 OF 1

```
PAL20R4A                                                PAL DESIGN SPECIFICATION
D4-SADOD 108393-001                                   PAUL R. CULLEY    01/09/87
Bus enable to address converter and cycle end logic
COPYRIGHT 1986, 1987 COMPAQ COMPUTER HOUSTON, TEXAS

CALE   ALE   /BE3   /BE2   /BE1 /BE0  LM-IO TOO   T10  /LM16  /IO16  GND
BHLDA /CMD   /CLAST /CLSTD  A1   A0   /BHE  /ALST /CX16 /DCMD  /RST   VCC

;The following 4 outputs are clocked by ALE, output only when /HLDA is true
/A1  := /RST* /BE3* /BE2
      + /RST* /A1*  /A0*  /CX16* /CLAST
      + /RST*  BE1*        CLAST

/A0  := /RST*  BE0*        CLAST
      + /RST*  BE2* /BE1*  CLAST
      + /RST*  BE2*  A0*  /CLAST
      + /RST*  CX16*      /CLAST

BHE  := /RST* /A0* /CX16* /CLAST
      + /RST*  BE1*        CLAST
      + /RST*  BE3

ALST := /RST* /CX16  * /BE2   * /CLAST
      + /RST* /BE2   * /BE0   *  CLAST
      + /RST* /BE3   * /BE1   *  CLAST
      + /RST* /BE3   *  A0    * /CLAST
      + /RST* /CX16  *  A1    * /A0    * /CLAST
      + /RST*  CX16  * /BE3   * /CLAST

;Cycle LAST PRESET input for internal F/F (Cleared by rising edge of ALE)
;This is pulsed only once to set F/F and generate the NAB* signal
CLSTD =  ALST*        TOO                ;Active during the last cycle of set
      +  LM-IO* LM16* TOO* /BE2
      +  LM-IO* LM16* TOO*  A1
      + /LM-IO* IO16* T10* /BE2* /ALST
      + /LM-IO* IO16* T10*  A1*  /ALST
      +  RST                           ;and during RESET

CLAST =  ALST*        TOO                ;Active during the last cycle of set
      +  LM-IO* LM16* TOO* /BE2
      +  LM-IO* LM16* TOO*  A1
      + /LM-IO* IO16* T10* /BE2* /ALST
      + /LM-IO* IO16* T10*  A1*  /ALST
      +  RST                           ;and during RESET
      + CLAST* /ALE                    ;HOLDS ACTIVE TILL ALE

CX16 = /RST*  LM-IO*  TOO* LM16       ;CPU MEM OP
     + /RST* /LM-IO*  T10* IO16       ;CPU I/O OP
     + /RST*         /ALE* CX16       ;CPU HOLD

DCMD = CMD                            ; DELAYED COMMAND

FUNCTION TABLE

CALE BHLDA /RST /BE3 /BE2 /BE1 /BE0 LM-IO ALE TOO T10 /LM16 /IO16 /CMD
/DCMD /CLAST A1  A0  /BHE  /ALST   /CLSTD /CX16
;                L                C          C
;C H             M       L I    D L        A  L C
;A L  R B B B B - A T T M O C  C A      B L  S X
;L D  S E E E E I L 0 1 1 1 M  M S  A A H S  T 1
;E A  T 3 2 1 0 0 E 0 0 6 6 D  D T  1 0 E T  D 6
-------------------------------------------------------------------
 C L  L H H H H H H H L H H H  H L  H H H H  L H ;RESET
```

```
 C L  L H H H H H L H L H H L  L L  H H H H  L H ;
 C L  H L L L L H L L L H H H  H L  L L L H  H H ;32 BIT ON 8 BUS
 C L  H L L L L H H H H H H H  H H  L H L H  H H ;
 C L  H L L L L H H H H H H H  H H  H L L H  H H ;
 C L  H L L L L H H L L H H H  H H  H H L L  H H ;
 L L  H L L L L H L H H H H H  H L  H H L L  L H ;
 C L  H H L L L H L H H H H H  H L  L L L H  H H ;24 BIT ON 8 BUS
 C L  H H L L L H H H H H H H  H H  L H L H  H H
 C L  H H L L L H H L L H H H  H H  H L H L  H H
 L L  H H L L L H L H H H H H  H L  H L H L  L H
 C L  H L L L H H L H H H H H  H L  L H L H  H H ;24 BIT ON 8 BUS HIGH
 C L  H L L L H H H H H H H H  H H  H L L H  H H
 C L  H L L L H H H L L H H H  H H  H H L L  H H
 L L  H L L L H H L H H H H H  H L  H H L L  L H
 C L  H H H L L H L H H H H H  H L  L L L H  H H ;16 LOW ON 8 BUS
 C L  H H H L L H H L L H H H  H H  L H L L  H H
 L L  H H H L L H L H H H H H  H L  L H L L  L H
 C L  H H L L H H L H H H H H  H L  L H L H  H H ;16 MED ON 8 BUS
 C L  H H L L H H H L L H H H  H H  H L H L  H H
 L L  H H L L H H L H H H H H  H L  H L H L  L H
 C L  H L L H H H L H H H H H  H L  H L L H  H H ;16 HIGH ON 8 BUS
 C L  H L L H H H H L L H H H  H H  H H L L  H H
 L L  H L L H H H L H H H H H  H L  H H L L  L H
 C L  H H H H L H H H H H H H  H L  L L H L  L H ;8 LOW ON 8 BUS
 C L  H H H L H H H H H H H H  H L  L H L L  L H ;8 HIGH ON 8 BUS
 C L  H H L H H H H H H H H H  H L  H L H L  L H ;8 LOW  ON 8 BUS HIGH WORD
 C L  H L H H H H L H H H H H  H L  H H L L  L H ;8 HIGH ON 8 BUS HIGH WORD
 C L  H L L L L H L H L L H H  H L  L L L H  H L ;32 BIT ON 16 BUS
 L L  H L L L L H L L L L H H  H L  L L L H  H L ;
 L L  H L L L L H H L L L H H  H H  L L L H  H H ;
 L L  H L L L L H L H L L H H  H H  L L L H  H L ;
 C L  H L L L L H L L L L H H  H H  H L L H  H L ;
 L L  H L L L L H H H H L H H  H L  H L L H  L L ;
 C L  H H L L L L L H H H L H  H L  L L L H  H L ;24 BIT ON 16 BUS
 L L  H H L L L L H H H H L H  H H  L L L H  H L ;
 L L  H H L L L L L H H H L H  H H  L L L H  H L ;
 C L  H H L L L L L L L H L H  H H  H L H L  H L
 L L  H H L L L L L H H H L H  H L  H L H L  L L
 C L  H L L L H L L H H L L H  H L  L H L H  H L ;24 BIT ON 16 BUS HIGH
 L L  H L L L H L H H H L L H  H H  L H L H  H L ;
 L L  H L L L H L L H H L L H  H H  L H L H  H L ;
 C L  H L L L H L L L L L L H  H H  H L L H  H L
 L L  H L L L H L H H H L L H  H L  H L L H  L L
 C L  H H H L L H H H H H L H  H L  L L L H  L L ;16 LOW ON 16 BUS
 L L  H H H L L H L H H L H H  H L  L L L H  L L ;
 C L  H H L L H H L H H L H H  H L  L H L H  H L ;16 MED ON 16 BUS
 L L  H H L L H H H H H L H H  H H  L H L H  H L ;
 L L  H H L L H H L H H L H H  H H  L H L H  H L
 C L  H H L L H H L L L L H H  H H  H L H L  H L
 L L  H H L L H H H H H L H H  H L  H L H L  L L
 C L  H L L H H H H H H L H H  H L  H L L H  L L ;16 HIGH ON 16 BUS
 C L  H H H H L H H H H L H H  H L  L L H L  L L ;8 LOW ON 16 BUS
 C L  H H H L H H H H H L H H  H L  L H L L  L L ;8 HIGH ON 16 BUS
 C L  H H L H H H H H H L H H  H L  H L H L  L L ;8 LOW  ON 16 BUS HIGH WORD
 C L  H L H H H L H H H L L H  H L  H H L L  L L ;8 HIGH ON 16 BUS HIGH WORD
 L L  H L H H H L L H H L L H  H L  H H L L  L L ;
 L L  H L H H H L L L L H L H  H L  H H L L  H L ;
 C L  H H H L L L L L L H H L  H L  L L L H  L L ;16 LOW ON 16 BUS
 L L  H H H L L L H L H H L H  H L  L L L H  L L ;
 L H  H H H L L L H L L H L H  H H  Z Z Z Z  H H ;
;                 L                 C         C
;C H               M       L I     D L         A  L C
;A L  R B B B B - A T T M O C  C A       B L   S  X
```

```
;L D  S E E E E E I L 0 1 1 1 M  M S  A A H S  T 1
;E A  T 3 2 1 0 0 E 0 0 6 6 D  D T  1 0 E T  D 6
```

DESCRIPTION

This PAL converts the CPUs bus enable lines to address lines and cycles from one to the next when multiple cycles are required. It also determines when the last cycle is in progress to develop the Cycle LAST signal.
Rev A of this device changes the CX16* equation to go away on ALE. The input T01 is changed to T10 and M-IO is changed to LM-IO as part of an overall change to delay the sampling of IO16* by one clock. Rev A can be used in any D4-PROCESSOR from rev X5 up.
Rev D is for the D4-Processor Enhanced (387 version)

```
PAL20R8A                                                    PAL DESIGN SPECIFICATION
D4-STATB  108219-001                                        PAUL R. CULLEY   07/17/86
Bus controller state machine logic
Copyright COMPAQ COMPUTER   Houston, Texas

CLK16 /MYCYC /CLAST /CX16   LMIO /LNOWS /BWAIT /M16  T00    T01   T10   GND
/OE    T31   /BRDY  /TS0   /CMD  /WDEN  /T40   /T41  CK8   /ALE  /RST   VCC

;The following functions are clocked by CLK16*

TS0  :=
  /RST* /CLAST*  T41* /BWAIT                ;START NEXT CYCLE WHEN DONE WITH
+ /RST* /CLAST* /CK8*  LNOWS* CMD           ; PREV CYCLE AND MORE IN GROUP
+ /RST*  CLAST*  T41* /BWAIT*      MYCYC    ;START NEXT CYCLE WHEN DONE WITH
+ /RST*  CLAST* /CK8*  LNOWS* CMD* MYCYC    ; PREV CYCLE AND NEW CPU REQUEST
                                           ; IS PENDING

CMD  :=
  /RST*  CMD* /LNOWS* /T41                  ;HOLDS UNTIL ENDED BY END OF
+ /RST*  CMD* /LNOWS*  BWAIT                ; WAIT
+ /RST*  CMD*  CK8                          ; OR NOWS AND CK8 LOW
+ /RST* /CMD* ALE* M16* LMIO                ;STARTS AFTER ALE UNLESS
+ /RST* /CMD* T00                           ; CMDLY  (THEN AFTER T00)

WDEN :=
  /RST*  TS0                                ;STARTS WHEN ALE DOES AFTER TS0
+ /RST* /TS0* /ALE* /CMD* /T00* MYCYC       ;OR WHEN CPU SENDS NEW START REQUEST
+ /RST*  ALE                                ;CONTINUES THROUGH T00
+ /RST*  T00                                ;AND T01
+ /RST*  CMD                                ;UNTIL AFTER CMD GOES AWAY

T41  :=
  /RST*  T40                                ;STARTS WHEN T40 ENDS
+ /RST*  T10*  CX16 * /LNOWS* CMD           ;OR WHEN T10 ENDS ON I/O CYCLE
+ /RST*  T41*  BWAIT                        ;AND HOLDS TILL WAIT IS GONE

T40  :=
  T01*  CX16* /LNOWS* /RST                  ;STARTS AFTER T01 IF 16 BIT
+ T31*        /LNOWS* /RST                  ;OR AFTER T31 OTHERWISE

/CK8 :=
  /RST*  TS0                                ;SET TO LOW DURING ALE AFTER TS0,
+ /RST* /TS0* /ALE* /CMD* /T00* MYCYC       ;WHEN CPU SENDS NEW START REQUEST
+  CK8                                      ; OTHERWISE, DIVIDE BY TWO

BRDY :=
  /RST*  CLAST*  T41* /BWAIT                ;START NEXT CYCLE WHEN DONE
+ /RST*  CLAST* /CK8*  LNOWS* CMD           ; WITH PREV CYCLE AND NO MORE IN GROUP

ALE  :=
  /RST*  TS0                                ;ALE FOLLOWS TS0 FOR INTERNAL USE
+ /RST* /TS0* /ALE* /CMD* /T00* MYCYC       ; WHEN CPU SENDS NEW START REQUEST

FUNCTION TABLE

CLK16 /OE  /RST /M16 LMIO /LNOWS /BWAIT /CLAST /CX16 /MYCYC TS0 ALE T00
T01 T10 T31 T40 T41 /BRDY /CMD /WDEN CK8

;        / / /    /
;C       L B C /  M                    /   /
;L / / L N W L C  Y                    B / W C
;K R M M O A A X  C T A T T T T T T    R C D L
;  E 1 I N I S 1  Y S L O O 1 3 4 4    D M E K
```

```
;6ET 6 0 S T T 6  C 0 E 0 1 0 1 0 1  Y D N 8
-------------------------------------------------------------------------
 LHH X H X X X X  X Z Z X X X X Z Z  Z Z Z Z   ;OE TEST
 CLL X H X H L X  H L L L L L L L L  H H H X   ;RESET
 CLH X H X H L X  H L L L L L L L L  H H H X   ;CLEAR RESET
 CLH X H H H L X  L L H L L L L L L  H H L L  *;ALE
 CLH L H H H L L  L L L L L L L L L  H L L H   ;CMD, T00, 16 BIT NORMAL CYCLE
 CLH L H H H H L  L L L H L L L L L  H L L L   ;T01
 CLH H H H H H L  L L L L H L L H L  H L L H   ;T40, NOT LAST CYCLE
 CLH H H H H H L  L L L L L L L L H  H L L L   ;T41
 CLH H H H H H L  L H L L L L L L L  H H L H   ;CMD END, TS0 NEXT CYCLE
 CLH H H H H H L  L L H L L L L L L  H H L L  +;ALE
 CLH L L H H H L  L L L L L L L L L  H H L H   ;T00, CMDLY, 16 BIT CYCLE
 CLH L L H H L L  L L L H L L L L L  H L L L   ;T01, CMD
 CLH L H H H L L  H L L L H L L H L  H L L H   ;T40, LAST CYCLE
 CLH L H H L L L  L L L L L L L L H  H L L L   ;T41, ADD A WAIT STATE
 CLH L H H L L L  L L L L L L L L H  H L L H   ;T41, ADD A WAIT STATE
 CLH L H H L L L  L L L L L L L L H  H L L L   ;T41, ADD A WAIT STATE
 CLH L H H H L L  L H L L L L L L L  L H L H   ;TS0 NEXT CYCLE
 CLH L H H H L L  L L H L L L L L L  H H L L  *;ALE
 CLH L H H H L L  L L L L L L L L L  H L L H   ;CMD, T00, 16 BIT NO WAIT STATE
 CLH L H L H H L  L L L H L L L L L  H L L L   ;T01
 CLH L L L H H L  L H L L H L L L L  H H L H   ;CMD END, TS0 NEXT CYCLE
 CLH L L H H H L  L L H L L L L L L  H H L L  +;ALE
 CLH L H H H H L  H L L L L L L L L  H L L H   ;CMD, T00, 16 BIT NO WAIT STATE
 CLH L H L H L L  L L L H L L L L L  H L L L   ;T01
 CLH X H L H L L  L H L L H L L L L  L H L H   ;REQ RECEIVED
 CLH L H H H L H  L L H L L L L L L  H H L L  *;ALE
 CLH H H H H L H  L L L L L L L L L  H H L H   ;T00, 8 BIT NO WAIT CYCLE
 CLH H H H H L H  L L L H L L L L L  H L L L   ;T01, CMD
 CLH L H H H L H  L L L L H L L L L  H L L H   ;T01, CMD
 CLH L H L H H H  L L L L L L L L L  H L L L   ;T11
 CLH L H L H H H  L H L L L H L L L  H H L H   ;CMD END, TS0 NEXT CYCLE
 CLH L H H H H H  L L H L L L L L L  H H L L  +;ALE
 CLH H H H H H H  L L L L L L L L L  H H L H   ;T00, 8 BIT NO WAIT CYCLE
 CLH H H H H H H  L L L H L L L L L  H L L L   ;T01
 CLH L H H H L H  H L L L H L L L L  H L L H   ;T10, CMD
 CLH L H H H L H  H L L L L H L L L  H L L L   ;T11
 CLH L H L H L H  L H L L L L L L L  L H L H   ;REQ RECEIVED
 CLH L H H H L H  L L H L L L L L L  H H L L  *;ALE
 CLH H H H H L H  L L L L L L L L L  H H L H   ;CMD, T00, 8 BIT NORMAL CYCLE
 CLH H H H H L H  L L L H L L L L L  H L L L   ;T01
 CLH L H H H L H  L L L L H L L L L  H L L H   ;T10
 CLH L H H H L H  H L L L L H L L L  H L L L   ;T11
 CLH L H H H L H  H L L L L L L L L  H L L H   ;T20,T21,T30
 CLH L H H H L H  H L L L L L L L L  H L L L   ;T31
 CLH L H H H L H  H L L L L L H H L  H L L H   ;T40
 CLH L H H H L H  H L L L L L L L H  H L L L   ;T41
 CLH L H H H L H  H L L L L L L L L  L H L H   ;CMD END
 CLH L H H H L H  H L L L L L L L L  H H H L   ;IDLE
 CLH X H H H L H  L L H L L L L L L  H H L L  *;ALE
 CLH L H H H L H  L L L L L L L L L  H L L H   ;CMD, T00, 16 BIT NORMAL CYCLE
 CLH L H H H H H  L L L H L L L L L  H L L L   ;T01
 CLH L H H H H H  L L L L H L L L L  H L L H   ;T10
 CLH L H H H H L  L L L L L H L L H  H L L L   ;T41
 CLH H H H H H L  L H L L L L L L L  H H L H   ;CMD END, TS0 NEXT CYCLE
;         / / /    /
;C        L B C /  M                    /   /
;L / / L N W L C  Y                    B / W C
;K R M M O A A X  C T A T T T T T T  R C D L
;10S 1 I W I S 1  Y S L 0 0 1 3 4 4  D M E K
;6ET 6 0 S T T 6  C 0 E 0 1 0 1 0 1  Y D N 8
-------------------------------------------------------------------------
```

DESCRIPTION

This PAL implements some of the bus controller state machine logic.
REV B adjusts the sampling time of the IO16* line by adding state T10 to the startup of T41. If the CX16* (IO16) line comes in after T00, then we shift to T41 instead of T40. REV B also tightens up the response from ADS* to ALE by one clock by shifting directly to ALE from MYCYC during the initial bus transaction. State TS0 is still used between transactions.

PAL16L8B
D4-SADI 105645-001

PAL DESIGN SPECIFICATION
PAUL R. CULLEY 02/13/86

Address to byte enable conversion and read latch enable logic


```
A1      A0      /BHE    /CX16   NC2     /CMD    LW-R    HLDA    NC1     GND
TST     /BE0    /BE1    /BE2    /BE3    B0CK    B1CK    B2CK    B3CK    VCC

IF (HLDA) BE0 = /A1 * /A0

IF (HLDA) BE1 = /A1 * BHE

IF (HLDA) BE2 = A1 * /A0

IF (HLDA) BE3 = A1 * BHE

IF (/TST) /B0CK = /CMD
                + LW-R
                + A0
                + A1

IF (/TST) /B1CK = /CMD
                + /BHE
                + /CX16  * /A0
                + LW-R
                + A1

IF (/TST) /B2CK = /CMD
                + /A1
                + LW-R
                + A0

IF (/TST) /B3CK = /CMD
                + /BHE
                + /A1
                + /CX16  * /A0
                + LW-R

FUNCTION TABLE

TST     HLDA    A1      A0      /BHE    /CX16   /CMD    LW-R
/BE3    /BE2    /BE1    /BE0    B3CK    B2CK    B1CK    B0CK

;
;
;  H       C   L           B B B B
;T L     B X C W   B B B B 3 2 1 0
;S D A A H 1 M -   E E E E C C C C
;T A 1 0 E 6 D R   3 2 1 0 K K K K
-------------------------------------------------------------------------
 L H L L L H L L   H H L L L L L H
 L H L L H H L L   H H H L L L L H
 L H L H L H L L   H H L H L L H L
 L H H L L H L L   L L H H L H L L
 L H H L H H L L   H L H H L H L L
 L H H H L H L L   L H H H H L L L
 L L L L L L L L   Z Z Z Z L L H H
 L L L L H L L L   Z Z Z Z L L L H
 L L L H L L L L   Z Z Z Z L L H L
 L L H L L L L L   Z Z Z Z H H L L
 L L H L H L L L   Z Z Z Z L H L L
 L L H H L L L L   Z Z Z Z H L L L
 L L H H H L L L   Z Z Z Z L L L L
```

```
L L H L L L H L   Z Z Z Z L L L L
L L L L L L L H   Z Z Z Z L L L L
L L H L L L L H   Z Z Z Z L L L L
H L H L L L L H   Z Z Z Z Z Z Z Z
```

DESCRIPTION

This PAL contains the logic to back drive the 386 byte enables during the non CPU operations. It decodes the address inputs and drives the appropriate BEx lines whenever the 386 is in a HLDA state.

This PAL also contains the decoding logic to drive the read latches clock lines (74ALS573 fall through latch). These clock lines have positive true outputs and are enabled when the CPU executes a MRDC, IORC, or INTA command.
The basic equation is: BxCK = BSOx * CMD * /LW-R

```
PAL16L8B                                                    PAL DESIGN SPECIFICATION
D4-SCMDD  108394-001                                      PAUL R. CULLEY    01/09/87
Command encode and decode logic
Copyright 1986, 1987 COMPAQ COMPUTER   Houston, Texas

/CMD     /DCMD    LM-IO    LW-R     LD-C     /RFSH   /BHLDA    NCI1      NCI2      GND
/OE      /IOWC    /MRDC    /MWTC    /IORC    MHLDA    M-IO     D-C       W-R       VCC

IF (/BHLDA* OE) MRDC =
  CMD  *  LM-IO * /LW-R                    ; PROCESSOR MEMORY READ
+ DCMD *  MRDC                             ; SHORT READ HOLD

IF (/BHLDA* OE) MWTC =
  CMD  *  LM-IO *  LW-R *  LD-C            ; PROCESSOR MEMORY WRITE

IF (/BHLDA* OE) IORC =
  CMD  * /LM-IO * /LW-R *  LD-C            ; PROCESSOR I/O READ
+ DCMD * IORC                              ; SHORT READ HOLD

IF (/BHLDA* OE) IOWC =
  CMD  * /LM-IO *  LW-R *  LD-C            ; PROCESSOR I/O WRITE

IF (BHLDA* OE) /M-IO = MWTC + MRDC         ; NON CPU MEMORY OPERATION

IF (BHLDA* OE) /D-C  = RFSH                ; NON CPU REFRESH OPERATION

IF (BHLDA* OE) /W-R  = MWTC                ; NON CPU WRITE OPERATION

/MHLDA =
  /BHLDA                          ; SAME A BHLDA EXCEPT
+ /MHLDA * /M-IO                  ; WHEN GOING HOLD, WAIT FOR M-IO TO GO HIGH

FUNCTION TABLE

/OE      /DCMD    /CMD     LM-IO    LD-C     LW-R     /RFSH   /BHLDA
/MRDC    /MWTC    /IORC    /IOWC    MHLDA    M-IO     D-C      W-R

;                 /
;  /   L      / B    / / / / M
;  D / M L L R H    M M I I H  M
;  C C - D W F L    R W O O L  - D W
;O M M I - - S D    D T R W D  I - -
;E D D O C R H A    C C C C A  O C R
-------------------------------------------------------------------------------
 L H L L L L L H    H H H H L  Z Z Z  ; INTA
 L H L L L H L H    H H H H L  Z Z Z  ;
 L H L L H L L H    H H L H L  Z Z Z  ; IORC
 L L L L H L L H    H H L H L  Z Z Z  ; IORC
 L L H L H L L H    H H L H L  Z Z Z  ; IORC
 L H L L H H L H    H H H L L  Z Z Z  ; IOWC
 L H L H L L L H    L H H H L  Z Z Z  ; CODE MRDC
 L H L H L H L H    H H H H L  Z Z Z  ;
 L H L H H L L H    L H H H L  Z Z Z  ; MRDC DATA
 L L L H H L L H    L H H H L  Z Z Z  ; MRDC DATA
 L L H H H L L H    L H H H L  Z Z Z  ; MRDC DATA
 L H L H H H L H    H L H H L  Z Z Z  ; MWTC
 L H H H H H L H    H H H H L  Z Z Z  ;
 H H H H H H L H    Z Z Z Z X  Z Z Z  ;
 H H H H H H L L    Z Z Z Z X  Z Z Z  ;
 L H H H H H L L    H H Z Z H  H L H  ; RFSH
 L H H H H H L L    L H Z Z H  L L H  ; RFSH MRDC
 L H H H H H H L    L H Z Z H  L H H  ; MRDC
 L H H H H H H L    H L Z Z H  L H L  ; MWTC
```

```
 H H L H H L H H   Z Z Z Z L  L H H  ;
 H H L H H L H L   Z Z Z Z L  L H H  ;
 H H H H H H H L   Z Z Z Z H  H H H  ;
;                 /
;  /   L     / B   / / / / M
;  D / M L L R H   M M I I H  M
;  C C - D W F L   R W O O L  - D W
;O M M I - - S D   D T R W D  I - -
;E D D O C R H A   C C C C A  O C R
-------------------------------------------------------------------------------
```

DESCRIPTION

This PAL decodes the processor status lines and generates the normal command output signals. These signals are floated during non processor commands.

In addition, the PAL decodes the non processor operations and feeds them to the cpu status bus during HOLDA.

Rev A of the PAL adds the input DCMD* and OE*. DCMD* is used to provide a short data hold time for read operations by extending MRDC and IORC by one PAL delay (10 ns). OE* is added to disable all outputs for testing.
Rev D of the PAL removes INTA and adds MHLDA for use in the DP3E D4-processor board (with 387).

```
; HLDA M-IO D-C  W-R
;  L    L    L    L   CPU INTERRUPT ACK
;  L    L    L    H   CPU NEVER PRODUCES THIS CODE
;  L    L    H    L   CPU I/O READ
;  L    L    H    H   CPU I/O WRITE
;  L    H    L    L   CPU MEMORY CODE READ
;  L    H    L    H   CPU HALT OR SHUTDOWN
;  L    H    H    L   CPU MEMORY DATA READ
;  L    H    H    H   CPU MEMORY DATA WRITE
;  H    L    L    L   NON CPU REFRESH WRITE (SHOULD NOT HAPPEN)
;  H    L    L    H   NON CPU REFRESH READ
;  H    L    H    L   NON CPU MEMORY WRITE
;  H    L    H    H   NON CPU MEMORY READ
;  H    H    L    X   NON CPU REFRESH CYCLE (BEFORE OR AFTER)
;  H    H    H    X   NON CPU NO CYCLE PRESENT
```

```
PAL16L8A                                                    PAL DESIGN SPECIFICATION
D4-SCPYD 108395-001                                        PAUL R. CULLEY    12/17/86
Copy buffer control logic and DMA low address logic
Copyright 1986 COMPAQ COMPUTER   Houston, Texas

/M16     /IO16    /MWTC    /MRDC    /IOWX    /IORC    /DAEN1    AEN2   BALE      GND
/HLDA    /DAEN2   /COPYEN  /COPYHL  /DAEN    /BHE     XA0       /LM16  NC01      VCC

COPYEN  = /DAEN* BHE * XA0 * /LM16* MWTC        ;CPU write MEM
        + /DAEN* BHE * XA0 * /IO16* IOWX        ;CPU write I/O
        + /DAEN* BHE * XA0 * /LM16* MRDC        ;CPU read MEM
        + /DAEN* BHE * XA0 * /IO16* IORC        ;CPU read I/O
        + DAEN1 * COPYHL * XA0 * LM16 * MRDC    ;DMA byte mem read high of 16
        + DAEN1 * XA0 * LM16 * IORC             ;DMA byte mem write high of 16

COPYHL  = /DAEN * BHE * XA0 * /LM16 * MWTC      ;mem write
        + /DAEN * BHE * XA0 * /IO16 * IOWX      ;I/O write
        + DAEN1 * XA0 * LM16 * MRDC             ;DMA byte mem read high of 16
        + COPYHL * COPYEN                       ; Short holdover for write

DAEN    = DAEN1 * HLDA
        + AEN2 * HLDA


                                                ;If word type of DMA, enable out
IF (AEN2 * HLDA) /XA0 = AEN2                    ; (Pin is low for word DMA)


                                                ;If DMA, enable output
IF (DAEN) BHE = XA0 * DAEN1                     ;If byte type, is inverted XA0
        + AEN2                                  ;If word type, is active

LM16 =  M16 * BALE                               ;Enable M16 input
     +  LM16 * /BALE                             ;Latch term
     +  LM16 * M16                              ;Deglitch term

DAEN2 = AEN2 * HLDA                            ;TIGHTEN UP ON HLDA

FUNCTION TABLE

/M16 /IO16 /MRDC /MWTC /IORC /IOWX /DAEN1 /AEN2 BALE /HLDA
/BHE XA0 /COPYEN /COPYHL /DAEN /LM16 /DAEN2

;                                C C
;                 D     /        O O     D
;  I M M I I A A B H             P P D L A
;M O R W O O E E A L  B X  Y Y A M E
;1 1 D T R W N N L D  H A  E H E 1 N
;6 6 C C C X 1 2 E A  E O  N L N 6 2
-------------------------------------------------------------------------------
 H H H H H H H H L H  H L  H H H X H    ;INACTIVE
 L H H H L H H H H H  L H  L H H L H    ;IORC
 L H L H H H L H L L  L H  L L L L H    ;MRDC
 L H H H L H L H L L  L H  L L L L H    ;IORC
 L H H H H H L H L L  H L  H H L L H    ;DAEN INACTIVE
 H H H H H H H L L L  L L  H H L L L    ;DAEN2
 L L L L L L H H H H  L H  H H H L H
 H H H H H H H H H H  L H  H H H H H    ;INACTIVE
 H H L H H H H H H H  L H  L H H H H    ;MRDC PROC
 H H H L H H H H L H  L H  L L H H H    ;MWTC PROC
 H H H H H H H H L H  H H  H H H H H    ;
 H H H H H L H H L H  L H  L L H H H    ;IOWC PROC
 L H H H H H L L H H  Z Z  H H H L H    ;
 L H H H H H L L L H  Z Z  H H H L H    ;
 H H H H H H L L L H  Z Z  H H H L H    ;
```

```
;                                C C
;              D     /           O O     D
;  I M M I I A A B H             P P D L A
;M O R W O O E E A L  B X  Y Y A M E
;1 1 D T R W N N L D  H A  E H E 1 N
;6 6 C C C X 1 2 E A  E O  N L N 6 2
```

DESCRIPTION

This PAL implements the logic to enable the copy buffer (high to low halves of the 16 bit bus). It also drives the A0 and BHE lines as appropriate during DMA.
Rev A changes the COPYHL enable during byte DMA operations to the high half of the bus. The timing is made earlier by changing to IORC from MWTC.
Rev D changes the polarity of the AEN2 signal for logic reduction on the D3PE D4-PROCESSOR board (with 80387).

PAL16L8A
D4-SDEND 108396-001
Data Buffer enable logic

PAL DESIGN SPECIFICATION
PAUL R. CULLEY 12/09/86

```
A1      A0      /BHE    /CMD    /M32    /WDEN   LW-R    LD-C    LM-IO   GND
TST     /BDIRRD /BOEN   /B1EN   /B2EN   /INTA   /MWTC   /MRDC   /B3EN   VCC

IF (/TST) BDIRRD = /MRDC* /WDEN                         ;OTHER WRITE TO LOCAL MEM

IF (/TST) BOEN = /A1* /A0* MWTC* /WDEN                  ;OTHER WRITE TO LOCAL MEM
               + /A1* /A0* MRDC* /WDEN* M32             ;OTHER READ FROM LOCAL MEM
               + /A1* /A0* LD-C* LW-R* WDEN             ;CPU WRITE TO BUS

IF (/TST) B1EN = /A1*  BHE* MWTC* /WDEN                 ;OTHER WRITE TO LOCAL MEM
               + /A1*  BHE* MRDC* /WDEN* M32            ;OTHER READ FROM LOCAL MEM
               + /A1*  BHE* LD-C* LW-R* WDEN            ;CPU WRITE TO BUS

IF (/TST) B2EN = A1* /A0* MWTC* /WDEN                   ;OTHER WRITE TO LOCAL MEM
               + A1* /A0* MRDC* /WDEN* M32              ;OTHER READ FROM LOCAL MEM
               + A1* /A0* LD-C* LW-R* WDEN              ;CPU WRITE TO BUS

IF (/TST) B3EN = A1*  BHE* MWTC* /WDEN                  ;OTHER WRITE TO LOCAL MEM
               + A1*  BHE* MRDC* /WDEN* M32             ;OTHER READ FROM LOCAL MEM
               + A1*  BHE* LD-C* LW-R* WDEN             ;CPU WRITE TO BUS

IF (/TST) INTA = CMD* /LM-IO* /LW-R* /LD-C              ;CPU INTERRUPT ACK

FUNCTION TABLE

TST A1 A0 /BHE /WDEN LM-IO LW-R LD-C /CMD /M32 /MWTC /MRDC
/BDIRRD /B3EN   /B2EN   /B1EN   /BOEN /INTA

;                           B
;                           D
;         W L L L     M M   I B B B B I
;T     B D M W D C M W R   R 3 2 1 O N
;S A A H E I - - M 3 T D   R E E E E T
;T 1 O E N O R C D 2 C C   D N N N N A
-------------------------------------------------------------------------
 L L L L H H H H H L L H   L H H L L H
 L H L L H H H H H L L H   L L L H H H
 L L L L H L H L L L H L   H H H L L H
 L H L L H H L L L L H L   H L L H H H
 L L L L H L L H L H H H   L H H H H H
 L L L L L L L L L H H H   H H H H H L
 L L L L L L L L H H H H   H H H H H H
 L L L L L H H H H H H H   H H H L L H
 L H L L L H H H H H H H   H L L H H H
 H H L L L H H H H H H H   Z Z Z Z Z Z
-------------------------------------------------------------------------
```

DESCRIPTION

This PAL develops the control signals to enable the data buffers on the system board.
Rev A ensures turnon of the buffer enables for mem write after the direction is active by leaving the buffer turned around during the entire write cycle.
Rev D is for use with D3PE D4-processor board (with 387).

```
PAL16R4                                                    PAL DESIGN SPECIFICATION
D4-SKEY 108360-001                                  JOHN THAYER   9/18/86
8042 A20 LINE FIX PAL
COPYRIGHT COMPAQ COMPUTER HOUSTON, TEXAS 1986

CLK /RST A2 /CS D4_D6 D7 D5 D3 D2 GND
/OE D1 D0 /Q0 /Q1 A20 /WC8042 /FF_OR_D1 /WC VCC

Q0 := /RST * WC          * CS              ;Q0 FOLLOWS WC, CLEARED ON RESET

Q1 := ; SET IF IN STATE 00 OR 10 AND D1 COMMAND TO PORT 64H
      /RST * /Q0 * CS * WC * A2 * D7*D4_D6*/D5*/D3*/D2*/D1*D0
      ; KEEP SET IF STATE 11
    + /RST * Q0 * Q1
      ; IF STATE 10, KEEP SET TILL CS * WC
    + /RST * /Q0 * Q1 * /CS
    + /RST * /Q0 * Q1 * /WC



/A20 := ; INVERSE OF A20 FUNCTION
       ; CLEAR IF STATE 10 AND 60 WRITE AND D1 IS LOW
         /RST * Q1 *  /Q0 * /A2 * CS * WC * /D1
       ; OTHERWISE FEED BACK
      +  /RST * Q0 * /A20
      +  /RST * /Q1 * /A20
      +  /RST * /CS * /A20
      +  /RST * /WC * /A20
      +  /RST * A2 * /A20


FF_OR_D1 = D7*D4_D6* D5* D3* D2* D1*D0
         + D7*D4_D6*/D5*/D3*/D2*/D1*D0

WC8042 := ; NO D1 WRITE YET: DON'T FILTER IF WRITE IS TO 60H
          /RST * /Q0 * /Q1 * CS * WC * /A2
                ; DON T FILTER IF WRITE IS TO 64H AND NOT <D1> OR <FF>
        + /RST * /Q0 * CS * WC * A2 * /FF_OR_D1


FUNCTION TABLE
/OE CLK RST CS WC A2 D4_D6 D7 D5 D3 D2 D1 D0
Q1 Q0 FF_OR_D1 A20 WC8042

;                                        F   W
;              D                         F   C
;              4                         0   8
;   O R        *                         R A 0
;O L S C W A D D D D D D   Q Q D 2 4
;C K T S C 2 6 7 5 3 2 1 0   1 0 1 0 2
-------------------------------------------------
 L X X X X X H H H H H H   X X H X X ;TEST FF_OR_D1
 L X X X X X H H L L L L H   X X H X X
 L X X X X X H L H L L L H   X X L X X

;
 L C H X X X X X X X X X   L L X H L ;RESET
;
 L C L L L X X X X X X X   L L X H L  ;IO WRITE, NO CS
 L C L L H X X X X X X X   L L X H L
 L C L L L X X X X X X X   L L X H L

;
 L C L H H H L L L L L L   L H L H H ;64 WRITE NOT (D1 OR FF)
 L C L H H H L L L L L L   L H L H L
```

```
 L C L H H H L L L L L L L   L H L H L
 L C L H L X X X X X X X X   L L X H L
;
 L C L H L X X X X X X X X   L L X H L
 L C L H H H H H H H H H H   L H H H L ;64 WRITE FF
 L C L H H H H H H H H H H   L H H H L
 L C L H L X X X X X X X X   L L X H L
;
 L C L H L X X X X X X X X   L L X H L
 L C L H L H H H H H H H H   L H H H H ;60 WRITE
 L C L H H L H H H H H H H   L H H H L
 L C L H H L H H H H H H H   L H H H L
 L C L H L X X X X X X X X   L L X H L
;
 L C L H L X X X X X X X X   L L X H L
 L C L H H H H H L L L L H   H H H H L ;CLEAR A20
 L C L H H H H H L L L L H   H H H H L         ;64 WRITE D1
 L C L H L X X X X X X X X   H L X H L
;
 L C L H L X X X X X X X X   H L X H L
 L C L H H L L L L L L L L   L H L L L         ;60 WRITE TO CLEAR
 L C L H H L L L L L L L L   L H L L L         ;LATCH
 L C L H L X X X X X X X X   L L X L L
;
 L C L H L X X X X X X X X   L L X L L
 L C L H H L H H H H H H H   L H H L H ;60 WRITE TO TEST TERMS
 L C L H H L H H H H H H H   L H H L L
 L C L H H L H H H H H H H   L H H L L
 L C L H L X X X X X X X X   L L X L L
;
 L C L H L X X X X X X X X   L L X L L
 L C L H H H H H L L L L H   H H H L L ;SET A20
 L C L H H H H H L L L L H   H H H L L         ;64 WRITE D1
 L C L H L X X X X X X X X   H L X L L
;
 L C L L H L X X X X X X X   H L X L L         ;TST TERM /RST*/CS*/A20
;
 L C L H L X X X X X X X X   H L X L L
 L C L H H H H H L L L L H   H H H L L         ;WRITE D1 AGAIN
 L C L H H H H H L L L L H   H H H L L
 L C L H L X X X X X X X X   H L X L L
;
 L C L H L X X X X X X X X   H L X L L
 L C L H H L L L L L L H L   L H L H L         ;60 WRITE TO SET
 L C L H H L L L L L L H L   L H L H L         ;LATCH
 L C L H L X X X X X X X X   L L X H L
;
 L C L H L X X X X X X X X   L L X H L
 L C L H H H H H L L L L H   H H H H L ;D1 THEN FF, MASK BOTH
 L C L H H H H H L L L L H   H H H H L         ;64 WRITE D1
 L C L H L X X X X X X X X   H L X H L
;
 L C L H L X X X X X X X X   H L X H L
 L C L H H H H H H H H H H   L H H H L         ;64 WRITE FF
 L C L H H H H H H H H H H   L H H H L
 L C L H L X X X X X X X X   L L X H L
;
 L C L H L X X X X X X X X   L L X H L
 L C L H H H H H L L L L H   H H H H L ;D1 THEN 64 WRITE, MASK ONLY D1
 L C L H H H H H L L L L H   H H H H L         ;64 WRITE D1
 L C L H L X X X X X X X X   H L X H L
;
 L C L H L X X X X X X X X   H L X H L
```

```
 L C L H H H H H H H H L   L H L H H          ;64 WRITE D0
 L C L H H H H H H H H L   L H L H L
 L C L H H H H H H H H L   L H L H L
 L C L H L X X X X X X X   L L X H L
;
 L C L H L X X X X X X X   L L X H L ;CLEAR A20
 L C L H H H H H L L L H   H H H H L          ;64 WRITE D1
 L C L H L X X X X X X X   H L X H L
 L C L H H L L L L L L L   L H L L L          ;60 WRITE TO CLEAR
 L C L H L X X X X X X X   L L X L L          ;LATCH
 L C L H L X X X X X X X   L L X L L ;TEST TERM /RST*Q0*/A20
 L C L H H H H H L L L H   H H H L L  ;(THIS IS NOT A LEGAL INPUT
 L C L H H L H H L L L H   H H H L L ; DURING NORMAL OPERATION)
;
;                                     F   W
;             D                       F   C
;             4                       0   8
;   C R       *                       R A 0
;O L S C W A D D D D D D D   Q Q D 2 4
;C K T S C 2 6 7 5 3 2 1 0   1 0 1 0 2
-------------------------------------------------------------
```

DESCRIPTION

This PAL is used to speed up the 8042's response to changes in the L0WA20 line. It works by intercepting the specific write commands to the 8042 and executing them itself.

```
PAL16R4C                                                PAL DESIGN SPECIFICATION
D4-SMSCD  108397-001                                  PAUL R. CULLEY     01/12/87
Miscellaneous garbage logic
Copyright 1986, 1987 COMPAQ COMPUTER   Houston, Texas

CLK   /M32   /BRDY   BALE   W-R   D-C  M-IO  /BEO   PA31  GND
/OE   /LNCP  /CLSTD /MYCYC /LOE   /NAB  /SHTD  387I /ADS   VCC

LOE :=
  MYCYC * BALE * /W-R * /LNCP            ; GOES ACTIVE AT ALE
+ LOE * /BRDY                            ; HOLD THROUGH TILL BRDY ACTIVE

SHTD :=
  MYCYC* BALE* M-IO* /D-C* W-R* BEO      ; DECODED SHUTDOWN OPCODE

MYCYC :=
  /CLSTD * ADS * /M-IO * /387I           ; WHEN NO 387 AND I/O
+ /CLSTD * ADS * /M-IO * /PA31           ; OR NOT NCP I/O CYCLE
+ /CLSTD * ADS *  M-IO * /M32            ; OR NOT 32 BIT MEMORY CYCLE
+ /CLSTD * ADS *  M-IO * /D-C * W-R      ; OR HALT/SHUTDOWN CYCLE
+ /CLSTD * MYCYC                         ; HOLD TILL NAB

NAB := CLSTD                             ; NEXT ADDRESS BUS

LNCP =
  MYCYC* BALE* PA31* /M-IO               ; NUMERIC COPROCESSOR OP
+ LNCP* /BALE                            ; HOLD TILL NEXT ALE OR HOLD
+ MYCYC* PA31* /M-IO* LNCP               ; DEGLITCH


FUNCTION TABLE

CLK /OE  /M32  /BRDY  BALE   M-IO  D-C  W-R   /BEO PA31
/ADS  /CLSTD 387I /LNCP  /MYCYC /LOE  /NAB  /SHTD

;
;                           C       M
;      B B M          P     L 3  L  Y      S
;C /  M R A - D W B A   A S 8  N  C L N H
;L O  3 D L I - - E 3   D T 7  C  Y O A T
;K E  2 Y E O C R O 1   S D I  P  C E B D
-----------------------------------------------------------------
 C L  H L H H H H H L   L H H  H  X H H H  RESET MTCYC BY /M32
 C L  H L H H H H H L   L H H  H  L H H H  RESET MTCYC BY /M32
 C L  H L H H H H H L   H H H  H  L H H H  HOLD MYCYC
 C L  H L H H H H H L   H L H  H  H H L H
 C L  L L H H L H H L   L L H  H  H H L H
 C L  L L H H L H L L   L H H  H  L H H H  MYCYC BY HALT
 C L  L L H H L H L L   L L H  H  H H L L
 C L  L L H L L L H L   L H H  H  L H H H  MYCYC BY I/O
 C L  L L H L L L H L   L L H  H  H L L H
 C L  L L H L L L H H   L H L  L  L H H H  MYCYC BY 387 NOT INSTALLED
 L L  L L L L L L H H   L H L  L  L H H H
 C L  L H L L L L H H   L L L  L  H H L H
 C L  L H L L L L H H   L L L  L  H H L H
-----------------------------------------------------------------
```

DESCRIPTION

Rev D of this PAL is for the upgraded D3PE D4-processor board (with 387) and is a new design.
This PAL contains the equations for the signal MYCYC (BUS state machine cycle), SHTD (decoded shutdown status), LNCP (numeric processor access status), and

LOE (latch output enable). It also is the F/F for the NAB signal.

```
PAL16L8A                                                PAL DESIGN SPECIFICATION
D4-SNCP          105657-001                               PAUL R. CULLEY    05/07/86
Numeric          Coproccessor error and busy logic
Copyright 1986 Compaq Computer Houston,          Texas

/TIMCS /XIOWC  XA0    /ERROR  /BUSYIN TIM0  /NCPIN /NCPCS  /RESET   GND
 XA3   RES287 /TIM2CS /TIM1CS  ONESHT IRQ13  NC02   EN_ERR /BUSYOUT VCC

;The following equation        is the positive true output of the equation:
;RES287         = RESET + XIOWC * NCPCS * /XA3 * XA0  ;I/O write to F1h

IF (VCC) /RES287 =
  /RESET * /XIOWC                          ;NOT I/O WRITE
+ /RESET * /NCPCS                          ;NOT port FX
+ /RESET *  XA3                                  ;NOT address XX1XXXb
+ /RESET * /XA0                                  ;NOT address XXXXX0b

IF (VCC) BUSYOUT =
  /RESET*  NCPIN* BUSYIN                   ;coprocessor busy
+ /RESET*  NCPIN* ERROR         * EN_ERR* /TIM0 ;error before int ack
+ /RESET* /NCPIN* NCPCS         * XA3 * XIOWC   ;When not installed and NCP accessed
+ /RESET* /NCPIN* ONESHT* /TIM0                 ;When not installed till timeout

;The following equation        is the positive true output of the equation:
;IRQ13 = ERROR*         /BUSYIN* EN_ERR* NCPIN ;Int when error and enabled

IF (VCC) /IRQ13          =
  /ERROR                                   ;No int if no error
+ BUSYIN                                   ; or busy
+ /EN_ERR                                  ; or not enabled for err
+ /NCPIN                                   ;No int if not installed

IF (VCC) /EN_ERR =
  /RESET* NCPIN* /EN_ERR * ERROR           ;Hold disabled till ERROR goes away
+ /RESET* NCPIN* /EN_ERR * BUSYIN          ;Hold disabled till BUSY goes away
+  XIOWC * NCPCS * /XA3         * /XA0           ;Disable on write to port 0F0h

IF (VCC) /ONESHT =
   NCPIN * /IRQ13                          ;One shot output when IRQ (installed)
+ /NCPIN * /ONESHT * /XIOWC               ;Goes high on NCP access when not
+ /NCPIN * /ONESHT * /XA3                 ;  installed
+ /NCPIN * /ONESHT * /NCPCS               ;
+ /NCPIN *  TIM0                          ;  and stays high till timeout
+  RESET                                   ;Low at reset time

IF (VCC) TIM1CS          = TIMCS * /XA3      ;Timer 1 at address 040h-047h,050h-057h

IF (VCC) TIM2CS          = TIMCS *  XA3      ;Timer 2 at address 048h-04Fh,058h-05Fh

FUNCTION TABLE

/NCPIN /XIOWC TIM0 /TIMCS /NCPCS XA3 XA0 /RESET /ERROR /BUSYIN
RES287 /BUSYOUT IRQ13  ONESHT /EN_ERR /TIM1CS /TIM2CS
;                    /     /     / / /
;/     / /     / / B   R B   0 E T T
;N /   T N     R E U   E U I N N I I
;C I T I C     E R S   S S R E _ M M
;P 0 I M P X X S R Y   2 Y 0 S E 1 2
;I W M C C A A E 0 I   8 0 1 H R C C
;N C 0 S S 3 0 T R N   7 U 3 T R S S
-------------------------------------------------------------------
 L H L H H H H L H H   H H L L L H H  ;RESET
 L H L H H H H H H H   L H L L L H H  ;NO RESET
```

```
 L L L H L L H H H H   H H L L L H H  ;RES287
 L L L H L H H H H L   L L L L L H H  ;BUSYOUT,NORES287 BY XA3,NOINT BY ERROR
 L L L H H L H H L H   L L H H L H H  ;IRQ13,BUSYOUT,NORES287 BY NCPCS
 L L H H H L H H L H   L H H H L H H  ;BUSYOUT,NORES287 BY NCPCS
 L L H H H L H L L L   H H L L L H H  ;NO INT BY BUSYIN
 L H H H L L H H H H   L H L L L H H  ;NO RES287 BY IOWC
 L L H H L L L H H H   L H L L H H H  ;LOCKERR,NO RES287 BY XA0
 L L H H L L L H H L   L L L L H H H  ;LOCKERR,NO RES287 BY XA0
 L L H H H L L H H L   L L L L H H H  ;LOCKERR,NO RES287 BY XA0
 L L H H H L L H L L   L L L L H H H  ;HOLD LOCKERR,NO INT BY EN_ERR
 L L H H H L L H L H   L H L L H H H  ;HOLD LOCKERR,NO INT BY EN_ERR
 L H H L H L H H H H   L H L L L L H  ;TIM1CS
 L H H L H H H H H H   L H L L L H L  ;TIM2CS
 H L L H L H L H H H   L L L H L H H  ;NOT INSTALLED AND SELECTED
 H H L H H H H H L H   L L L H L H H  ;NOT INSTALLED ERROR
 H H H H H H H H H L   L H L L L H H  ;NOT INSTALLED BUSY
 H H L H L H H H H L   L H L L L H H  ;
 H H L H H L H H H L   L H L L L H H  ;
 H L L H H H H H H L   L H L L L H H  ;
 H H L H H L H H H L   L H L L L H H  ;
 H L L H L L H H H L   H H L L L H H  ;
;
;    T             B   R B   O E T T
;N   I T N     R E U   E U I N N I I
;C I M I C     E R S   S S R E _ M M
;P O O M P X X S R Y   2 Y Q S E 1 2
;I W U C C A A E O I   8 0 1 H R C C
;N C T S S 3 0 T R N   7 U 3 T R S S
```

DESCRIPTION

This PAL is used in the Magnum processor board to handle the error logic for the numberic coprocessor. It allows a greater measure of compatibility with the previous products. It sets up the system to generate an interrupt when the error signal is recieved. It holds the interrupt until the service routine does a write to port F0h. It also holds busy out active until the interrupt occurs or till the CPU times out from no activity. This is to prevent any other numeric processor instructions from being executed until the error has been recognized. If the no activity timeout occurs, that means the CPU hung up on the 287 interface due to different design of the 386. In this case, the interrupt will have been recieved by the 386.

In addition, the timer chip selects are broken out to the seperate selects by the PAL logic.

```
PAL16L8A                                              PAL DESIGN SPECIFICATION
D4-SPPI 105659-001                                    PAUL R. CULLEY    12/10/85
Peripheral interface decode logic
Copyright Compaq Computer Houston, Texas

XA4      /PPICS   /XIORC   XA3     XA9      XA0      XA8      /XIOWC  /INTA   GND
RESCMOS  /CMOSWR  /NMICLK  /PBWR   /CMOSRD  /KEYCS   /CIORD   /PBRD   CMOSAWR VCC

NMICLK   = PPICS *  XA4 * /XA3 * /XA0 * XIOWC     ;NMI register write (70h)

CMOSRD   = PPICS *  XA4 * /XA3 *  XA0 * XIORC     ;CMOS data read (71h)

CMOSWR   = PPICS *  XA4 * /XA3 *  XA0 * XIOWC     ;CMOS data write (71h)

KEYCS    = PPICS * /XA4 * /XA3 * /XA0             ;8042 (60h, 64h)

PBWR     = PPICS * /XA4 * /XA3 *  XA0 * XIOWC     ;Port B write (61h)

PBRD     = PPICS * /XA4 * /XA3 *  XA0 * XIORC     ;Port B read (61h)

CIORD    = /XA9 * /XA8 * XIORC                    ;0-FFH
         + INTA                                   ;or Interrupt ack

/CMOSAWR = /NMICLK * /RESCMOS                     ;Inverted NMICLK
         + /XIOWC  * /RESCMOS                     ;CMOS address write (70h)


FUNCTION TABLE

/XIORC /XIOWC /INTA XA9 XA8 XA4 XA3 XA0 /PPICS RESCMOS
/NMICLK CMOSAWR /CMOSWR /CMOSRD /KEYCS /PBWR /PBRD /CIORD

;                      R   N C C C
;X X                   P E   M M M M K     C
;I I I                 P S   I O O O E P P I
;O O N X X X X X I C   C S   S S S Y B B O
;R W T A A A A A C M   L A   W R C W R R
;C C A 9 8 4 3 0 S O   K W   R D S R D D
-------------------------------------------------------------------------
 H H H H H H L H H H   H H   H H H H H H H
 H H H L L L L L L L   H L   H H L H H H      ;8042 SELECT
 H H L H H H L H H L   H L   H H H H H L      ;BUFFER ENABLE ON INTA
 H L H L L H L L L L   L H   H H H H H H      ;CMOS ADDRESS WRITE
 H H H L L H L L L L   H L   H H H H H H      ;CMOS ADDRESS WRITE
 H L H L L H L H L L   H L   L H H H H H      ;CMOS WRITE
 L H H L L H L H L L   H L   H L H H H L      ;CMOS READ
 L H H L L L L H L L   H L   H H H H L L      ;PORT B READ
 L H H L L L L H H L   H L   H H H H H L      ;BUFFER ENABLE
 L H H H L L L H H L   H L   H H H H H H      ;BUFFER DISABLE
 L H H L H L L H H L   H L   H H H H H H      ;BUFFER DISABLE
 H L H L L L L H L L   H L   H H H L H H      ;PORT B WRITE (NO BUF ENABLE)
 H L H L L L H H L L   H L   H H H H H H      ;
 H L H L L H H H L L   H L   H H H H H H      ;
;
;                      R   C C C
;X X                   P E   M M M K     C
;I I I                 P S   O O O E P P I
;O O N X X X X X I C   S S   S S Y B B O
;R W T A A A A A C M   A W   R C W R R
;C C A 9 8 4 3 0 S O   W R   D S R D D
-------------------------------------------------------------------------
```

DESCRIPTION

This PAL is used in the D4 (386) processor board to decode addresses within the range 60h to 7Fh for I/O. It also generates the signal that controls the direction of the I/O data buffer XD<7..0>.

```
PAL16L8A                                                PAL DESIGN SPECIFICATION
D4-SROMA 108135-001                                   PAUL R. CULLEY    06/26/86
System ROM decode logic
Copyright 1986 Compaq Computer Houston, Texas

BALE   LA23    LA22  LA21 LA20 LA19  LA18   LA17   SA16   GND
/MRDC /ROM1OE /RFSH /M32 /M16E /ROM /ROMEN /LOWEN /ROM2OE VCC

M16E  = /LA23*/LA22*/LA21*/LA20* LA19* LA18* LA17        ;00E0000h-00FFFFFh
      +  LA23* LA22* LA21* LA20* LA19* LA18* LA17        ;0FE0000h-0FFFFFFh
      +  M32

ROM   = /LA23*/LA22*/LA21*/LA20* LA19* LA18* LA17* BALE ;00E0000h-00FFFFFh
      +  LA23* LA22* LA21* LA20* LA19* LA18* LA17* BALE ;0FE0000h-0FFFFFFh
      + /LA23*/LA22*/LA21*/LA20* LA19* LA18* LA17* ROM  ;DEGLITCH
      +  LA23* LA22* LA21* LA20* LA19* LA18* LA17* ROM  ;DEGLITCH
      + /BALE* ROM                                      ;LATCH TERM

ROM1OE = ROM *  SA16 * MRDC                             ;00F0000h-00FFFFFh
                                                        ;0FF0000h-0FFFFFFh

ROM2OE = ROM * /SA16 * MRDC                             ;00E0000h-00EFFFFh
                                                        ;0FE0000h-0FEFFFFh

ROMEN  = ROM * MRDC                                     ;BUFFER ENABLE

LOWEN = /LA23* /LA22* /LA21* /LA20* BALE        ; BOTTOM ONE MEGABYTE AND BALE
      + /LA23* /LA22* /LA21* /LA20* LOWEN       ; DEGLITCH TERM
      + /BALE* LOWEN                            ; LATCH TERM
      + RFSH                                    ; AND REFRESH


FUNCTION TABLE

BALE LA23 LA22 LA21 LA20 LA19 LA18 LA17 SA16 /MRDC /RFSH /M32
/ROM /ROM1OE /ROM2OE /ROMEN /M16E /LOWEN

;                              R R
;                              O O R   L
;B L L L L L L L S M R         M M O M O
;A A A A A A A A R F M   R 1 2 M 1 W
;L 2 2 2 2 1 1 1 1 D S 3   O O O E 6 E
;E 3 2 1 0 9 8 7 6 C H 2   M E E N E N
-------------------------------------------------------------------------
 H L L L L L L L L H H L   H H H H L L    ;INACTIVE
 L L L L L L L L L H H H   H H H H H L    ;INACTIVE
 L L L L L H H H L H H H   H H H H L L    ;ROM2 ADDRESS, NO READ, NO ALE
 H L L L L H H H L H H H   L H H H L L    ;ROM2 ADDRESS, NO READ, ALE
 L L L L L L L L L L H H   L H L L H L    ;ROM2 READ, HOLD ADDRESS ON ROM
 H L L L L L L L L H H H   H H H H H L    ;INACTIVE
 L L L L L L L L L H H H   H H H H H L    ;INACTIVE
 L H H H H H H H H H H H   H H H H L L    ;ROM1 ADDRESS, NO READ, NO ALE
 H H H H H H H H H H H H   L H H H L H    ;ROM1 ADDRESS, NO READ, ALE
 L H H H H L L L H L H H   L L H L H H    ;ROM1 READ, HOLD ADDRESS ON ROM
 H L L L L L L L H H H H   H H H H H L    ;INACTIVE
 H H L L L H H H H H H H   H H H H H H    ;INACTIVE
 H L H L L H H H H H H H   H H H H H H    ;INACTIVE
 H L L H L H H H H H H H   H H H H H H    ;INACTIVE
 H L L L H H H H H H H H   H H H H H H    ;INACTIVE
 H L L L L L H H H H H H   H H H H H L    ;INACTIVE
 H L L L L H L H H H H H   H H H H H L    ;INACTIVE
 H L L L L H H L H H H H   H H H H H L    ;INACTIVE
 H L L L L H H H L H H H   H H H H H L    ;INACTIVE
```

```
H H L H H H H H H H H H   H H H H H H     ;INACTIVE
H H H L H H H H H H H H   H H H H H H     ;INACTIVE
H H H H L H H H H H H H   H H H H H H     ;INACTIVE
H H H H H L H H H H H H   H H H H H H     ;INACTIVE
H H H H H H L H H H L H   H H H H H L     ;INACTIVE
H H H H H H H L H H H H   H H H H H H     ;INACTIVE
```

DESCRIPTION

This PAL is used in the D4 (386) processor board to decode ROM addresses within the two ranges 0FE0000h-0FFFFFFh and 00E0000h-00FFFFFh. It also generates the signal that controls the ROM data buffer RD<15..0> and the signal M16 (memory is 16 bits) during ROM accesses.
The signal LOWEN* is generated by this PAL to indicate when the low one megabyte of the system is being accessed.

```
PAL16R8B                                                PAL DESIGN SPECIFICATION
D4-RCTLA 108352-001                                     PAUL R. CULLEY  09/13/86
D4 PAGE RAM BOARD Control logic
Copyright Compaq Computer Houston, Texas 1986

CLK /ADSM /DMIO  D-C  W-R  /M32   HLDA /CLK16 /HIT GND
/OE /MRAS /SWM   /NAM /MCAS /MRDY /MWE  /MRD  /YY   VCC

SWM :=
  /HLDA*  CLK16* ADSM* /MRDY* /W-R* M32          ;CPU IDLE TO MEMORY
+ /HLDA*  CLK16* ADSM* /MRDY*  D-C* M32          ;CPU IDLE TO MEMORY
+ /HLDA*  CLK16* YY*   /MRAS* /SWM               ;AFTER A MISS
+        /CLK16* SWM*  /MRAS                     ;CLK16 SYNC
+  HLDA* /ADSM*  D-C*  /MRAS                     ;DMA
+  HLDA* /ADSM* /D-C*   MRAS*  YY                ;REFRESH START
+  HLDA* /ADSM* /D-C*   SWM*   DMIO              ;REFRESH HOLD
+  HLDA* /ADSM*  DMIO*  SWM*  /MRAS              ;REFRESH END

YY :=
  /HLDA*  CLK16* ADSM*  MRDY* /W-R* M32* /HIT   ;CPU PIPE TO MEMORY MISS
+ /HLDA*  CLK16* ADSM*  MRDY*  D-C* M32* /HIT   ;CPU PIPE TO MEMORY MISS
+ /HLDA*         NAM*   MRAS                    ;OR WHEN LATCH NEEDS CLOSED
+ /HLDA* /CLK16* YY                             ;CLK16 SYNC
+  HLDA*  D-C*  MCAS* DMIO* /ADSM               ;DMA
+  HLDA*        YY*   DMIO* /ADSM               ;DMA,REFRESH HOLD TO END
+  HLDA* /D-C*  MRAS* DMIO* /ADSM* /SWM* CLK16   ;REFRESH

NAM :=
  /HLDA*  CLK16* ADSM*  MRDY* /W-R* M32*  HIT   ;CPU PIPE TO MEMORY HIT
+ /HLDA*  CLK16* ADSM*  MRDY*  D-C* M32*  HIT   ;CPU PIPE TO MEMORY HIT
+ /HLDA*  CLK16* SWM*  /ADSM* /NAM              ;AFTER AN IDLE OR MISS
+        /CLK16* NAM                            ;CLK16 SYNC
+  HLDA*                /ADSM                   ;DURING REFRESH AND DMA

MRDY :=
  /HLDA*  CLK16* NAM* MRAS                      ;AFTER NA WILL BE READY
+ /HLDA* /CLK16* MRDY                          ;CLK16 SYNC

MRAS :=
  /HLDA* SWM*  /ADSM* /NAM              ;OUT OF A MISS OR IDLE OPERATION
+ /HLDA* MRAS* /MRDY                    ;TILL MRDY
+ /HLDA* MRAS* /CLK16                   ; AND TILL CLK16 UNLESS
+ /HLDA* MRAS*  ADSM* /W-R* M32* HIT    ;CPU PIPE HIT
+ /HLDA* MRAS*  ADSM*  D-C* M32* HIT    ;CPU PIPE HIT
+  HLDA* DMIO* /ADSM* /D-C* /SWM* CLK16 ;REFRESH
+  HLDA* DMIO* /ADSM* /D-C* /SWM* MRAS  ;REFRESH HOLD
+  HLDA* DMIO* /ADSM*  D-C* M32* /YY    ;DMA

MCAS :=
  /HLDA*  CLK16* NAM* MRD*  MRAS        ;AFTER NA WILL BE CAS FOR READ
+ /HLDA* /CLK16* MCAS                   ;CLK16 SYNC
+ /HLDA* /CLK16* MRDY* MWE              ;AFTER START OF MRDY IS WRITE CAS
+  HLDA* /ADSM*  D-C* DMIO* MRAS* /SWM  ;DMA START
+  HLDA* /ADSM*  D-C* DMIO* MCAS*  MRD  ;DMA READ HOLD TILL END

MWE :=
  /HLDA* /CLK16* NAM* D-C* W-R* M32* MRAS       ;CPU WRITE TO MEMORY
+ /HLDA* /CLK16* MWE                           ;CLK16 SYNC
+ /HLDA*  CLK16* MWE* NAM
+  HLDA* /W-R* DMIO* /ADSM* M32* /YY           ;DMA WRITE
+  HLDA*  MWE* DMIO* /ADSM                     ;DMA WRITE HOLD

MRD :=
```

```
  /HLDA* /CLK16* NAM* /W-R* M32* MRAS                    ;CPU READ FROM MEMORY
+ /HLDA* /CLK16* MRD                                     ;CLK16 SYNC
+ /HLDA*  CLK16* MRD* NAM
+  HLDA*  W-R* DMIO* D-C* /ADSM* M32* MRAS                ;DMA READ (NOT REFRESH)
+  HLDA*  MRD* DMIO*       /ADSM                         ;DMA READ HOLD


FUNCTION TABLE

CLK /CLK16 /OE /ADSM /DMIO  D-C  W-R  /M32  HLDA  /HIT
/MRAS /SWM /MCAS /NAM /MRDY /MWE  /MRD  /YY
;  /
;C C   / /           /   /   /
;L L   A D     / H / M / M / M / /
;K K / D M D W M L H R S C N R M M /
;3 1 0 S I - - 3 D I A W A A D W R Y
;2 6 E M O C R 2 A T S M S M Y E D Y
-------------------------------------------------------------------------
 C L L L H H H H H H  H H H H H H H H  RESET
 C H L L H L L L L L  H H H H H H H H
 C L L L H L L L L L  H L H H H H H H  MEM READ INITIAL
 C H L H H L L L L L  L L H H H H H H
 C L L H H L L L L L  L H H L H H H H
 C H L H H L L L L L  L H H L H H L L
 C L L H H L L L L H  L H L H L H L L
 C H L L H L L L L L  L H L H L H L L
 C L L L H L L L L L  L H H L H H H H  READ HIT STARTS
 C H L H H L L L L L  L H H L H H L L
 C L L H H L L L L L  L H L H L H L L
 C H L L H L L L L H  L H L H L H L L
 C L L L H L L L L H  H H H H H H H L  READ MISS STARTS
 C H L H H L L L L H  H H H H H H H L
 C L L H H L L L L H  H L H H H H H H
 C H L H H L L L L H  L L H H H H H H
 C L L H H L L L L L  L H H L H H H H
 C H L H H L L L L L  L H H L H H L L
 C L L H H L L L L H  L H L H L H L L
 C H L L H H H L L L  L H L H L H L L
 C L L L H H H L L L  L H H L H H H H  WRITE HIT STARTS
 C H L H H H H L L L  L H H L H L H L
 C L L H H H H L L L  L H H H L L H L
 C H L L H H H L L H  L H L H L L H L
 C L L L H H H L L H  H H H H H H H L  WRITE MISS STARTS
 C H L H H H H L L H  H H H H H H H L
 C L L H H H H L L H  H L H H H H H H
 C H L H H H H L L H  L L H H H H H H
 C L L H H H H L L L  L H H L H H H H
 C H L H H H H L L L  L H H L H L H L
 C L L H H H H L L H  L H H H L L H L
 C H L H H H H L L L  L H L H L L H L
 C L L H H H H L L L  H H H H H H H H  IDLE CYCLE
 C H L L H H H L L L  H H H H H H H H
 C L L L H H H L L L  H L H H H H H H  WRITE INITIAL OUT OF A LONGGG PIPE
 C H L L H H H L L L  H L H H H H H H
 C L L L H H H L L L  H L H H H H H H
 C H L H H H H L L L  L L H H H H H H
 C L L H H H H L L L  L H H L H H H H
 C H L H H H H L L L  L H H L H L H L
 C L L H H H H L L H  L H H H L L H L
 C H L H H H H L L L  L H L H L L H L
 C L L H H H H L L L  H H H H H H H H  IDLE CYCLE
 C H L L H H H L L L  H H H H H H H H
 C L L L H H H L L L  H L H H H H H H  WRITE INITIAL OUT OF A LONGGG PIPE
 C H L L H H H L L L  H L H H H H H H
 C L L L H H H L L L  H L H H H H H H
 C H L H H H H L L L  L L H H H H H H
 C L L H H H H L L L  L H H L H H H H
 C H L H H H H L L L  L H H L H L H L
 C L L H H H H L L H  L H H H L L H L
 C H L H H H H L L L  L H L H L L H L
 C L L H H H H L L L  H H H H H H H H  IDLE CYCLE
 C H L L H H H L L L  H L H L H H H H
```

```
 C L L H H L H L H L  H H H L H H H H
 C H L H H L H L H L  H H H L H H H H
 C L L H L L H H H H  L H H L H H H H  REFRESH
 C H L H L L H H H H  L H H L H H H H
 C L L H L L H H H H  L H H L H H H L
 C H L H L L H H H H  L L H L H H H L
 C L L H L L H H H H  H L H L H H H L
 C H L H L L H H H H  H L H L H H H L
 C L L H H L H H H H  H H H L H H H H
 C H L H H H L H H H  H L H L H H H H
 C L L H L H H H H H  H L H L H H H H  DMA READ ELSEWHERE
 C H L H L H H L H H  L L H L H H H H  DMA READ
 C L L H L H H L H H  L H H L H H L H
 C H L H L H H L H H  L H L L H H L H
 C L L H L H H L H H  L H L L H H L L
 C H L H L H L L H H  H H L L H H L L
 C L L H L H L L H H  H L L L H H L L
 C H L H H H L L H H  H L H L H H H H
;  /
;C C   / /           /   /   /
;L L   A D     / H /  M / M / M / /
;K K / D M D W M L H  R S C N R M M /
;3 1 0 S I - - 3 D I  A W A A D W R Y
;2 6 E M O C R 2 A T  S M S M Y E D Y
 C L L H H H L H H H  H L H L H H H H
 C H L H L H L H H H  H L H L H H H H  DMA WRITE ELSEWHERE
 C L L H L H L L H H  L L H L H L H H  DMA WRITE
 C H L H L H L L H H  L H H L H L H H
 C L L H L H L L H H  L H L L H L H H
 C H L H L H L L H H  L H L L H L H L
 C L L H L H L L H H  H H L L H L H L
 C H L H L H H L H H  H L H L H L H L
 C L L H L H H L H H  H L H L H L H L
 C H L H H H H L H H  H L H L H H H H
 C L L H H H L L H H  H L H L H H H H
 C H L H H H L L L H  H L H L H H H H
 C L L H H H L L L H  H H H H H H H H
```

DESCRIPTION

This PAL is used in the D4 (386) memory board to control the DRAM subsystem. The RAS and CAS master strobes are generated, and the CPU next address and READY signals are provided.
Rev A of this PAL changes the DMA state machine to prevent spurious RAM cycles after refresh or DMA cycles.

```
PAL16L8B                                              PAL DESIGN SPECIFICATION
D4-RM32 108053-001                                    PAUL R. CULLEY    04/02/86
D4 PAGE RAM BOARD M32 decode logic
Copyright Compaq Computer Houston, Texas 1986

A31  A23   A22   A21   A20   A19   A18  A17  FA20  GND
/2M /M32A /M32B /ROM  /512K /640K /1M  /8M  /M32C  VCC

IF (/A22 * /A21) M32A =
  /A31*/A23*/A22*/A21*/A20*/A19*/A18                    ;000000-03FFFF 256K
+ /A31*/A23*/A22*/A21*     /A19*/A18*   /FA20          ;000000-03FFFF 256K
+ /A31*/A23*/A22*/A21*/A20*/A19* A18*      512K       ;040000-07FFFF 256K
+ /A31*/A23*/A22*/A21*/A20* A19*/A18*/A17* 640K       ;080000-09FFFF 128K
+ /A31*/A23*/A22*/A21*/A20* A19* A18* A17* ROM        ;0E0000-0FFFFF 128K
+ /A31*/A23*/A22*/A21* A20*                 1M        ;100000-1FFFFF 1M
+ /A31* A23*/A22*/A21*                      8M        ;800000-9FFFFF 2M

IF (A22 * /A21) M32B =
  /A31*/A23* A22*/A21*                      8M        ;400000-5FFFFF 2M
+  A31* A23* A22*/A21*/A20*/A19*/A18*/A17               ;DIAG 8000000h 128K

IF (A21) M32C =
  /A31* A23* A22* A21* A20*/A19* A18*     /512K       ;F40000-F7FFFF 256K
+ /A31* A23* A22* A21* A20* A19*/A18*/A17*/640K       ;F80000-F9FFFF 128K
+ /A31* A23* A22* A21* A20* A19*/A18* A17             ;FA0000-FBFFFF 128K
+ /A31* A23* A22* A21* A20* A19* A18                  ;FC0000-FFFFFF 256K
+ /A31*/A23* A22* A21*                      8M        ;600000-7FFFFF 2M
+ /A31*/A23*/A22* A21*                      2M        ;200000-3FFFFF 2M


FUNCTION TABLE

A31 A23 A22 A21 A20 A19 A18 A17 FA20 /512K /640K /1M /2M /8M /ROM
/M32A /M32B /M32C
;
;                                  / / /
;                    F             M M M
;A A A A A A A A A  5 6             R  3 3 3
;3 2 2 2 2 1 1 1 2  1 4           1 2 8 0  2 2 2
;1 3 2 1 0 9 8 7 0  2 0           M M M M  A B C
-------------------------------------------------------------------------
 H H H L L L L L L  L L L L L L   Z L Z  DIAG
 H L H L H L L L L  L L L L L L   Z H Z  OFF
 H L H H L L L L H  H L L L L L   Z Z H  OFF
 H L L L L L L L H  L L L L L L   H Z Z  OFF
 L L L L L L L L H  L L L L L L   L Z Z  256K
 L L L L H L L L L  L L L L L L   L Z Z  256K
 L L L L L L H L L  L L L L L L   L Z Z  512K
 L L L L L H L L L  L L L L L L   L Z Z  640K
 L L L L L H H H L  L L L L L L   L Z Z  128K AT 0E0000h
 L H H H H L H L L  H L L L L L   Z Z L  256K AT F40000h
 L H H H H H L L L  H H L L L L   Z Z L  128K AT F80000h
 L H H H H H L H L  L L L L L L   Z Z L  128K AT FA0000h
 L H H H H H H L L  L L L L L L   Z Z L  256K AT FC0000h
 L L L L H H H H H  L L L L L L   L Z Z  1M AT 100000h
 L L L H L L L L L  L L L L L L   Z Z L  2M AT 200000h
 L L H L L L L L L  L L L L L L   Z L Z  2M AT 400000h
 L L H H L L L L L  L L L L L L   Z Z L  2M AT 600000h
 L H L L L L L L L  L L L L L L   L Z Z  2M AT 800000h
 L H L L L L L L L  L L L L H L   H Z Z  2M AT 800000h OFF
 L L L H L L L L L  L L L H L L   Z Z H  2M AT 200000h OFF
 L L L L H L L L H  L L H L L L   H Z Z  1M AT 100000h OFF
 . . . . . . . . .  . . . . . .   . . .  128K AT 0E0000h OFF
```

DESCRIPTION

This PAL is used in the D4 (386) memory board to decode addresses within the memory space and assert the M32* signal. It does all the decoding for all the expected options according to the following jumper settings.

```
512K 640K                                   1M
H    H 256K    000000-03FFFFh               H       NO EXTENDED MEMORY
L    H 512K    000000-07FFFFh               L       1024K   100000-1FFFFFh
L    L 640K    000000-9FFFFFh
H    L  ****   ILLEGAL

8M 2M
H  H   OK
H  L   2048K   200000-3FFFFFh
L  H   6144K   400000-9FFFFFh  (NOTE: The 8 Meg board asserts both 8M and 2M
L  L   8192K   200000-9FFFFFh   strobes)
```

When FA20 is low, the address line A20 should be considered to be low.
When FA20 is high, A20 is decoded as usual.
The above set of m32 outputs are wire ORed to form the signal M32*. The actual equation for M32 is shown below.

```
M32 =
  /A31*/A23*/A22*/A21*/A20*/A19*/A18                ;000000-03FFFF 256K
+ /A31*/A23*/A22*/A21*     /A19*/A18*   /FA20      ;000000-03FFFF 256K
+ /A31*/A23*/A22*/A21*/A20*/A19* A18*      512K    ;040000-07FFFF 256K
+ /A31*/A23*/A22*/A21*/A20* A19*/A18*/A17* 640K    ;080000-09FFFF 128K
+ /A31*/A23*/A22*/A21*/A20* A19* A18* A17* ROM     ;0E0000-0FFFFF 128K
+ /A31* A23* A22* A21* A20*/A19* A18*     /512K    ;F40000-F7FFFF 256K
+ /A31* A23* A22* A21* A20* A19*/A18*/A17*/640K    ;F80000-F9FFFF 128K
+ /A31* A23* A22* A21* A20* A19*/A18* A17          ;FA0000-FBFFFF 128K
+ /A31* A23* A22* A21* A20* A19* A18               ;FC0000-FFFFFF 256K
+ /A31*/A23*/A22*/A21* A20*                 1M     ;100000-1FFFFF 1M
+ /A31*/A23*/A22* A21*                      2M     ;200000-3FFFFF 2M
+ /A31*/A23* A22*/A21*                      8M     ;400000-5FFFFF 2M
+ /A31*/A23* A22* A21*                      8M     ;600000-7FFFFF 2M
+ /A31* A23*/A22*/A21*                      8M     ;800000-9FFFFF 2M
+  A31* A23* A22*/A21*/A20*/A19*/A18*/A17           ;DIAG 80C0000h 128K
```

PAL16L8B
D4-RRAS 108054-001
D4 PAGE RAM BOARD RAS decode logic

PAL DESIGN SPECIFICATION
PAUL R. CULLEY - 05/20/86

```
 A31   A23  A22  A21  A20  A19    A18    A17  FA20 GND
-/RFSH /RS0 /MWE /MRD /WE0 /PARRD /PARWR /ROM /RS1  VCC

RS0 =
  /A31* /A23* /A22* /A21* /A20* /A19                          ;00000000H 512K
+ /A31* /A23* /A22* /A21* /FA20* /A19                         ;00100000H 512K
+ /A31* /A23* /A22* /A21* /A20*  A19* /A18* /A17              ;00080000H 128K
+ /A31* /A23* /A22* /A21* /A20*  A19*  A18*  A17              ;000E0000H 128K
+ /A31*  A23*  A22*  A21*  A20                                ;00F00000H 1024K
+  RFSH                                                              ; REFRESH

RS1 =
  /A31* /A23* /A22* /A21*  A20* FA20                          ;00100000H 1024K
+  RFSH                                                              ; REFRESH

PARWR =
  MWE* A31*  A23*  A22* /A21* /A20* /A19* /A18* /A17          ;80C00000H 128K

PARRD =
  MRD* A31*  A23*  A22* /A21* /A20* /A19* /A18* /A17          ;80C00000H 128K

WE0 =
 MWE*/A31* /A23* /A22* /A21*       /A19                      ;00000000H 512K
+MWE*/A31* /A23* /A22* /A21* /A20*  A19* /A18* /A17           ;00080000H 128K
+MWE*/A31* /A23* /A22* /A21* /A20*  A19*  A18*  A17* /ROM     ;000E0000H 128K
+MWE*/A31*  A23*  A22*  A21*  A20* /A19*  A18                 ;00F40000H 256K
+MWE*/A31*  A23*  A22*  A21*  A20*  A19* /A18                 ;00F80000H 256K
+MWE*/A31*  A23*  A22*  A21*  A20*  A19*  A18* /A17           ;00FC0000H 128K
+MWE*/A31*  A23*  A22*  A21*  A20*  A19*  A18*  A17* /ROM     ;00FE0000H 128K

FUNCTION TABLE

A31 A23 A22 A21 A20 A19 A18 A17 FA20 /ROM /MWE /MRD /RFSH
/RS0 /RS1 /PARWR /PARRD /WE0
;
;                          /      P P
;                  F /  / / R  / / A A /
;A A A A A A A A A R  M M F  R R R R W
;3 2 2 2 2 1 1 1 2 0  W R S  S S W R E
;1 3 2 1 0 9 8 7 0 M  E D H  0 1 R D 0
--------------------------------------------------------------------------
 L L L L L L L L H L  L H H  L H H H L 000000H 512K
 L L L L H L L L L L  L H H  L H H H L 100000H 512K
 L L L L L H L L H L  L H H  L H H H L 080000H 128K
 L L L L L H H H H L  L H H  L H H H H 0E0000H 128K
 L L L L L H H H H H  L H H  L H H H L 0E0000H 128K
 L H H H H L H L H L  L H H  L H H H L F40000H 256K
 L H H H H H L L H L  L H H  L H H H L F80000H 256K
 L H H H H H H L H L  L H H  L H H H L FC0000H 128K
 L H H H H H H H H L  L H H  L H H H H FE0000H 128K
 L H H H H H H H H H  L H H  L H H H L FE0000H 128K
 L L L L H L L L H L  H H H  H L H H H 100000H 1024K
 H H H L L L L L H L  L H H  H H L H H 80C00000H 128K
 H H H L L L L L H L  H L H  H H H L H 80C00000H 128K
 H H H H H H H H H L  H H L  L L H H H REFRESH
--------------------------------------------------------------------------
```

DESCRIPTION

This PAL is used in the D4 (386) memory board to decode the RAS signals and the parity read and write logic.

```
NOWS*       9C8,12B8
OSC         7A1,12B8
OSC32*      7A8
PA31        2D1, 3D8, 4A8,11B8,13A8
PA<23:2>    2B1, 3D8,11B8,13C8
PAGES*      5D8, 7B1
PARIT*      7D8,13A8
PBRD*       6A8, 7B1
PBWR*       6A8, 7B1
PCLK*       6C8, 7A1
PD<31:0>    2D8, 4D8,11C8,13C8
PEREQ       2D8,11D1
PWGOOD      7A8,13D1
RDETEC      6A1, 8A1
READY*      2A1, 7D8,11B8
REFCK       6A1, 7B8, 8B8
REFEN*      8A1, 9C8
REFRS       6D8, 8A1
REFRS*      4B8, 5D8, 8A1,10A8,12C8
RES287      7D1,11C8
RESCP       2B8, 7B8, 8C1
RESCP*      8C1
RESCPU*     2A1,11B8
RESDRV      5D8,12C8,13D1
RRD         8A8
RST*        3A8, 6A8, 7C8, 8C8, 9B8,10A8,11A8,13D1,13A8
RSTAR*      6C1, 8C8
SA<19:0>    3C1, 5B1, 7D8, 9C1,10D8,12D8
SD<15:0>    4C1,10C1,12A8,12D8
SHTD*       4A1, 8C8
SLOWH*      6D1, 8C8
SMRDC*      4B1,12B8
SMWTC*      4B1,12B8
T-C         5D1,12C8
T00         3A8, 9A1
T10         3A8, 9A1
TIM1S*      6C8, 7D1
TIM2S*      6D8, 7D1
TIMCLK      6D8, 7A1
TMLD        7A1
TST1        3A8, 4A8
TST3        4A8
W-R         2B1, 3D8, 4A8,11B8,13A8
WDEN*       3B8, 9B1
XA<8:0>     4B1, 5C1, 6C8, 7D8,10A8,11C8
XIORC*      5C8, 6C8, 7B8, 8D8,11C8
XIOWC*      5C8, 6C8, 7B8, 8D8,11C8
XMWTC*      5C8, 8D8
ZC32        2A8
ZCK16*      2A1, 4A8
ZDS32I      7A8
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Title: SCHEMATIC-DP3E DEC 16, 1986
Drawing: 000559-000 REV: X

C	1	13C3
C	2	13C4
C	3	13C4
C	4	13C3
C	5	13C5
C	6	13C4
C	7	13C5
C	8	13C5
C	9	7B8
C	10	14D8
C	11	14D8
C	12	14D7
C	13	14D7
C	14	14D6
C	15	14D6
C	16	14D5
C	17	14D5
C	18	14D4
C	19	14D4
C	20	12C2
C	21	14D3
C	22	7B6
C	23	14D2
C	24	14D1
C	25	14D8
C	26	14D8
C	27	14D7
C	28	14D7
C	29	14D6
C	30	14D6
C	31	14D5
C	32	14D5
C	33	14D4
C	34	14D4
C	35	14D3
C	36	14D3
C	37	14D2
C	38	14D2
C	39	14D1
C	40	14C8
C	41	14C8
C	42	14C7
C	43	14C7
C	44	14C6
C	45	14C6
C	46	14C5
C	47	14C5
C	48	14C4
C	49	14C4
C	50	14C3
C	51	14C3
C	52	14C2
C	53	14C2
C	54	14C1
C	55	14B8
C	56	14B8
C	57	14B7
C	58	14B7

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C  60    9A2
C  61   14B5
C  62   14B5
C  63   14B4
C  64   14B4
C  65   14B3
C  66   14B3
C  67   14B2
C  68   14B2
C  69   14B1
C  70   14B8
C  71   14B8
C  72   14B7
C  73   14B7
C  74   14B6
C  75   14B6
C  76   14B5
C  77   14B5
C  78   14B4
C  79   14B4
C  80   14B3
C  81   14B3
C  82   14B2
C  83    7A6
C  84   14B1
C  85   14A8
C  86   14A8
C  87   14A7
C  88   14A7
C  89   14A6
C  90   14A6
C  91   14A5
C  92   14A5
C  93   14A4
C  94   14A4
C  95   14A3
C  96   14A3
C  97    2A7
C  98   14A2
C  99   14A1
C 100    7A8
C 101    7A4
C 102   14A8
C 103   14A8
C 104   14A7
C 105   14A7
C 106   14A6
C 107   14A6
C 108   14A5
C 109   14A5
C 110   14A4
C 111   14A4
C 112   14A3
C 113   14A3
C 114    6B2
C 115    6B1
C 116    6A4
C 117    7A7
C 118   14A2
C 119   14A2
CR  1    7B6
CR  2    7B6
```

CR 4	13A2
ER 1	10C8
ER 2	10B8
ER1-1	10D8
ER1-2	10C8
ER1-3	10C8
ER2-1	10C8
ER2-2	10C8
ER2-3	10B8
F 1	13B3
F 2	6C1
J 101	13D6
J 102	12D7
J 103	12D6
J 104	12D5
J 105	12D5
J 106	12D4
J 107	12D4
J 108	12D3
J 109	13B5
J 110	13A5
J 111	13B4
J 112	13A4
J 113	13A2
J 115	6A3
J 116	6B1
J 117	13B2
J 118	7B5
J 119	6C1
J 121	13A5
J 123	12B6
J 124	12B5
J 125	12B5
J 126	12B4
J 127	12B4
L 1	9B3
L	6B1
L 3	6B1
L 4	6B1
L 5	6C1
PCB .	1A3
Q 1	7B7
R 1	7B7
R 2	7B7
R 3	7B8
R 4	7A2
R 5	12B2
R 6	12B2
R 7	13A2
R 8	7A4
R 9	1
R 10	9D8
R 11	3B8
R 12	12D6
R 13	5C4
R 14	13D5
R 15	13D4
R 16	7C7
R 17	7A4
R 18	7A7
R 19	7A4
R 20	7A6

R	22	6D4
R	23	10A[illegible]
R	24	6B3
R	25	9D[illegible]
R	26	[illegible]D3
R	27	10A[illegible]
R	28	10B[illegible]
R	29	9B5
R	30	4A8
R	31	2C4
R	32	5A4
R	33	2B[illegible]
R	34	2A4
R	35	2A4
R	36	[illegible]A6
R	37	2A6
R	38	[illegible]46
R	[illegible]	[illegible]
R	40	[illegible]7
R	41	1[illegible]
R	42	[illegible]A8
R	43	10[illegible]
R	44	[illegible]
RP	1	1[illegible]
RP	2	[illegible]B2
RP	3	1[illegible]
RP	4	[illegible]D2
RP	5	1[illegible]
RP	6	5D8, 5D8, 8D7
RP	7	13B7
RP	8	6B[illegible], 6B2, 6B2, 6C2, 6D2, 6D3, 6D3
SW	1	6D2
U	1	6[illegible]7
U	2	[illegible]7
U	3	4[illegible]
[illegible]	4	[illegible]2
U	[illegible]	[illegible]
[illegible]	6	[illegible]4
U	7	7[illegible], 8A3
U	8	4C7
U	9	4D7
U	10	4C4
U	11	4[illegible]4
U	12	[illegible]A3
U	13	10A4, 10A5
U	14	[illegible]C3
U	15	10[illegible], 10D5
U	16	[illegible]A2
U	17	4[illegible]
[illegible]	[illegible]	[illegible]
U	[illegible]	[illegible]
U	[illegible]	[illegible]3
U	2[illegible]	4[illegible]
[illegible]	[illegible]	[illegible]7
U	2[illegible]	[illegible]
[illegible]	[illegible]	[illegible]5
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]6	[illegible]2
U	2[illegible]	[illegible]
U	[illegible]	[illegible]
U	[illegible]	1[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

U 82 3B6
U 83 3C7
U 84 9C4
U 85 3C3
U 86 11D3
U 87 5 , 9D2
U 88 4A6
U 89 8C5
U 90 4B4
U 91 3B7
U 92 11C5
U 93 11C , 11D7
U 94 4D5
U 95 6C5
U 96 4B3
U 97 4A , 4B2, 8A2, 8D6
U 98 3B5, 5C2, 5A5,10A5
U 4
U 97
U 5
U 5D2
U 5 , 5D4, 5D4, 9A7
U 4 5D4, 5B5, 5D6, 5D7
U 5 5 , 5A5, 5D5, 6C2, 7A4, 8A3
U 96 9A4
U 5
U 5A3 A5
U 5 2
U 60 1B3
U 61 7C , 7C6
U 62 9C5, 8B3
U 63 7C , 9D4
U 64 9B2
U 65 8B3, 8D3, 8B5, 8C5
U 66 8C5, 7A1, 8A3, 8D5
C 9C4
A7
U 6 2A5
C2, 7C3
U 7 8C , 6D4, 9B2, 9B2
72 8C2, 8C4
U 7 2C , 8D2, 8B3, 8A6
U 74 9B5, 9B5, 9B8,13D2
U 7 3A7, 2A7, 2A7, 2A7
U 76 9B3, 2D3
U 77 7A5
78 8B3, 6B3
U 7 9C , 8C7
80 84
5 , 8A6
, 9A2
U 8 9C ,11A5
4 A7,11A6
8
U 7 , 7A7, 7A8, 7B8,13D3,13D4
U 87 10A2
U 8 6C4, 8C2, 8D2, 8A8
89 8A4, 8A5, 8A7, 8A7
U 90 8B6, 8B7
U 91 6B2, 6C2, 7C7, 8A2,10B2,10B2
U 92 2B6, 5B5, 9A7
U 93 6A4

PA<31:2>	2B1, 3C8
PARCK	2B1, 3A1
PARIT*	2A1, 4A1
PARRD*	3A1, 4A8
PARWR*	2D8, 3A1, 4B8
RAS0A*	4C1, 5C8, 6C8
RAS0B*	4C1, 7C8, 8C8
RAS1A*	4C1, 5B8, 6B8
RAS1B*	4C1, 7B8, 8B8
RFSH*	2A1, 3A8, 9B8
ROM*	3B8, 4A1
RS0*	3A1, 4C8
RS1*	3B1, 4C8
RST*	2A1, 4B8
SWM*	3A8, 4D1
TST	4D8
TST0	4A1, 9D8
TST1*	2D8, 3B1, 4D1
TST2*	3D8, 4D1
W-R	2A1, 4D8
WE0*	3A1, 5D8
WPRT*	3A1, 4A1

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Drawing: 000414-000 REV: A

C	1	10D8
C	2	10D7
C	3	10D7
C	4	10D7
C	5	10D6
C	6	10D6
C	7	10D5
C	8	10D5
C	9	10D4
C	10	10D4
C	11	10A8
C	12	10D3
C	13	10A7
C	14	10D2
C	15	10D2
C	16	10D2
C	17	10A7
C	18	10D1
C	19	10A6
C	20	10D8
C	21	10A6
C	22	10D7
C	23	10D7
C	24	10D7
C	25	10D6
C	26	10D6
C	27	10D5
C	28	10D5
C	29	10D4
C	30	10D4
C	31	10D3
C	32	10D3
C	33	10D2
C	34	10D2
C	35	10D2
C	36	10D1
C	37	10C8
C	38	10C7
C	39	10C7
C	40	10C7
C	41	10C6
C	42	10C6
C	43	10C5
C	44	10C5
C	45	10C4
C	46	10C4
C	47	10C3
C	48	10C3
C	49	10C2
C	50	10C2
C	51	10C2
C	52	10C1
C	53	10C8
C	54	10C7
C	55	10C7
C	56	10C7
C	57	10C6
C	58	10C6

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C  60     10C5
C  61     10C4
C  62     10C4
C  63     10C3
C  64     10C3
C  65     10C2
C  66     10C2
C  67     10C2
C  68     10C1
C  69     10C8
C  70     10C7
C  71     10C7
C  72     10C7
C  73     10C6
C  74     10C6
C  75     10C5
C  76     10C5
C  77     10C4
C  78     10C4
C  79     10C3
C  80     10C3
C  81     10C2
C  82     10C2
C  83     10C2
C  84     10C1
C  85     10B8
C  86     10B7
C  87     10B7
C  88     10B7
C  89     10B6
C  90     10B6
C  91     10B5
C  92     10B5
C  93     10B4
C  94     10B4
C  95     10A5
C  96     10A5
C  97     10A4
C  98     10A4
C  99     10A3
C 100     10A3
C 101     10A2
E   1      3A8
E   2      3A7
E   3      3A7
E 123      3A7
J 301      9A7
J 302      9A5
P 101      2D8
P 121      9C4
PCB .      1A2
R   1      4C7
R   2      4C7
RP  1      5D7
RP  2      5B7, 5D7
RP  3      5B7
RP  4      4B2, 4B2, 4B2, 4B2, 4C2, 4C2, 4C2, 4C2
RP  5      4A6
RP  6      2C3, 2C4, 2C6, 2C7, 4D3, 4D3, 4D8, 9A8, 9A8
RP  7      4A2
RP  8      4A3
RP  9      4A5
U   1      4A5  9D3
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Title: D4 PAGE DRAM BOARD AUG 06, 1986
Drawing: 000414-000 REV: A

1M*	3A8, 4A8
2M*	3B8, 4A8, 9B8
512K*	3B8, 4A8
640K*	3B8, 4A8
8M*	3A8, 9B8
ADS*	2A1
ADSM*	2B1, 4C8
BA<31:11>	3D1, 9B8
BE*<3:0>	2A1, 3A8
CAS0*	4B1, 5B8, 5C8
CAS1*	4B1, 6B8, 6C8
CAS2*	4B1, 7B8, 7C8
CAS3*	4B1, 8B8, 8C8
CLAT	3A8, 4D1
CLK16*	2A1, 4D8
CLK32	2A1, 4C8
CS*	3A1, 4C8, 9B8
D-C	2A1, 4D8
DMIO	2B1, 4D8
EQ1*	3D1, 4D8
EQ2*	3C1, 4D8
ER*<3:0>	2C1, 4A8
F20	2B1, 3C8
HLDA	2A1, 4D8
LOWA20	2A1
M-IO	2A1
M0	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M1	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M2	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M3	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M32*	2A1, 3B1, 4D8
M4	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M5	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M6	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M7	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
M8	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
MA<9:0>	3D1, 5B8, 5D8, 9C8
MCAS*	4D1, 9B8
MD<31:0>	2D1, 4A1, 5A8, 5C8, 6A8, 6C8, 7A8, 7C8, 8A8, 8C8, 9D8
MRAS*	3C8, 4D1, 9B8
MRD*	2D8, 3A8, 4D1
MRDY*	2A1, 4D1
MW	5D1, 6D1, 6D8, 7D1, 7D8, 8D1, 8D8
MWE*	3A8, 4D1, 5B8, 9B8
N0	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
N1	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
N2	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
N3	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
N4	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
N5	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
N6	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
N7	5C1, 6C1, 6C8, 7C1, 7C8, 8C1, 8C8
N8	5C1, 6C1, 6C8, 7C1, 7C8, 8C1, 8C8
NAM*	2A1, 4D1
NW	5B1, 6B1, 6B8, 7B1, 7B8, 8B1, 8B8
P0	5A1, 5C1
P1	6A1, 6C1
P2	7A1, 7C1
P3	8A1, 8C1

U	2	2A5, 2A6
U	3	2A2, 2B2, 3A2, 4D7
U	4	4C6
U	5	3D7
U	6	3D5
U	7	3A7
U	8	4B5, 4B5
U	9	2A3, 2B3, 4D2, 4D2, 4D6, 4D7
U	10	3A4, 3A4, 3A4, 3A4
U	11	3A5
U	12	3B5
U	13	3C7
U	14	3C5
U	15	3D2
U	16	3C2
U	17	3B2
U	18	3A2
U	19	4B3, 4B3, 4B3, 4B3
U	20	2B2, 4A7
U	21	2B2, 2B4, 2B5, 2B6
U	22	5D7
U	23	5B7
U	24	4C3, 4C3, 4C3, 4C3
U	25	2C3, 2C4, 2C6, 2C7
U	26	2C7
U	27	4A7
U	28	2C2
U	29	2C4
U	30	2C5
U	31	5C6
U	32	5C5
U	33	5C5
U	34	5C4
U	35	5C4
U	36	5C3
U	37	5C2
U	38	5C2
U	39	5C1
U	40	6C6
U	41	6C5
U	42	6C5
U	43	6C4
U	44	6C4
U	45	6C3
U	46	6C2
U	47	6C2
U	48	6C1
U	49	7C6
U	50	7C5
U	51	7C5
U	52	7C4
U	53	7C4
U	54	7C3
U	55	7C2
U	56	7C2
U	57	7C1
U	58	8C6
U	59	8C5
U	60	8C5
U	61	8C4
U	62	8C4
U	63	8C3

U	65	8C2
U	66	8C1
U	67	5A6
U	68	5A5
U	69	5A5
U	70	5A4
U	71	5A4
U	72	5A3
U	73	5A2
U	74	5A2
U	75	5A1
U	76	6A6
U	77	6A5
U	78	6A5
U	79	6A4
U	80	6A4
U	81	6A3
U	82	6A2
U	83	6A2
U	84	6A1
U	85	7A6
U	86	7A5
U	87	7A5
U	88	7A4
U	89	7A4
U	90	7A3
U	91	7A2
U	92	7A2
U	93	7A1
U	94	8A6
U	95	8A5
U	96	8A5
U	97	8A4
U	98	8A4
U	99	8A3
U	100	8A2
U	101	8A2
U	102	8A1

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D4 MOTHER BOARD SCHEMATIC Drawing No: 000559-000 Rev: X

Item	Qty	Part Number	Description	Ref Des		
16	1	101262-001	XTAL, MINTR,32.768KHz	Y	2	
42	1	100144-002	IC, PRGML INTRPT CONTR..8259-2	U	1	
42	1	100144-002	IC, PRGML INTRPT CONTR..8259-2	U	2	
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	3	
99	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U	4	
101	1	101653-001	IC, CNTR.....74LS590	U	5	
34	1	100195-005	XTAL, OSCR,14.31818mHZ	U	6	
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	7	AB
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	8	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	9	
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	10	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	11	
105	1	100079-008	SCKT, IC,LO PF,28P,.600	U	12	
105	1	100079-008	SCKT, IC,LO PF,28P,.600	U	13	S
61	1	108328-001	ASSY, EPROM, MEM #2 [EVEN]	U	13	
105	1	100079-008	SCKT, IC,LO PF,28P,.600	U	14	
105	1	100079-008	SCKT, IC,LO PF,28P,.600	U	15	S
62	1	108327-001	ASSY, EPROM,MEM #1 [ODD]	U	15	
52	1	102605-001	IC, 4-BIT BIN CNTR....74ALS163	U	16	
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	17	
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	18	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	19	
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	20	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	21	
40	1	100147-001	IC, DMA CONTR.....8237	U	22	
40	1	100147-001	IC, DMA CONTR.....8237	U	23	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	24	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	25	
99	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U	26	
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	27	
98	1	105672-001	IC, QD BUS XCVR.....74LS243	U	28	
72	1	108135-001	ASSY, IC,PAL,D4-SROMA....16L8A	U	29	
102	1	101649-001	IC, MEM MAPPER.....74LS612	U	30	
65	1	108394-001	ASSY, IC,PAL,D4-SCMDD....16L8B	U	31	
67	1	108396-001	ASSY, IC,PAL,D4-SDEND....16L8A	U	32	
100	1	100129-001	IC, OCT BUS XCVR.....74LS245	U	33	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	34	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	35	
36	1	108066-001	XTAL, OSCR,24.000mHz,CMOS	U	36	
99	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U	37	AB
63	1	105645-001	ASSY, IC,PAL,D4-SADI.....16L8B	U	38	
54	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	39	
99	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U	40	
99	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U	41	
106	1	100079-009	SCKT, IC,LO PF,40P,.600	U	42	
90	1	108223-001	IC, DL J(K) F/F.....74HC109	U	43	AB
41	1	101592-001	IC, PRGML INTVL TIMER.....8254	U	44	
41	1	101592-001	IC, PRGML INTVL TIMER.....8254	U	45	
66	1	108395-001	ASSY, IC,PAL,D4-SCPYD....16L8A	U	46	
95	1	100131-001	IC, QD GATED BFR.....74LS125	U	47	ABCD
95	1	100131-001	IC, QD GATED BFR.....74LS125	U	48	ABCD
96	1	100135-001	IC, 3-8 L DCDR/DMUXR...74LS138	U	49	
97	1	100151-001	IC, QD D-TYPE F/F.....74LS175	U	50	
99	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U	51	
70	1	105657-001	ASSY, IC,PAL,D4-SNCP.....16L8A	U	52	

Item	Qty	Part Number	Description	Ref Des		
50	1	101628-001	IC, QD 2-INP AND GATE..74ALS08	U	53	ABCD
47	1	101632-001	IC, QD 2-INP NAND GATE.74ALS00	U	54	ABCD
49	1	101636-001	IC, HEX INV.....74ALS04	U	55	ABCDEF
73	1	108219-001	ASSY, IC,PAL,D4-STATB....20R8A	U	56	
53	1	108221-001	IC, OCT D-TYPE F/F....74ALS273	U	57	
64	1	108393-001	ASSY, IC,PAL,D4-SADOD....20R4A	U	58	
82	1	101639-001	IC, QD 2-1 D SEL/MUXR...74F257	U	59	
108	1	108398-001	SCKT, IC,68 PIN PGA	U	60	
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	61	AB
94	1	100132-001	IC, AND-OR-INVERT GATE..74LS51	U	62	AB
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	63	AB
71	1	105659-001	ASSY, IC,PAL,D4-SPPI.....16L8A	U	64	
81	1	101156-001	IC, QD D-TYPE F/F.....74F175	U	65	ABCD
47	1	101632-001	IC, QD 2-INP NAND GATE.74ALS00	U	66	ABCD
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	67	AB
69	1	108397-001	ASSY, IC,PAL,D4-SMSDD....16R4C	U	68	
80	1	100527-001	IC, DL D-TYPE F/F.....74F74	U	69	AB
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	70	AB
77	1	101170-001	IC, QD NAND GATE.....74F00	U	71	ABCD
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	72	AB
78	1	101158-001	IC, QD 2-INP AND GATE....74F08	U	73	ABCD
81	1	101156-001	IC, QD D-TYPE F/F.....74F175	U	74	ABCD
91	1	108222-001	IC, QD GATED BFR.....74HC125	U	75	ABCD
109	1	106148-001	SCKT, IC,132 PIN,PGA	U	76	S
44	1	105674-002	IC, 32-BIT MICROPRCSR.80386-16	U	76	
46	1	101646-001	IC, REAL TIME CLK.....MC146818	U	77	
107	1	100079-012	SCKT, IC,LD PF,40P,.600W,CLR	U	78	S
60	1	102720-004	ASSY, IC,KYBD INTFC-M	U	78	
80	1	100527-001	IC, DL D-TYPE F/F.....74F74	U	79	AB
74	1		SPARE IC LOCATION 14 PIN	U	80	
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	81	AB
80	1	100527-001	IC, DL D-TYPE F/F.....74F74	U	82	AB
80	1	100527-001	IC, DL D-TYPE F/F.....74F74	U	83	AB
80	1	100527-001	IC, DL D-TYPE F/F.....74F74	U	84	AB
37	1	100195-013	XTAL, OSCR,32mHz	U	85	
39	1	101647-001	IC, HEX INV.....4069	U	86	ABCDEF
68	1	108360-001	ASSY, IC,PAL,D4-SKEY.....16R4A	U	87	
48	1	101656-001	IC, QD 2-INP NOR GATE..74ALS02	U	88	ABCD
81	1	101156-001	IC, QD D-TYPE F/F.....74F175	U	89	ABCD
51	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	90	AB
55	1	108361-001	IC, HEX BFR,OPEN COL.74ALS1035	U	91	ABCDEF
79	1	101631-001	IC, TPL 3-INP AND GATE...74F11	U	92	ABC
43	1	100181-001	IC, DL PRPHL NAND DRVR...75477	U	93	
75	1	100278-001	SW, REC RKR DIP,8POS	SW	1	
32	1	100200-002	RNET, 8.2K OHM,6PIN SIP,5RES	RP	1	
38	1	100200-010	RNET, 300 OHM,6 PIN SIP,5RES	RP	2	
33	1	100201-001	RNET, 8.2K OHM,10 PIN SIP,9RES	RP	3	
33	1	100201-001	RNET, 8.2K OHM,10 PIN SIP,9RES	RP	4	
33	1	100201-001	RNET, 8.2K OHM,10 PIN SIP,9RES	RP	5	
33	1	100201-001	RNET, 8.2K OHM,10 PIN SIP,9RES	RP	6	FG
35	1	100201-009	RNET, 20K OHM,10 PIN SIP,9RES	RP	7	
7	1	100083-030	RES, 8.2K OHM,1/4W,5%,CF	RP	8	ABCDEFG
30	1	100198-023	RES, 2.87K OHM,1/4W,1%,MF	R	1	
31	1	100198-002	RES, 3.48K OHM,1/4W,1%,MF	R	2	
24	1	100083-034	RES, 270 OHM,1/4W,5%,CF	R	3	

Item	Qty	Part Number	Description	Ref Des
15	1	100083-019	RES, 30 OHM,1/4W,5%,CF	R 4
5	1	100083-026	RES, 1K OHM,1/4W,5%,CF	R 5
6	1	100083-032	RES, 4.7K OHM,1/4W,5%,CF	R 6
25	1	100083-044	RES, 360 OHM,1/4W,5%,CF	R 7
15	1	100083-019	RES, 30 OHM,1/4W,5%,CF	R 8
21	1	100083-012	RES, 100 OHM,1/4W,5%,CF	R 9
22	1	100083-056	RES, 180 OHM,1/4W,5%,CF	R 10
22	1	100083-056	RES, 180 OHM,1/4W,5%,CF	R 11
5	1	100083-026	RES, 1K OHM,1/4W,5%,CF	R 12
22	1	100083-056	RES, 180 OHM,1/4W,5%,CF	R 13
12	1	100083-009	RES, 20K OHM,1/4W,5%,CF	R 14
7	1	100083-030	RES, 8.2K OHM,1/4W,5%,CF	R 15
5	1	100083-026	RES, 1K OHM,1/4W,5%,CF	R 16
14	1	100083-085	RES, 22MEG OHM,1/4W,5%,CF	R 17
26	1	100083-051	RES, 470K OHM,1/4W,5%,CF	R 18
7	1	100083-030	RES, 8.2K OHM,1/4W,5%,CF	R 19
5	1	100083-026	RES, 1K OHM,1/4W,5%,CF	R 20
5	1	100083-026	RES, 1K OHM,1/4W,5%,CF	R 21
7	1	100083-030	RES, 8.2K OHM,1/4W,5%,CF	R 22
12	1	100083-009	RES, 20K OHM,1/4W,5%,CF	R 23
5	1	100083-026	RES, 1K OHM,1/4W,5%,CF	R 24
15	1	100083-019	RES, 30 OHM,1/4W,5%,CF	R 25
15	1	100083-019	RES, 30 OHM,1/4W,5%,CF	R 26
6	1	100083-032	RES, 4.7K OHM,1/4W,5%,CF	R 27
6	1	100083-032	RES, 4.7K OHM,1/4W,5%,CF	R 28
22	1	100083-056	RES, 180 OHM,1/4W,5%,CF	R 29
22	1	100083-056	RES, 180 OHM,1/4W,5%,CF	R 30
19	1	100083-003	RES, 68 OHM,1/4W,5%,CF	R 31
23	1	100083-059	RES, 200 OHM,1/4W,5%,CF	R 32
19	1	100083-003	RES, 68 OHM,1/4W,5%,CF	R 33
13	1	100083-001	RES, 22 OHM,1/4W,5%,CF	R 34
13	1	100083-001	RES, 22 OHM,1/4W,5%,CF	R 35
19	1	100083-003	RES, 68 OHM,1/4W,5%,CF	R 36
18	1	100083-020	RES, 51 OHM,1/4W,5%,CF	R 37
19	1	100083-003	RES, 68 OHM,1/4W,5%,CF	R 38
8	1	100083-008	RES, 10K OHM,1/4W,5%,CF	R 39
8	1	100083-008	RES, 10K OHM,1/4W,5%,CF	R 40
12	1	100083-009	RES, 20K OHM,1/4W,5%,CF	R 41
22	1	100083-056	RES, 180 OHM,1/4W,5%,CF	R 42
3	1	100111-001	RES, 0 OHM	R 43
20	1	100199-004	RES, 68 OHM,1/2W,5%,CC	R 44
110	1	100234-001	IC, REG,SH,2%,50PPM/C.....431	Q 1
45	1	000560-001	PCB, DP3E, 80386 SYSTEM BOARD	PCB.
27	1	101374-001	FERRITE BEAD, W/LEAD	L 1
83	1	101374-001	FERRITE BEAD, W/LEAD	L 2
83	1	101374-001	FERRITE BEAD, W/LEAD	L 3
83	1	101374-001	FERRITE BEAD, W/LEAD	L 4
83	1	101374-001	FERRITE BEAD, W/LEAD	L 5
59	1	100224-003	CONN, PCB STD EDGE,40/80	J 101
58	1	100224-001	CONN, PCB STD EDGE,31/62	J 102
58	1	100224-001	CONN, PCB STD EDGE,31/62	J 103
58	1	100224-001	CONN, PCB STD EDGE,31/62	J 104
58	1	100224-001	CONN, PCB STD EDGE,31/62	J 105
58	1	100224-001	CONN, PCB STD EDGE,31/62	J 106
58	1	100224-001	CONN, PCB STD EDGE,31/62	J 107

Item	Qty	Part Number	Description	Ref Des	
58	1	100224-001	CONN, PCB STD EDGE,31/62	J	108
103	1	100218-001	HDR, PCB,1ROW,5POS,STR POST	J	109
103	1	100218-001	HDR, PCB,1ROW,5POS,STR POST	J	110
103	1	100218-001	HDR, PCB,1ROW,5POS,STR POST	J	111
103	1	100218-001	HDR, PCB,1ROW,5POS,STR POST	J	112
87	1	105609-004	HDR, 1ROW,5POS,KEY 4POS,STR	J	113
85	1	105609-002	HDR, 1ROW,4POS,KEY 2POS,STR	J	115
88	1	105609-006	HDR, 1ROW,7POS,KEY 5POS,STR	J	116
104	1	101329-001	HDR, 20POS,.156CTR,.045SQ POST	J	117
86	1	105607-001	HDR, 1ROW,KEY 2POS,STR	J	118
84	1	100186-006	HDR, PCB,1ROW,2POS,STR POST	J	119
56	1	108122-001	CONN, PCB STD EDGE,3/6	J	121
57	1	100224-002	CONN, PCB STD EDGE,18/36	J	123
57	1	100224-002	CONN, PCB STD EDGE,18/36	J	124
57	0	100224-002	CONN, PCB STD EDGE,18/36	J	125
57	1	100224-002	CONN, PCB STD EDGE,18/36	J	126
57	1	100224-002	CONN, PCB STD EDGE,18/36	J	127
76	1	101270-004	FUSE, SUB MINTR,5.0A,125V	F	1
76	1	101270-004	FUSE, SUB MINTR,5.0A,125V	F	2
92	0	100081-001	JMPR, PCB,2 POS	ER	1-3
92	0	100081-001	JMPR, PCB,2 POS	ER	1-2
92	0	100081-001	JMPR, PCB,2 POS	ER	1-1
89	0	100186-010	HDR, PCB,1ROW,9POS,STR POST	ER	1
92	0	100081-001	JMPR, PCB,2 POS	ER	2-3
92	0	100081-001	JMPR, PCB,2 POS	ER	2-2
92	0	100081-001	JMPR, PCB,2 POS	ER	2-1
89	0	100186-010	HDR, PCB,1ROW,9POS,STR POST	ER	2
29	1	100192-001	DIODE, GENL PRP.....1N914B	CR	1
29	1	100192-001	DIODE, GENL PRP.....1N914B	CR	2
29	1	100192-001	DIODE, GENL PRP.....1N914B	CR	3
93	1	100254-001	DIODE, LED,RED DIFFUSED	CR	4
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	1
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	2
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	3
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	4
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	5
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	6
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	7
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	8
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	9
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	10
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	11
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	12
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	13
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	14
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	15
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	16
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	17
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	18
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	19
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C	20
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	21
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C	22
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	23
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C	24

Item	Qty	Part Number	Description	Ref Des
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 25
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 26
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 27
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 28
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 29
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 30
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 31
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 32
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 33
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 34
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 35
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 36
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 37
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 38
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 39
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 40
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 41
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 42
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 43
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 44
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 45
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 46
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 47
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 48
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 49
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C 50
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 51
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 52
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 53
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 54
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 55
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 56
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 57
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 58
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 59
17	1	100085-024	CAP, 47PF,50V,10%,COG	C 60
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 61
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 62
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 63
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 64
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 65
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 66
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 67
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 68
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 69
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 70
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 71
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 72
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 73
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 74
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 75
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 76
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 77
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 78
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C 79

Item	Qty	Part Number	Description	Ref Des
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 80
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 81
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 82
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 83
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 84
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 85
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 86
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 87
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 88
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 89
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 90
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 91
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 92
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 93
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C 94
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 95
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C 96
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C 97
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 98
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 99
9	1	100085-013	CAP, 10PF,50V,10%,COG	C 100
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 101
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 102
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 103
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 104
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 105
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 106
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 107
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C 108
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 109
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 110
1	1	100085-007	CAP, .001MFD,50V,20%,X7R	C 111
2	1	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C 112
10	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 113
17	1	100085-024	CAP, 47PF,50V,10%,COG	C 114
17	1	100085-024	CAP, 47PF,50V,10%,COG	C 115
28	1	100085-006	CAP, .01MFD,50V,20%,Z5U	C 116
11	1	100085-014	CAP, 18PF,50V,10%,COG	C 117
4	1	108242-001	CAP, .05MFD,DECOUPLING,PGA/LCC	C 118
4	1	108242-001	CAP, .05MFD,DECOUPLING,PGA/LCC	C 119

Total parts = 306 Total holes = 3317

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D4 MOTHER BOARD SCHEMATIC Drawing No: 000559-000 Rev: X

Item	Qty	Part Number	Description	Ref Des
1	8	100085-007	CAP, .001MFD,50V,20%,X7R	C20,50,79,94,96,97,108,111
2	88	100085-009	CAP, .047MFD,50V,-20/+80%,Z5U	C2,4,6,8,10,11,13-19,23-42,44-49,51-56,58,59,61,63-68,70-74,76-78,80-85,87-93,95,98,99,101-107,109,110,112
3	1	100111-001	RES, 0 OHM	R43
4	2	108242-001	CAP, .05MFD,DECOUPLING,PGA/LCC	C118,119
5	6	100083-026	RES, 1K OHM,1/4W,5%,CF	R5,12,16,20,21,24
6	3	100083-032	RES, 4.7K OHM,1/4W,5%,CF	R6,27,28
7	4	100083-030	RES, 8.2K OHM,1/4W,5%,CF	R15,19,22,8
8	2	100083-008	RES, 10K OHM,1/4W,5%,CF	R39,40
9	1	100085-013	CAP, 10PF,50V,10%,COG	C100
10	15	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C1,3,5,7,9,12,21,22,43,57,62,69,75,86,113
11	1	100085-014	CAP, 18PF,50V,10%,COG	C117
12	3	100083-009	RES, 20K OHM,1/4W,5%,CF	R14,23,41
13	2	100083-001	RES, 22 OHM,1/4W,5%,CF	R34,35
14	1	100083-085	RES, 22MEG OHM,1/4W,5%,CF	R17
15	4	100083-019	RES, 30 OHM,1/4W,5%,CF	R4,8,25,26
16	1	101262-001	XTAL, MINTR,32.768KHz	Y2
17	3	100085-024	CAP, 47PF,50V,10%,COG	C60,114,115
18	1	100083-020	RES, 51 OHM,1/4W,5%,CF	R37
19	4	100083-003	RES, 68 OHM,1/4W,5%,CF	R31,33,36,38
20	1	100199-004	RES, 68 OHM,1/2W,5%,CC	R44
21	1	100083-012	RES, 100 OHM,1/4W,5%,CF	R9
22	6	100083-056	RES, 180 OHM,1/4W,5%,CF	R10,11,13,29,30,42
23	1	100083-059	RES, 200 OHM,1/4W,5%,CF	R32
24	1	100083-034	RES, 270 OHM,1/4W,5%,CF	R3
25	1	100083-044	RES, 360 OHM,1/4W,5%,CF	R7
26	1	100083-051	RES, 470K OHM,1/4W,5%,CF	R18
27	1	101374-001	FERRITE BEAD, W/LEAD	L1
28	1	100085-006	CAP, .01MFD,50V,20%,Z5U	C116
29	3	100192-001	DIODE, GENL PRP.....1N914B	CR1-3
30	1	100198-023	RES, 2.87K OHM,1/4W,1%,MF	R1
31	1	100198-002	RES, 3.48K OHM,1/4W,1%,MF	R2
32	1	100200-002	RNET, 8.2K OHM,6PIN SIP,5RES	RP1
33	4	100201-001	RNET, 8.2K OHM,10 PIN SIP,9RES	RP3-6
34	1	100195-005	XTAL, OSCR,14.31818mHZ	U6
35	1	100201-009	RNET, 20K OHM,10 PIN SIP,9RES	RP7
36	1	108066-001	XTAL, OSCR,24.000mHz,CMOS	U86
37	1	100195-013	XTAL, OSCR,32mHz	U85
38	1	100200-010	RNET, 300 OHM,6 PIN SIP,5RES	RP2
39	1	101647-001	IC, HEX INV.....4069	U86
40	2	100147-001	IC, DMA CONTR.....8237	U22,23
41	2	101592-001	IC, PRGML INTVL TIMER.....8254	U44,45
42	2	100144-002	IC, PRGML INTRPT CONTR..8259-2	U1,2
43	1	100181-001	IC, DL PRPHL NAND DRVR...75477	U93
44	1	105674-002	IC, 32-BIT MICROPRCSR.80386-16	U76

Item	Qty	Part Number	Description	Ref Des
45	1	000560-001	PCB, DP3E, 80386 SYSTEM BOARD	PCB.
46	1	101646-001	IC, REAL TIME CLK.....MC146818	U77
47	2	101632-001	IC, QD 2-INP NAND GATE.74ALS00	U54,66
48	1	101656-001	IC, QD 2-INP NOR GATE..74ALS02	U88
49	1	101636-001	IC, HEX INV.....74ALS04	U55
50	1	101628-001	IC, QD 2-INP AND GATE..74ALS08	U53
51	8	101637-001	IC, DL D-TYPE F/F.....74ALS74	U7,61,63,67,70,72, 81,90
52	1	102605-001	IC, 4-BIT BIN CNTR....74ALS163	U16
53	1	108221-001	IC, OCT D-TYPE F/F....74ALS273	U57
54	9	101633-001	IC, OCT D-TYPE LCH....74ALS573	U9,11,19,21,24,25, 34,35,39
55	1	108361-001	IC, HEX BFR,OPEN COL.74ALS1035	U91
56	1	108122-001	CONN, PCB STD EDGE,3/6	J121
57	4	100224-002	CONN, PCB STD EDGE,18/36	J123,124,(J125), 126,127
58	7	100224-001	CONN, PCB STD EDGE,31/62	J102-108
59	1	100224-003	CONN, PCB STD EDGE,40/80	J101
60	1	102720-004	ASSY, IC,KYBD INTFC-M	U78
61	1	108328-001	ASSY, EPROM, MEM #2 [EVEN]	U13
62	1	108327-001	ASSY, EPROM,MEM #1 [ODD]	U15
63	1	105645-001	ASSY, IC,PAL,D4-SADI.....16L8B	U38
64	1	108393-001	ASSY, IC,PAL,D4-SADOD....20R4A	U58
65	1	108394-001	ASSY, IC,PAL,D4-SCMDD....16L8B	U31
66	1	108395-001	ASSY, IC,PAL,D4-SCPYD....16L8A	U46
67	1	108396-001	ASSY, IC,PAL,D4-SDEND....16L8A	U32
68	1	108360-001	ASSY, IC,PAL,D4-SKEY.....16R4A	U87
69	1	108397-001	ASSY, IC,PAL,D4-SMSCD....16R4C	U68
70	1	105657-001	ASSY, IC,PAL,D4-SNCP.....16L8A	U52
71	1	105659-001	ASSY, IC,PAL,D4-SPPI.....16L8A	U64
72	1	108135-001	ASSY, IC,PAL,D4-SROMA....16L8A	U29
73	1	108219-001	ASSY, IC,PAL,D4-STATB....20R8A	U56
74	1		SPARE IC LOCATION 14 PIN	U80
75	1	100278-001	SW, REC RKR DIP,8POS	SW1
76	2	101270-004	FUSE, SUB MINTR,5.0A,125V	F1,2
77	1	101170-001	IC, QD NAND GATE.....74F00	U71
78	1	101158-001	IC, QD 2-INP AND GATE....74F08	U73
79	1	101631-001	IC, TPL 3-INP AND GATE...74F11	U92
80	5	100527-001	IC, DL D-TYPE F/F.....74F74	U69,79,82-84
81	3	101156-001	IC, QD D-TYPE F/F.....74F175	U65,74,89
82	1	101639-001	IC, QD 2-1 D SEL/MUXR...74F257	U59
83	4	101374-001	FERRITE BEAD, W/LEAD	L2-5
84	1	100184-006	HDR, PCB,1ROW,2POS,STR POST	J119
85	1	[illegible]	HDR, 1ROW,KEY 3POS,STR	J115
86	1	105607-001	HDR, 1ROW,KEY 2POS,STR	J118
87	1	105609-004	HDR, 1ROW,5POS,KEY 4POS,STR	J113
88	1	105609-006	HDR, 1ROW,7POS,KEY 5POS,STR	J116
89	2	100184-010	HDR, PCB,1ROW,9POS,STR POST	(ER1),(ER2)
90	1	108223-001	IC, DL J(K) F/F.....74HC109	U43
91	1	108222-001	IC, QD GATED BFR.....74HC125	U75
92	9	100061-001	JMPR, PCB,2 POS	(ER1-1),(ER1-2), (ER1-3),(ER2-1), (ER2-2),(ER2-3)

Item	Qty	Part Number	Description	Ref Des
93	1	100254-001	DIODE, LED,RED DIFFUSED	CR4
94	1	100132-001	IC, AND-OR-INVERT GATE..74LS51	U62
95	2	100131-001	IC, QD GATED BFR.....74LS125	U47,48
96	1	100135-001	IC, 3-8 L DCDR/DMUXR...74LS138	U49
97	1	100151-001	IC, QD D-TYPE F/F.....74LS175	U50
98	1	105672-001	IC, QD BUS XCVR.....74LS243	U28
99	6	100091-001	IC, OCT BFR/L DRVR.....74LS244	U4,26,37,40,41,51
100	8	100129-001	IC, OCT BUS XCVR.....74LS245	U3,8,10,17,18,20, 27,33
101	1	101653-001	IC, CNTR.....74LS590	U5
102	1	101649-001	IC, MEM MAPPER.....74LS612	U30
103	4	100218-001	HDR, PCB,1ROW,5POS,STR POST	J109-112
104	1	101329-001	HDR, 20POS,.156CTR,.045SQ POST	J117
105	4	100079-008	SCKT, IC,LO PF,28P,.600	U12-15
106	1	100079-009	SCKT, IC,LO PF,40P,.600	U42
107	1	100079-012	SCKT, IC,LO PF,40P,.600W,CLR	U78
108	1	108398-001	SCKT, IC,68 PIN PGA	U60
109	1	106148-001	SCKT, IC,132 PIN,PGA	U76
110	1	100234-001	IC, REG,SH,2%,50PPM/C.....431	Q1

Total parts = 306 Total holes = 3317

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D4 PAGE DRAM BOARD SCHEMATIC Drawing No: 000414-000 Rev: A

Item	Qty	Part Number	Description	Ref Des
1	89	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C1-10,12,14-16,18,20,22-94
2	12	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C11,13,17,19,21,95-101
3	1	100083-022	RES, 150 OHM,1/4W,5%,CF	R1
4	1	100083-034	RES, 270 OHM,1/4W,5%,CF	R2
5	4	100201-005	RNET, 4.7K 10 PIN SIP 9RES	RP5,7-9
6	1	100201-001	RNET, 8.2K OHM,10 PIN SIP,9RES	RP6
7	4	100203-001	RNET, 33 OHM,16PIN DIP,8RES	RP1-4
8	36	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U31-66
9	2	108022-001	IC, 10 BIT BUFFER.....29827	U22,23
10	1	000415-001	PCB, D4 PAGE DRAM BOARD	PCB.
11	1	101628-001	IC, QD 2-INP AND GATE..74ALS08	U10
12	2	101637-001	IC, DL D-TYPE F/F.....74ALS74	U1,8
13	2	101633-001	IC, OCT D-TYPE LCH....74ALS573	U6,14
14	1	108352-001	ASSY, IC,PAL,D4-RCTLA....16R8C	U4
15	1	108053-001	ASSY, IC,PAL,D4-RM32.....16L8C	U7
16	1	108054-001	ASSY, IC,PAL,D4-RRAS.....16L8B	U18
17	1	101170-001	IC, QD NAND GATE.....74F00	U25
18	1	101214-001	IC, HEX INV.....74F04	U9
19	3	101157-001	IC, QD 2-INP OR GATE.....74F32	U3,19,24
20	1	100527-001	IC, DL D-TYPE F/F.....74F74	U2
21	3	101640-001	IC, QD 2-1 D SEL/MUXR...74F158	U15-17
22	1	101156-001	IC, QD D-TYPE F/F.....74F175	U21
23	2	108024-001	IC, OCTAL EQUAL CMP.....74F521	U5,13
24	2	108023-001	IC, OCTAL LATCH.....74F573	U11,12
25	4	108015-001	IC, OCTAL PARITY XCVR...74F657	U26,28-30
26	1	100186-010	HDR, PCB,1ROW,9POS,STR POST	E123
27	2	108010-001	HDR, PCB,2ROW,40POS,STR,BKAWY	J301,302
28	3	100081-001	JMPR, PCB,2 POS	E1-3
29	1	101187-001	IC, 4-INP NAND GATE.....74LS20	U20
30	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U27
31	1		PCB GOLD FINGERS	P101
32	36	100079-003	SCKT, IC,LO PF,16P,.300	U67-102

Total parts = 222 Total holes = 2109

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D4 PAGE DRAM BOARD SCHEMATIC Drawing No: 000414-000 Rev: A

Item	Qty	Part Number	Description	Ref Des		
12	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	1	AB
20	1	100527-001	IC, DL D-TYPE F/F.....74F74	U	2	AB
19	1	101157-001	IC, QD 2-INP OR GATE.....74F32	U	3	ABCD
14	1	108352-001	ASSY, IC,PAL,D4-RCTLA....16R8C	U	4	
23	1	108024-001	IC, OCTAL EQUAL CMP.....74F521	U	5	
13	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	6	
15	1	108053-001	ASSY, IC,PAL,D4-RM32.....16L8C	U	7	
12	1	101637-001	IC, DL D-TYPE F/F.....74ALS74	U	8	AB
18	1	101214-001	IC, HEX INV.....74F04	U	9	ABCDEF
11	1	101628-001	IC, QD 2-INP AND GATE..74ALS08	U	10	ABCD
24	1	108023-001	IC, OCTAL LATCH.....74F573	U	11	
24	1	108023-001	IC, OCTAL LATCH.....74F573	U	12	
23	1	108024-001	IC, OCTAL EQUAL CMP.....74F521	U	13	
13	1	101633-001	IC, OCT D-TYPE LCH....74ALS573	U	14	
21	1	101640-001	IC, QD 2-1 D SEL/MUXR...74F158	U	15	
21	1	101640-001	IC, QD 2-1 D SEL/MUXR...74F158	U	16	
21	1	101640-001	IC, QD 2-1 D SEL/MUXR...74F158	U	17	
16	1	108054-001	ASSY, IC,PAL,D4-RRAS.....16L8B	U	18	
19	1	101157-001	IC, QD 2-INP OR GATE.....74F32	U	19	ABCD
29	1	101187-001	IC, 4-INP NAND GATE.....74LS20	U	20	AB
22	1	101156-001	IC, QD D-TYPE F/F.....74F175	U	21	ABCD
9	1	108022-001	IC, 10 BIT BUFFER.....29827	U	22	
9	1	108022-001	IC, 10 BIT BUFFER.....29827	U	23	
19	1	101157-001	IC, QD 2-INP OR GATE.....74F32	U	24	ABCD
17	1	101170-001	IC, QD NAND GATE.....74F00	U	25	ABCD
25	1	108015-001	IC, OCTAL PARITY XCVR...74F657	U	26	
30	1	100091-001	IC, OCT BFR/L DRVR.....74LS244	U	27	
25	1	108015-001	IC, OCTAL PARITY XCVR...74F657	U	28	
25	1	108015-001	IC, OCTAL PARITY XCVR...74F657	U	29	
25	1	108015-001	IC, OCTAL PARITY XCVR...74F657	U	30	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	31	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	32	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	33	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	34	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	35	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	36	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	37	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	38	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	39	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	40	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	41	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	42	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	43	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	44	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	45	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	46	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	47	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	48	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	49	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	50	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	51	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	52	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	53	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	54	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	55	

Item	Qty	Part Number	Description	Ref Des		
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	56	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	57	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	58	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	59	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	60	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	61	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	62	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	63	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	64	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	65	
8	1	108021-001	IC, D-RAM,256K,100nS,FAST PAGE	U	66	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	67	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	68	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	69	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	70	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	71	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	72	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	73	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	74	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	75	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	76	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	77	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	78	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	79	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	80	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	81	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	82	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	83	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	84	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	85	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	86	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	87	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	88	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	89	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	90	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	91	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	92	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	93	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	94	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	95	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	96	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	97	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	98	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	99	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	100	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	101	
32	1	100079-003	SCKT, IC,LO PF,16P,.300	U	102	
7	1	100203-001	RNET, 33 OHM,16PIN DIP,8RES	RP	1	
7	1	100203-001	RNET, 33 OHM,16PIN DIP,8RES	RP	2	AB
7	1	100203-001	RNET, 33 OHM,16PIN DIP,8RES	RP	3	
7	1	100203-001	RNET, 33 OHM,16PIN DIP,8RES	RP	4	ABCDEFGH
5	1	100201-005	RNET, 4.7K 10 PIN SIP 9RES	RP	5	
6	1	100201-001	RNET, 8.2K OHM,10 PIN SIP,9RES	RP	6	ABCDEFGHI
5	1	100201-005	RNET, 4.7K 10 PIN SIP 9RES	RP	7	
5	1	100201-005	RNET, 4.7K 10 PIN SIP 9RES	RP	8	

Item	Qty	Part Number	Description	Ref Des
5	1	100201-005	RNET, 4.7K 10 PIN SIP 9RES	RP 9
3	1	100083-022	RES, 150 OHM,1/4W,5%,CF	R 1
4	1	100083-034	RES, 270 OHM,1/4W,5%,CF	R 2
10	1	000415-001	PCB, D4 PAGE DRAM BOARD	PCB.
31	1		PCB GOLD FINGERS	P 101
27	1	108010-001	HDR, PCB,2ROW,40POS,STR,BKAWY	J 301
27	1	108010-001	HDR, PCB,2ROW,40POS,STR,BKAWY	J 302
28	1	100081-001	JMPR, PCB,2 POS	E 1
28	1	100081-001	JMPR, PCB,2 POS	E 2
28	1	100081-001	JMPR, PCB,2 POS	E 3
26	1	100186-010	HDR, PCB,1ROW,9POS,STR POST	E 123
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 1
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 2
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 3
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 4
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 5
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 6
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 7
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 8
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 9
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 10
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 11
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 12
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 13
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 14
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 15
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 16
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 17
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 18
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 19
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 20
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 21
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 22
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 23
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 24
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 25
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 26
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 27
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 28
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 29
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 30
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 31
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 32
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 33
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 34
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 35
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 36
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 37
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 38
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 39
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 40
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 41
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 42
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 43
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 44

Item	Qty	Part Number	Description	Ref Des
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 45
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 46
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 47
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 48
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 49
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 50
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 51
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 52
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 53
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 54
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 55
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 56
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 57
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 58
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 59
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 60
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 61
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 62
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 63
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 64
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 65
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 66
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 67
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 68
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 69
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 70
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 71
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 72
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 73
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 74
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 75
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 76
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 77
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 78
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 79
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 80
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 81
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 82
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 83
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 84
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 85
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 86
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 87
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 88
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 89
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 90
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 91
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 92
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 93
1	1	101240-001	CAP, .1MFD,50V,20%,AXIAL,CER M	C 94
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 95
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 96
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 97
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 98
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 99

Item	Qty	Part Number	Description	Ref Des
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 100
2	1	100082-005	CAP, 10MFD,16V,20%,TANTALUM	C 101

Total parts = 222 Total holes = 2109

D3PE (80386) PROCESSOR BOARD CIRCUIT DESCRIPTIONS

DIFFERENCES FROM ORIGINAL D4 PROCESSOR:

*** addition of an 80387 coprocessor socket

*** addition of a 80287/80387 selection switch

*** addition of a keyboard processor enhancement PAL

*** bus timing changes to improve compatibility

*** DESIGN ASSUMPTIONS:

*** 80386, 80387 or 80287 processor combination.

*** 16mHz 80386 processor clock.

*** 16mHz 80387 numeric coprocessor clock.

*** 4mHz (compatible) or 8mHz 80287 coprocessor clock.

*** 8mHz 286 compatible expansion bus.

*** 4.00 mhz DMA subsystem clock.

*** Standard RAM accesses are 32 bit when CPU requests.

*** Seven bus slots have a compatible edge connector which can be used by standard IBM-PC peripherals.

*** Four bus slots have a second connector which will allow specially designed peripherals to access additional address lines and the rest of the 16 bit data bus. In addition several more interrupt and DMA request lines will be available. This connector is Deskpro 286 compatible.

*** 15 Interrupt request lines.

*** Total of 7 DMA request lines (3 word channels and 4 byte channels).

*** System bus runs a refresh cycle 256 times in 4 milliseconds.

*** Special cards with a second bus connector will be able to do 16 bit memory or I/O operations by asserting a specific line and working with the eight additional data signals.

*** All software addresses are to be compatible with IBM PC-AT.

*** Variable system speed control via software.

HARDWARE DIFFERENCES FROM IBM PCAT (Includes MEMORY Board)

*** All RAM is located on an expansion board. This uses one slot that is not used in the PCAT. Parity checking on the memory is done as though it was a standard expansion board memory, a parity error shows up as an I/O check (parity check 2) with a testable bit on port 61h bit 6 to indicate the error. Port 61h bit 7 is used for an additional timer interrupt input. Port 61h bit 2 output (used to control the parity check on the PCAT) is used to enable the additional timer to the NMI processor input.

*** The memory size of the main system is not testable by the software. On the IBM PCAT, the 8042 pin 31 was connected to the motherboard 256/512k byte jumper to allow testing the memory configuration. On the D4-Motherboard, this bit is connected to a configuarable jumper.

*** The ROM configuration allows for four ROMs. Standard decoding sets these up as two banks of 32k words (16 bits), or 64k bytes, with each pair of ROMs split into evenly addressed bytes in one ROM, and odd addressed bytes in the other. The standard ROMs (in the high bank) will be 2 x 16k bytes, however, decoded such that they will appear twice in the 64kbyte space. The PCAT uses two 32k ROMs to completely fill the 64k space.

*** The keyboard processor (8042) input clock is connected to a 7.1591 Mhz reference source. The clock reference for the 8042 on the PCAT is connected to a 6MHz reference. The keyboard processor has been enhanced by the addition of a PAL which intercepts and interprets the A20 control sequence much more rapidly than the 8042 could.

*** Processor clock speed will be full time very fast (16mHz). The execution speed is greater than that of the 286 products. Programs requiring a specific speed may not work.

*** The 80386 CPU does not respond to certain opcodes in the same way that the 80286 does. Programs using these opcodes may not work.

*** The bus clock is not always at 8mHz. It is re-synchronized with the CPU for each bus cycle to simulate the timing of a 286 product.

*** The NMI mask register for Parity Check 1 is changed to allow/disallow interrupts from a special additional timer to be used for watchdog purposes.

*** There is an additional timer to be used for watchdog purposes in software. The address for this timer is located in one of the "PHANTOM" spaces for the original system timer.

The system refresh counter has been extended to 10 bits. Also the bottom two bits are copied from address lines 0 and 1 to 8 and 9. This simplifies the interface of megabit DRAMs and the 32 bit memory board.

*** References to the 32 bit memory board do not appear on the compatible expansion bus. This will prevent the operation of hardware debugging aids developed for the 80286 products.

*** The 80287 coprocessor interface to the main processor is different. Some of the pins defined in the INTEL 80287 specification are not connected as specified. Only recent 80287 revisions will work properly. Any other "strange" hardware devices that connect to the 80287 socket may not work.

*** The 80387 coprocessor is slightly different than the 80287. Also the software reset control of the 80387 is not connected.

HARDWARE INCOMPATIBILITIES WITH DESKPRO 286

*** Most of the above incompatibilities apply to comparisons with the DESKPRO 286.

*** Speed switching by jumper or software is supported differently. The 8042 speed control bits are connected differently and are used only to disable the speed circuit entirely.

The majority of this document assumes a working knowledge of standard digital logic techniques and parts, and an understanding of the 80386 processor IC in particular. The following documents contain information necessary to understand this design in detail:

INTEL 80386 hardware reference manual
INTEL 8237 data sheet
INTEL 8254 data sheet
INTEL 8259 data sheet
Motorola MC146818 CMOS Clock data sheet

SYSTEM CLOCK CIRCUITS

The system clocks are seperated into three sections. One is the CPU clock (32mHz) for the 80386 and it's associated circuits. Another is the 24mHz clock which is used for the numeric coprocessor. The third is the 14.31818mHz clock which provides software compatible system timing functions, a fixed frequency signal on the expansion bus, and the 8042 keyboard processor clock reference.

32mHz 80386/80387 CLOCK

The CPU clock is provided by a crystal oscillator, CMOS buffer IC (74HC125), and an F74 flip-flop. There are three outputs from these circuits, a 32mHz processor clock, a 16mHz reference clock (CLK16, CLK16*) (which has the same phase as the internal CPU clock), and reset signals which meets the setup and hold time requirements for the 80386 and 80387. The 80386 and 80387 reset signals are always adjusted to the 16mHz clock so that the phase is properly matched to the internal CPU clock.

For test purposes, the 32mHz crystal oscillator can be stopped and replaced by an external source by pulling the signal TST32 high (there is a 180 ohm pulldown keeping it low) and driving the processor clocks directly with an external frequency source.

The 32mHz clock and the CLK16* signal are provided to the 32 bit memory board for use in state machines synchronized to the CPU.

The signal BCLK is an (approximately) divide by two from CLK16*. This division take piace in the bus state machine PAL D4-STAT where the clock is also re-synchronized to the CPU on each bus cycle. It is this adjusting that leads to the "approximate" part of the divide by two function. The average frequency will be somewhat less than 8mHz. Transitions of BCLK occur on rising edges of CLK16*.

The clock for the DMA subsystem is generated from the rising edge of the BCLK clock by toggling a 74LS74 flip-flop. The outputs (DCLK, DCLK*) will therefore have a frequency of one half that of BCLK.

24mHz 80287 CLOCK

The clock source for the 80287 is developed from a 24mHz crystal oscillator. The 24mHz frequency (CLK24) is divided down in a single 74HC109 to provide either 12mHz or 8mHz for use by the numeric coprocessor (80287). The 12mHz frequency is divided again inside an 80287-3 to provide a 4mHz operating frequency. The 8mHz has the required 33% duty cycle for direct use by an 80287-8 giving an operating frequency of 8mHz. The choice of frequencies is provided by switch SW1-3. Switch OFF selects 8mHz (80287-8), switch ON selects 4mHz (80287-3).

The only way of disabling the 24mHz clock for testing is to overdrive it's output.

14.31818mHz CLOCK

The specific time dependent clocks in the system are generated by a crystal oscillator at a frequency of 14.31818 MHz which generates the signal OSC.

The only way of disabling the OSC clock for testing is to overdrive it's output.

The OSC signal is provided to the system bus for compatibility with past products. The OSC signal is also divided by two by the PCLK flip-flop to provide a stable and unchanging frequency source (7.1591 MHz) to the keyboard processor (8042). The PCLK signal is in turn divided by six to provide a timing reference for the system timer (TIMCLK). This frequency is 1.19318 MHz and is compatible with the previous products for timing and speaker purposes.

The divide by six is done with a synchronous counter which cycles through the counts of 1 through 6 and back again. The counter is not specifically reset on powerup but will always cycle into the legal count sequence within seven clocks.

SYSTEM (EXPANSION) BUS

CPU ADDRESS HANDLING

The following information is applicable to nearly all the cycle types. When the CPU begins a bus cycle, it begins by placing an address and status on it's bus. This address will usually come out even while the previous cycle is still in progress. Since most devices expect to see a valid address for the duration of a bus cycle, it is necessary to latch the address seen by the system bus. System bus lines that contain the latched address are SA<19:0>. Since some devices (notably high speed memory) are already short on time to do their thing, they would like to overlap some of their operations (like address decode) with others. To allow this, the system bus also provides a set of address lines LA<23:17> which are not latched but which can provide a greater setup time to do decoding. The typical usage of these lines is to do the address decoding whenever the address changes, and then latch the decoded outputs.

To provide the unlatched addresses, the board contains buffer ICs which are connected to the CPU's PA<23:17> address lines and provide LA<23:17> as an output.

To provide the latched addresses, the board contains latch ICs which are connected to the CPU's PA<19:2> and provide SA<19:2> as an output. These latches are of the fallthrough type so that when the address latch enable signal (ALE) goes active the address appears at the output. When ALE goes inactive, the addresses will stay on the outputs until the next bus cycle begins.

The address lines SA0 and SA1 are handled a differently. The CPU indicates which bytes are to be accessed out of the 32 bit dword by the status lines BE3* to BE0* or Bus Enable three through zero. The system bus conversion state machine takes these status lines and the current bus state and sequences to the appropriate bus state. The output of this state machine are the address lines SA0, SA1 and BHE*.

The signal BHE* is used on the system bus to indicate that the high half of the 16 bit data bus contains valid data.

These signals (SA0, SA1 and BHE*) are changed at the rising edge of ALE so that their timing is very similar to the other SA<19:2> address lines.

All of the address outputs listed above are disabled when the CPU responds to a hold request (BHLDA) so that another device can control the address bus. When this occurs, the address lines are fed back to the CPU bus (PA<23:2> and BE<3:0>) so that the 32 bit memory board can recieve the address data from that other device. The feed back operation occurs from the SA<16:0> and the LA<23:17> lines through buffers and a PAL (D4-SADI) for SA0, SA1 and BHE*.

CPU address line PA20 is handled a little differently. Because of software compatiblity considerations (with 8088 products) it is sometimes necessary to restrict program access to the bottom megabyte of memory. This is done by disconnecting the PA20 line from the bus and forceing a low in it's place (by means of a 74F257). This is controlled by the line LOWA20 from the keyboard controller system. To equalize the delay with the other address lines, the output of the 74F257 is used to directly drive the LA20 line instead of being buffered again by a 74LS245.

CPU DATA HANDLING

The CPU data bus is buffered from the rest of the system by four bidirectional buffer ICs and four latches. On the CPU side of the bus, the 80386 and 80287 are connected together to PD<15:0>. The four ICs buffer the separate bytes of the data bus PD<31:0> to SD<15:0>. The latches are used to hold read data for the CPU during seperate read cycles on the system bus when the CPU attempts to read a bigger chunk than the system bus allows.

The data path also contains a bidirectional buffer between the high and low half of the bus to enable routing of the data from high half to low during high writes and routing of the data from low to high half during high reads of the eight bit bus. This function is controlled by the CPYEN* and CPYHL* lines. CPYEN* enables the buffer, CPYHL* controlls the direction according to the type of cycle (active for CPU writes or DMA reads).

The last item in the data path is a buffer for the processor board I/O devices. This buffer is normally active in the "TO" direction to the I/O devices and switches to the "FROM" direction when an I/O read occurs to these devices (controlled by CIORD*). This buffer is disabled when DMA operations occur to allow the bus to be used by the DMA controllers for address latching.

The folowing table shows the bus conversion from the CPUs BE<3:0> lines to the address lines and the data buffers that are enabled for each conversion.

Note that in the following table the "X8" term means that the system bus has indicated the cycle should be 8 bits. The "BEx*" lines are negative true bus enables from the CPU. The SA1 and SA0 lines are positive true and BHE* is negative true. The BENx* lines enable the data buffers to the bus and the latching function from the bus, they are negative true. The CPYEN* line enables the copy buffer from the SD<7:0> to SD<15:8>, the CPYHL* line is also enabled when reading (high to low copy). The LAST CYCLE term is used to indicate the last cycle in a group of cycles from one CPU status, it tells the state machine to send the CPU the READY* signal.

X8	BEx* 3210	SA 10	BHE	LAST CYCLE	BENx* 3210	CPYEN*	
X	1110	00	1	1	1110	1	LOW BYTE ON 8 OR 16 BUS
1	1101	01	0	1	1101	0	HIGH BYTE ON 8 BUS
0	1101	01	0	1	1101	1	HIGH BYTE ON 16 BUS
X	1011	10	1	1	1011	1	LOW BYTE ON 8 OR 16 BUS
1	0111	11	0	1	0111	0	HIGH BYTE ON 8 BUS
0	0111	11	0	1	0111	1	HIGH BYTE ON 16 BUS
0	1100	00	0	1	1100	1	WORD ON 16 BUS
							WORD ON 8 BUS:
1	1100	00	0	0	1100	1	LOW BYTE
1	1100	01	0	1	1101	0	HIGH BYTE
							2 SPLIT BYTES ON 16 BUS:
0	1001	01	0	0	1101	1	LOW WORD HIGH BYTE
0	1001	10	1	1	1011	1	HIGH WORD LOW BYTE
							2 SPLIT BYTES ON 8 BUS:
1	1001	01	0	0	1101	0	LOW WORD HIGH BYTE
1	1001	10	1	1	1011	1	HIGH WORD LOW BYTE
0	0011	10	0	1	0011	1	WORD ON 16 BUS
							WORD ON 8 BUS:
1	0011	10	0	0	0011	1	LOW BYTE
1	0011	11	0	1	0111	0	HIGH BYTE
							3 BYTE ON 16 BUS:
0	1000	00	0	0	1100	1	LOW WORD
0	1000	10	1	1	1011	1	HIGH WORD LOW BYTE
							3 BYTE ON 8 BUS:
1	1000	00	0	0	1100	1	LOW WORD LOW BYTE
1	1000	01	0	0	1101	0	LOW WORD HIGH BYTE
1	1000	10	1	1	1011	1	HIGH WORD LOW BYTE
							3 BYTE ON 16 BUS:
0	0001	01	0	0	1101	1	LOW WORD HIGH BYTE
0	0001	10	0	1	0011	1	HIGH WORD
							3 BYTE ON 8 BUS:
1	0001	01	0	0	1101	0	LOW WORD HIGH BYTE
1	0001	10	0	0	0011	1	HIGH WORD LOW BYTE
1	0001	11	0	1	0111	0	HIGH WORD HIGH BYTE
							4 BYTE ON 16 BUS:
0	0000	00	0	0	1100	1	LOW WORD
0	0000	10	0	1	0011	1	HIGH WORD
							4 BYTE ON 8 BUS:
1	0000	00	0	0	1100	1	LOW WORD LOW BYTE
1	0000	01	0	0	1101	0	LOW WORD HIGH BYTE
1	0000	10	0	0	0011	1	HIGH WORD LOW BYTE
1	0000	11	0	1	0111	0	HIGH WORD HIGH BYTE

PROCESSOR BOARD CPU COMMAND/CYCLE TYPES

The command cycles generated by the bus control logic are listed below. The number of 62.5nsec clocks is listed for a no-wait state cycle, normal cycle, and 1 wait state cycle for each of the command types. Both the total cycle time and the command active (on) time are given. For cycles with more than one bus wait state, each wait state adds two additional 62.5nsec clock cycles. The 32 bit memory board is documented seperately.

		No-wait cycle:on	Normal cycle:on	1-wait cycle:on
CPU MEM READ	16 BUS	4:2	6:4	8:6
CPU MEM READ	8 BUS	6:3	12:9	14:11
CPU MEM WRITE	16 BUS	4:2	6:4	8:6
CPU MEM WRITE	8 BUS	6:3	12:9	14:11
CPU I/O READ	16 BUS	6:3	6:3	8:5
CPU I/O READ	8 BUS	6:3	12:9	14:11
CPU I/O WRITE	16 BUS	6:3	6:3	8:5
CPU I/O WRITE	8 BUS	6:3	12:9	14:11
CPU INTA READ		n/a	12:9	n/a
CPU HALT		n/a	6:4	n/a
CPU SHUTDOWN		n/a	6:4	n/a

If the CPU status indicates more than one bus cycle will be required for a single CPU access, then the bus state machine will run the necessary number of bus cycles (duration indicated above) to complete the CPU access. For example, if the CPU status indicates a double-word memory read from the 8 bit bus, then the total cycles for the access would be 4*12=48, 62.5 nsec cycles (assuming normal cycles).

CPU ACCESS TO SYSTEM (8/16) BUS

For the following discussion, it should be noted that the CPU is normally held in the NOT READY state, READY* only goes active (low) when a cycle is guaranteed to be finished. Also, the CPU next address (NA*) line is normally inactive, requireing the logic to specifically tell the CPU when it is ok to send the next address.

The cycle begins when the 80386 activates ADS* and presents the status lines. The address is decoded by the 32 bit memory board (if present) and the signal M32* is produced. The system board decodes the status lines from the processor and the M32* line to produce the signal MYCYC*. This signal is produced whenever the decoded cycle indicates that the system board should handle it. The signal is NOT active when accesses to 32 bit memory or the 80387 coprocessor are taking place. The signal is active when 16 or 8 bit memory, I/O, Halt, Shutdown, Interrupt acknowledges, or 80287 accesses are taking place.

MYCYC* is then sampled by the D4-STAT PAL on the rising edge of CLK16* (the bus clock). Until further notice all clocks referred to are CLK16* clocks. When the PAL clocks in MYCYC* it generates the signal ALE*. The PAL code is set up to allow ALE* to be active only for a single cycle. What follows next is the propagation of the ALE* pulse through a series of flip-flops arranged in a configurable shift register. The general method is to bypass parts of the shift register to shorten the total bus cycle time depending on the type of bus cycle to be executed.

The rising edge of ALE latches the address and status for later use and does the SA1, SA0, BHE* generation. The signal BCLK will be forced to a low during ALE by the D4-STAT PAL to insure the compatibility with previous products.

The next stage is T00. It is always generated. If the command being generated is a 16 bit memory command, as signified by LM-IO and M16*, then the signal CMD* will also be set active at this time. CMD* is combined with the decoded status to generate the signal MRDC* or MWTC*. If this is the last cycle in a set, (either guaranteed by the state or because the bus size is known by M16* and a memory cycle) then the D4-SADO PAL will set the signal CLSTD* active at this time. CLSTD* will be discussed later.

The next stage is T01. It is always generated. If the command being generated is not a 16 bit memory command, as signified by LM-IO and M16*, then the signal CMD* will also be set active at this time. CMD* is combined with the decoded status to generate the signal IORC*, IOWC*, or INTA*. If this is the last cycle in a set, (because the bus size is known by IO16* and an I/O cycle) then the D4-SADO PAL will set the signal CLSTD* active at this time. If this is a 16 bit memory cycle, and the NOWS* signal was received during T00 (LNOWS* active), then the signal BRDY* will be generated next to terminate the cycle and no other stages will be activated.

The next stage is T10. It is always generated. If the cycle is a 16 bit memory cycle, then the T40 stage will also be activated at this time. In this case, the T10 and T11 states will be ignored for the remainder of the 16 bit memory cycle.

The next stage is T11. It will always be generated. If the cycle is a 16 bit I/O cycle, then T41 will also occur at the same time as T11. If this is an 8 bit cycle, and the NOWS* signal was received earlier (LNOWS* active), then the signal BRDY* will be generated next to terminate the cycle and no other stages will be activated. Otherwise, stages T20, T21, T30 and T31 will follow if the cycle is an eight bit bus cycle as signalled by CX16* inactive.

The next stage is T40. This stage is entered either from T31 during an eight bit cycle, or T01 if a 16 bit memory cycle or a cycle that does not depend on the CX16* status occurs. This stage is skipped if the LNOWS* line is found active.

The next stage is T41. This is entered only from T40 (the normal case) or T10 (if a 16 bit I/O cycle is in progress). If the signal WAIT* is active at the end of T41, then T41 will be restarted, holding the bus in a wait state. Since the WAIT* signal is developed by sampling the BUSRDY* going high only every BCLK rising edge, wait states will come in increments of two clock cycles. When WAIT* goes inactive, the signal BRDY* will be generated to terminate the cycle.

At the same time as the cycle is being terminated (BRDY* is set active) then several things can happen. If this is not the last cycle in the set (CLAST* inactive), then TS0* is set active by the D4-STAT PAL to start another cycle. If this is the last cycle in the set (CLAST* active) and another cycle is pending (MYCYC* is active), then TS0* is set active by the D4-STAT PAL to start another cycle. If no more cycles are to be run for the moment, then the bus state machine will remain idle waiting for another cycle.

TS0* is used to provide an adequate address setup between cycles in a group or between groups when the CPU pipelines the next cycle. After TS0* the ALE state will be entered for the next cycle.

The signal CMD* (which is used to enable one of MRDC*, MWTC*, IORC*, IOWC*, or INTA*) is started at the beginning of T00 or T01 as discussed above. It will end at the end of the basic bus cycle (when BRDY* or TS0 goes active).

The signal WDEN* is used for enableing the various data buffers during write cycles. It goes active at the same time as ALE and goes inactive one cycle after CMD* goes inactive. In the case of back to back cycles, WDEN* will therefor remain active until after the last CMD*.

The signal BRDY* from the D4-STAT PAL signals the end of a set of bus cycles to the CPU.

The signal CLSTD* (which goes active for one CLK16* cycle to indicate that the last cycle of a set is in progress) also generates the CLAST* signal internal to the D4-SADO PAL. CLAST* is used by the D4-SADO PAL to do the conversion from BE<3:0> to SA1, SA0, and BHE*. CLAST* is also used to tell the state machine that no more cycle are in the set. At the rising edge of ALE, CLAST* is set to the inactive state in preparation for the next CPU access.

The signal CLSTD* is also used to generate NAB* (next address from bus) which signals the CPU that it is all right to put a new address and status onto the CPU bus. Since NAB* is sampled at the beginning of phase 2 of a CPU clock cycle, it is synchronized to the rising edge of CLK32 at the rising edge of CLK16* by the D4-SMSCD PAL. This assures a setup time to the CPU for NA*.

The signal CX16* is used to signal the presence of a 16 bit memory or I/O cycle. It is set active during T00 for memory cycles if M16* is active. It is also set active during T10 for I/O cycles if IO16* is active. It is set inactive at ALE in preperation for the next cycle. This signal is used to control the bus address conversion for the 8 or 16 bit bus and to adjust the timing of the expansion bus for 16 bit operations.

The signal LOE* (Latch Output Enable) is generated during read cycles from the 8/16 bus to enable the data stored in the data latches to the CPU data bus. LOE* is first set active on the CLK16* edge following ALE in the D4-SMSCD PAL and is set inactive on the CLK16* edge following the signal BRDY* active. When LOE* goes inactive, it has 31.25nsec from the edge of CLK32 to disable the latch output buffers before the CPU may begin driving the bus again. The total delay to disable the latches is calculated below.

Data Latches off the CPU data bus

CLK32 cycle time		31.2
ZPC32 to PCLK32 delay		2.0
CLK32 to ZCK16* in F74		- 7.8
ZCK16* to LOE* in PAL		-10.0
LOE* to disable in ALS573		-13.0
MARGIN	**********	+ 2.4

The following are some timing checks of the critical setup times to the CPU.

NA* setup during bus cycles

CLK32 cycle time		31.2
ZPC32 to PCLK32 delay		2.0
CLK32 to ZCKP16* in F74		- 7.8
ZCK16* to NAB* in PAL		-10.0
NAB* to NA* in F08		- 6.6
386 NA* setup time		-10.0
MARGIN	**********	- 1.2

READY* setup during bus cycles

CLK16* cycle time		62.5
ZPC32 to PCLK32 delay		2.0
CLK32 to CLK16* in F74		- 9.5
CLK16* to BRDY* in PAL		-15.0
BRDY* to READY* in F08		- 5.6
386 READY* setup time		-20.0
MARGIN	**********	+14.4

STATE SEQUENCES FOR TYPICAL CYCLES.

The "cmd" is the time that the command (MRDC, IOWC, etc) is valid. The "NA" is the time when CLASTD* is set active. The "done" is when BRDY* is set active. TSx is either the next TS0 state (if another cycle is pending, or an idle cycle (as far as the bus state machine is concerned). Each state lasts 62.5 nsec.

```
NO WAIT STATE 16 BIT MEMORY
TS0 ALE T00 T01 TSx
        cmd cmd
        NA      done
NORMAL WAIT STATE 16 BIT MEMORY
TS0 ALE T00 T01 T40 T41 TSx
        cmd cmd cmd cmd
        NA              done
NORMAL WAIT STATE 16 BIT I/O or NO WAIT STATE 16 BIT I/O
TS0 ALE T00 T01 T40 T41 TSx
            cmd cmd cmd
            NA          done
EXTRA WAIT STATE 16 BIT MEMORY
TS0 ALE T00 T01 T40 T41 T41 T41 TSx
        cmd cmd cmd cmd cmd cmd
        NA                  done
EXTRA WAIT STATE 16 BIT I/O
TS0 ALE T00 T01 T40 T41 T41 T41 TSx
            cmd cmd cmd cmd cmd
            NA                  done
NO WAIT STATE 8 BIT MEMORY or I/O
TS0 ALE T00 T01 T40 T41 TSx
            cmd cmd cmd
            NA      done
NORMAL WAIT STATE 8 BIT MEMORY or I/O
TS0 ALE T00 T01 T10 T11 T20 T21 T30 T31 T40 T41 TSx
            cmd cmd cmd cmd cmd cmd cmd cmd cmd
            NA                              done
EXTRA WAIT STATE 8 BIT MEMORY or I/O
TS0 ALE T00 T01 T10 T11 T20 T21 T30 T31 T40 T41 T41 T41 TSx
            cmd cmd cmd cmd cmd cmd cmd cmd cmd cmd cmd
            NA                                      done
```

BUSRDY, NOWS*, M16* and IO16* requirements.

(BUSRDY) This signal is used to add additional wait states to a bus cycle. If a 16 bit device wants to add an additional wait state, then it must pull the BUSRDY low (inactive) by the end of the third CLK16 cycle after the falling edge of ALE. To add only one wait state, BUSRDY must return to the high state during the fourth CLK16 cycle after the falling edge of ALE. If an 8 bit device wants to add an additional wait state, then it must pull the BUSRDY low (inactive) by the end of the ninth CLK16 cycle after the falling edge of ALE. To add only one wait state, BUSRDY must return to the high state during the tenth CLK16 cycle after the falling edge of ALE. The decode logic to drive BUSRDY should use the device address and MRDC*, MWTC*, IORC* or IOWC* as inputs. Synchronous peripherals usually use the falling edge of BCLK as the time to change the state of BUSRDY.

(NOWS*) This signal is used to shorten the standard bus cycles. If a 16 bit memory device wants to prevent the standard wait state then it must pull the NOWS* line low (active) within one CLK16 time from the falling edge of ALE. (Note that this is not possible on 16 bit I/O cycles because it is not known that an I/O cycle exists until the required time). If an 8 bit device wants to prevent the standard wait states then it must pull the NOWS* line low (active) within two CLK16 times from the falling edge of the command. The decode logic to drive NOWS* should use the device address and MRDC*, MWTC*, IORC* or IOWC* as inputs. If less than the four standard wait states normally used on 8 bit bus cycles is desired, then the NOWS* line can be used to provide 1, 2, or 3 wait states by delaying the activation of NOWS*. The NOWS* line is sampled at approximately the falling edge of BCLK.

(M16*) This signal is used to indicate that the current address on the LA<23:17> lines is covered by a 16 bit memory peripheral. The system board will only use this signal if the current cycle is a memory cycle. The addressed peripheral on the bus must pull the M16* line low as soon as the address is decoded and hold it low until the address becomes invalid. The M16* line must be correct before BALE goes inactive to insure that it is latched by the system board latch. Pulling this line low prevents the 16 bit to 8 bit bus conversion logic from being activated.

(IO16*) This signal is used to indicate that the current address on the SA<9:0> lines is covered by a 16 bit I/O peripheral. The system board will only use this signal if the current cycle is an I/O cycle. The addressed peripheral on the bus must pull the IO16* line low as soon as the address is decoded and hold it low until the address becomes invalid. The IO16* line must be correct by the second CLK16 cycle after ALE goes away to insure that it is latched by the system board latch. Pulling this line low prevents the 16 bit to 8 bit bus conversion logic from being activated.

COMPATIBLE BUS MEMORY COMMANDS

The signals SMRDC* and SMWTC* are used by the eight bit bus only. These memory signals are only enabled when the lower one megabyte of memory is addressed. They are developed from the regular MRDC*, and MWTC* signals by enabling a set of tri-state buffers with the signal LOWEN*. This signal is developed by the D4-SROM PAL from the address information on the system bus. The PAL also includes the latching function required to hold the address through the entire cycle and the refresh function for any dynamic memory on the original eight bit bus.

NON PROCESSOR SUBSYSTEMS

The processor board also contains logic to generate or handle other types of bus cycles. Following is a list of those cycles.

PROCESSOR BOARD DMA CYCLE TYPES

DMA MEM READ BYTE	16	RAM	LOW BYTE
DMA MEM READ BYTE	16	RAM	HIGH BYTE
DMA MEM READ BYTE	8	BUS	LOW BYTE
DMA MEM READ BYTE	8	BUS	HIGH BYTE
DMA MEM WRITE BYTE	16	RAM	LOW BYTE
DMA MEM WRITE BYTE	16	RAM	HIGH BYTE
DMA MEM WRITE BYTE	8	BUS	LOW BYTE
DMA MEM WRITE BYTE	8	BUS	HIGH BYTE
DMA MEM READ WORD	16	RAM	
DMA MEM WRITE WORD	16	RAM	
REFRESH READ			

SYSTEM BUS MASTER CYCLE TYPES

BUS MASTER MEM READ BYTE	16	RAM	LOW BYTE
BUS MASTER MEM READ BYTE	16	RAM	HIGH BYTE
BUS MASTER MEM READ BYTE	8	BUS	LOW BYTE
BUS MASTER MEM READ BYTE	8	BUS	HIGH BYTE
BUS MASTER MEM WRITE BYTE	16	RAM	LOW BYTE
BUS MASTER MEM WRITE BYTE	16	RAM	HIGH BYTE
BUS MASTER MEM WRITE BYTE	8	BUS	LOW BYTE
BUS MASTER MEM WRITE BYTE	8	BUS	HIGH BYTE
BUS MASTER MEM READ WORD	16	RAM	
BUS MASTER MEM WRITE WORD	16	RAM	
BUS MASTER I/O READ BYTE	16	BUS	LOW BYTE
BUS MASTER I/O READ BYTE	16	BUS	HIGH BYTE
BUS MASTER I/O READ BYTE	8	BUS	LOW BYTE
BUS MASTER I/O READ BYTE	8	BUS	HIGH BYTE
BUS MASTER I/O WRITE BYTE	16	BUS	LOW BYTE
BUS MASTER I/O WRITE BYTE	16	BUS	HIGH BYTE
BUS MASTER I/O WRITE BYTE	8	BUS	LOW BYTE
BUS MASTER I/O WRITE BYTE	8	BUS	HIGH BYTE
BUS MASTER I/O READ WORD	16	BUS	
BUS MASTER I/O WRITE WORD	16	BUS	

HOLD REQUEST ARBITRATION

The RFK (refresh request) signal is synchronized to DCLK* by the RFQ flip-flop. Another flip-flop synchronizes the DREQ (DMA request) signal from the DMA subsystem to the DCLK clock. This insures that the two requests cannot arrive simultaneously. Both requests are next clocked by a pair of flip-flops (DMARQ, REFRQ) that have their Q* outputs cross connected to the other's clear inputs. This guarantees that only one of the two signals (DMARQ, REFRQ) can be active at a time.

The two request signals are also ORed together and run through a circuit which locks out the combined request when a hold acknowledge cycle is in progress but the original request has gone away. This prevents a new hold request from being initiated before the last one is completed. The output of the speed control circuit is also ORed in with the other requests in order to use up cpu bus bandwidth as a means of slowing the system down.

This output (HRQ) is fed to an F74 flip-flop to which acts as another arbitration circuit. This circuit prevents the initiation of processor reset from occurring during HRQ or HRQ from occurring during processor reset. This prevents the CPU from aborting a hold request and subsequent garbaged hold cycles.

After the reset arbitration, the output (GHRQ*) is gated with the signal RESCP. This prevents a hold from being started during the duration of the reset signal to the CPU.

The output signal from the reset lockout circuit (HRQCP) is synchronized to the CPU clock by a 74F175 (HOLD) to assure a proper setup time to the CPU.

CPU HOLD REQUEST SETUP TIME

CLK16* cycle time		62.5
CLK32 to CLK16* in F74		- 9.5
CLK16* to HOLD in F175		- 9.5
386 HOLD setup time		-25.0
MARGIN	**********	+18.5

When the HLDA signal is received from the CPU indicating that the bus is available, then the signal REFRS* (gated from REFRQ) or HAK (gated from DMARQ) is set active, enabling the appropriate subsystem. If the speed control circuit is the source of the request, then neither of the above is set active.

It should be noted that if a cycle is in progress from one requestor, and the other requestor makes a request, then on the first rising edge of BCLK after the first xxxREQ signal goes away, the second requestor will be acknowledged. This will occur without giving the bus back to the CPU, i.e. a DMA hold and a refresh hold will be run back to back. If the speed control circuit is holding the bus then holds from DMA or refresh will be immediately acknowledged.

CPU OFF THE BUS

When the HLDA signal is received from the CPU, the address latches between PA<19:2> and SA<19:2> are tri-stated. The PAL which converts BE<3:0> to SA1, SA0, and BHE* (D4-SADO) is also tri-stated. The CPU bus command generator PAL (D4-SCMD) command output signals are also tri-stated. The command signals are held inactive by pullup resistors until the DMA controller, refresh controller, or other bus master can take over the bus. The bus address latch enable signal (BALE) is forced to the active state requiring that any other bus master must hold an address stable for the duration of a bus cycle.

To allow the 32 bit memory board to receive addresses generated by the other subsystems, a series of buffers back feeds the CPU address bus (PA<23:2>) from the system busses (LA<23:17> and SA<16:2>. Another PAL (D4-SADI) converts SA1, SA0, and BHE* to the BE<3:0> lines from the CPU and the D4-SCMD PAL converts the MRDC*, MWTC*, and REFRS* lines to an encoded status on the M-IO, D-C, and W-R lines for use by the memory board. The encoding is described in detail in the 32 bit bus descriptions.

The data buffers between the CPU (PD<31:0>) and system bus (SD<15:0>) are turned around to work in the opposite direction from normal so that the other bus master can access the 32 bit memory as if it was regular 16 bit memory.

DMA OPERATIONS

The DMA controllers in the system operate as a separate subsystem from the main bus controller. They handle requests from the DMA peripherals, arbitrate between them, and then request access to the system address and command busses from the CPU by asserting DREQ. The system consists of two controller ICs (8237A-5), a page register for handling the high order bits of DMA address (74LS612), and various latches and logic for address routing and control.

There are two types of DMA on this design, byte and word DMA. One of the controllers is connected to handle byte operations, the other, word operations. In order to simplify the arbitration between sources, the hold request line from the byte controller is connected to a DMA request line (DRQ4) on the word controller. The word controller is programmed for cascade mode on channel 0 (to which is connected DRQ4) so that it will not actually place an address on the bus when it acknowledges the byte controllers request.

BYTE DMA OPERATIONS

The DMA byte cycle begins when a peripheral sets a DRQ0-DRQ3 line active. The 8237 then arbitrates among any other pending requests and sets the hold request output active. This line (DRQ4) is connected to the word controller as discussed above which does it's arbitration. The word controller then sets it's hold request line active (DREQ) which is then synchronized and arbitrated by the Hold arbitration logic discussed above.

When the system responds to the DREQ with a HAK, one DCLK later the HAKDMA will be generated. This provides for setup time to the 8237 from the last CPU access. When HAKDMA goes active, the word 8237 will respond with a DAK4 which acts as a hold acknowledge to the byte controller. The byte controller will, after synchronizing the acknowledge, assert DAEN1* (through a gate) and place an address on the XA<0:7> lines. It will place the high byte of the address on the IOD<0:7> lines and assert the address strobe signal to latch the address into the associated latch. The DAEN1* signal also enables the output of the latch to the SA<8:15> lines.

The D4-SCPY PAL drives the SBHE* line in the opposite sense of SA0 in order to satisfy 16 bit devices on the bus.

The DAEN1* signal is ORed with the DAEN2* signal inside the D4-SCPY PAL to produce DAEN* which changes the direction of the bidirectional buffers between the XA<0:8> and the SA<0:8> busses so that the DMA address will be on the system bus.

The SA16 line has an additional tri-state buffer between the LS612 output and SA16. This buffer is enabled for byte type DMA (as discussed here) and disabled for word type DMA (because the word 8237 drives SAi6 in word DMA).

The lines LA<23:17> are driven by the 74LS612 page register when the CPU sets HLDA active (through the DMA* line). The selection of which internal register to enable to the bus is done by three gates which encode the DAKx signals into a register address for the LS612. The lines A<19:17> are also copied to SA<19:17> by a buffer enabled by the DMA* line.

In the above fashion, all of the address lines on the bus are driven with appropriate address. When this is complete, the 8237 drives the lines XIORC*, XIOWC*, XMWTC*, and DMRDC* according to the type of cycle being run. The first three of these lines are buffered back to the IORC*, IOWC*, MWTC* lines by a bidirectional buffer controlled by DAEN*. The DMRDC* line is handled differently. It is delayed by one DCLK cycle before being gated onto the XMRDC* line and then to the MRDC* line. When DMRDC* goes inactive, XMRDC* goes inactive without the DCLK delay. This action provides a greater memory address setup on read commands for block transfer modes of the 8237.

A single DCLK length wait state is added to all DMA cycles. To do this, the OR of DMRDC* and XIORC* clocks the DWQ flip-flop to inactive, setting DRDY inactive. On the next rising edge of DCLK the DXQ flip-flop is clocked active which in turn sets the DWQ flip-flop active again. On the next DCLK, DXQ will go inactive, allowing DRDY to go active and signal ready to the 8237. If a peripheral wants additional wait states, it can pull the BUSRDY line low which will set the DWQ output to a low and prevent DXQ from going inactive. The wait circuit is prevented from being affected by BUSRDY except during DMA cycles by a gate which holds the DWQ flip-flop set active.

The D4-SCPY PAL enables the COPYEN* line if SA0 is high and the addressed memory is 16 bit in order to route the data between the low half and high half of the data bus. The COPYHL line moves the data from high to low on memory reads, and from low to high on memory writes.

WORD DMA OPERATIONS

Word DMA operations are only possible between word memory (16 or 32 bit) and word peripherals. Also, the DMA cannot do anything to an odd address boundary, on either memory or I/O.

The DMA word cycle begins when a peripheral sets a DRQ5-DRQ7 line active. The 8237 then arbitrates among any other pending requests and sets the hold request output active. The hold request line (DREQ) is then synchronized and arbitrated by the Hold arbitration logic discussed above.

When the system responds to the DREQ with a HAKDMA, the word 8237 will, after synchronizing the acknowledge, respond with a DAKx acknowledge to the peripheral. It will also assert AEN2 and DAEN2* (through a gate and D4-SCPY PAL) and place an address on the XA<8:1> lines. It will place the high byte of the address on the IOD<7:0> lines and assert the address strobe signal to latch the address into the associated latch. The DAEN2* signal also enables the output of the latch to the SA<16:9> lines.

The D4-SCPY PAL drives the SA0 and SBHE* line to a low in order to satisfy 16 bit devices on the bus.

The remainder of the word DMA operation is the same as the byte operation except for the handling of the COPYEN* and COPYHL* signals. These signals are not enabled at all for word based DMA.

DYNAMIC RAM REFRESH AND HOLD ARBITRATION

The dynamic RAM refresh subsystem is designed to do a memory read cycle on each of 256 addresses in the memory space as addressed by SA7 to SA0. Address lines SA8 is made equal to SA0 and SA9 is made equal to SA1 in order to simplify 32 bit memory board design. To allow for future DRAMs requireing additional refresh addresses, SA10 and SA11 have two additional counter bits present for a total of 1024 possible refresh addresses. The other address lines are in an undefined state during the RAM refresh time. The system is also capable of being driven by an external source if another bus master has control. The system consists of a timer (part of the 8254) which generates the refresh requests every 15.924usec, arbitration logic which arbitrates whether the refresh controller or the DMA subsystem gets hold of the bus, a timing generator, and a refresh address counter. The refresh request rate of 62.799 kHz provides 128 refresh cycles in 2.038 millisec or 256 cycles in 4.0765 milliseconds etc.

The refresh cycle starts when the REFCK out of the 8254 goes to a high. The clocks the RFK flip-flop to a high. The RFK flip-flop will remain high until the refresh request has been satisfied. This line goes to the hold request arbitration circuit discussed above. Nothing else will happen until the arbitration circuit responds with the acknowledge signal REFRS*. (Note: to allow bus masters control of refresh, the REFRS* driver is an open collector gate with a pullup resistor).

When REFRS* goes active, it will be clocked into (through a gate), the REFEN* flip-flop by the BCLK signal, enabling the refresh address from the counter onto the bus. The REFEN* signal is in turn clocked into REFRD* flip-flop by the next rising edge of BCLK, enabling the MRDC* command onto the bus. The REFRD* signal is gated with BUSRDY and clocked into the next flip-flop (REFEND) by BCLK. This allows a slow memory board to insert wait states into refresh cycles. The output of this flip-flop (REFEND) is gated with the REFRS* signal mentioned at the beginning of this paragraph to end the refresh cycle on the next BCLK. At the same time that the REFEND signal is clocked through, the REFCL* flip-flop is clocked to a low, clearing the RFK and RFQ flip-flops and ending the refresh cycle.

If an external bus master wishes to take the bus for long periods of time, it must perform refresh or risk losing the dynamic memory. The external bus master can do this by developing it's own refresh request timer and internal arbitration. When it is not otherwise driving the bus, but still has bus control, it can do a refresh cycle by pulling the REFRS* line low with an open collector gate. When the MRDC* line goes inactive from the refresh cycle, the REFRS* line should be released. The external bus master can then take full control.

OTHER BUS MASTER OPERATIONS

This system allows other bus masters to take over the system busses and use the I/O peripherals and memory. This is accomplished by the bus master software programming an unused DMA channel for cascade operation. When this is complete, the bus master can request the bus by setting the appropriate DRQ line active and waiting for a response. When the system responds with DAK, the bus master can pull the GRAB* line active (low) disabling the address, data, and control lines. The bus master should then wait one BCLK period before enabling it's own buffers with valid address information and wait one more BCLK period before driving the control lines. When the bus master is finished, it should release the GRAB* and DRQ lines to allow the CPU to continue operations. If the bus master keeps hold of the bus for more than 15 usec, then it should contain it's own refresh timing and request logic to prevent loss of dynamic memory.

SPEED CONTROL

This system is implemented to give the user some control of the system speeds in the case that software is speed dependent. The system consists of a one channel of the second 8254 timer counter and an interconnect the the hold request circuit. The timer channel is programmed as a one-shot which is triggered by refresh requests. If the 8042 keyboard controller SLOWD* line is active (LOW) then the timer output will extend the CPU hold time for refresh by the programmed value of the one-shot. During this hold time, the CPU cannot use the bus for execution, but the DMA subsystem can continue to work. The timer is clocked by DCLK giving a 250nsec increment in bus hold time. To disable the circuit, the 8042 SLOWD* output can be set inactive (HIGH) or the 8254 timer can be stopped by programming the channel but not giving it a count value (out 4Bh, 92h). To enable the one-shot, program for MODE 1 (out 4Bh, 92h) and give a count value between 01h and 38h (out 4Ah, xxh).

PROCESSOR SHUTDOWN AND RESET

The CPU reset and shutdown circuits are designed to properly reset the processor during: powerup, temporary power loss, CPU shutdown, and under program control for mode switching.

Since the CPU requires a reset pulse width minimum of 15 CLK32 times (469nsec) to respond properly, the circuit described next pulses the CPU reset line for 4 BCLK cycles (500nsec) for the cases of shutdown and program reset.

The shutdown reset function is used to get the processor out of the situation where a processor exception occurs while doing a processor exception. In this case, the CPU goes into shutdown mode as signaled by the status M-IO * /D-C * W-R * BE0 * ALE (signal SHTD*). The shutdown flip-flop (SHQ) is clocked active by SHTD*.

This output (SHQ) is fed to an F74 flip-flop to which acts as another arbitration circuit. This circuit prevents processor reset from occurring during hold cycles or hold from occurring during processor reset. This prevents the CPU from aborting a hold request and subsequent garbaged hold cycles.

The SHQ* signal (out of the reset arbitration) is clocked into another flip-flop by the RCLK signal (which has a rising edge every 4 BCLK times) producing RESCP*. This is in turn synchronized to CLK16 by another F74 to form the RESCPU signal which resets the CPU. RESCP* clears the SHQ flip-flop and ends the reset pulse. Making RESCPU synchronous with CLK16 insures that CLK16 is in turn synchronous with the internal 80386 CLK signal.

Restarting the processor under program control is done by pulsing a bit in the 8042 keyboard processor (RSTAR*). This line sets the SHQ flip-flop active and starts the reset sequence in the same manner as described for shutdown.

The last two functions, powerup reset and power loss reset, are provided by the PWGOOD signal from the power supply. This signal is clocked by CLK16* to form the signals RST* and RESDRV. RST* is used by most circuits on the system board for powerup setup, RESDRV is sent to the system bus for resetting most other circuits in the system. The CPU gets reset through the shutdown circuit. When RST* is active, the RESCP* flip-flop is set active which in turn resets the CPU through the F74 and RESCPU.

The signal RESCP (inverse of RESCP*) is used to hold the signal CMSAWR in the high state during the rising edge of CMSCE* (which goes high with PWGOOD) in order to properly set up the CMOS clock IC.

I/O SUBSYSTEMS

The I/O subsystems consist of the 8259A interrupt controllers, the 8254 timer/counters and their associated circuits, the CMOS clock/RAM IC (MC146818), the 8042 keyboard interface, and the peripheral interface circuits. Also located within the I/O space on the processor board, are the DMA controllers and the DMA Page registers which are used to determine the top eight address bits during DMA operations.

The address decoding is done with three ICs, a 74LS138 which decodes the bits SA<9:5>, (D4-SNCP) PAL which breaks out the two timers, and a (D4-SPPI) PAL which decodes other addresses. Below are the PAL equations for the decode PALs:

```
NMICS  = PPICS* SA4* /SA3* /SA0* XIOWC   ;NMI enable latch write (70h)

CMSAWR = CMSAWR* XIOWC                   ;CMOS address write (70h)
       + RESCMS                          ;or during powerup

CMSRD  = PPICS* SA4* /SA3* SA0* XIORC    ;CMOS data read (71h)

CMSWR  = PPICS* SA4* /SA3* SA0* XIOWC    ;CMOS data write (71h)

KEYCS  = PPICS* /SA4* /SA3* /SA0         ;8042 (60h, 64h)

PBWR   = PPICS* /SA4* /SA3* SA0* XIOWC   ;Port B write (61h)

PBRD   = PPICS* /SA4* /SA3* SA0* XIORC   ;Port B read (61h)

CIORD  = /SA9* /SA8* XIORC               ;0-FFH except 80287
       + INTA                            ;or Interrupt ack

TIM1CS = TIMCS* /SA3                     ;Standard timer

TIM2CS = TIMCS* SA3                      ;Special 386 timer
```

Following is an address and bit map of the devices in the I/O subsystem.

ADDRESS	ADDRESS BITS										DEVICE
HEX	9	8	7	6	5	4	3	2	1	0	
00h-0Fh	0	0	0	0	0	x	Y	Y	Y	Y	8237A-5 byte DMA controller
20h-21h	0	0	0	0	1	x	x	x	x	Y	8259A Interrupt 2 controller
40h	0	0	0	1	0	x	0	x	0	0	8254-1 System clock Timer 0
41h	0	0	0	1	0	x	0	x	0	1	8254-1 Refresh request Timer 1
42h	0	0	0	1	0	x	0	x	1	0	8254-1 Speaker Timer 2
43h	0	0	0	1	0	x	0	x	1	1	8254-1 Command Mode register
48h	0	0	0	1	0	x	1	x	0	0	8254-2 Failsafe clock Timer 0
49h	0	0	0	1	0	x	1	x	0	1	8254-2 Extra Timer 1
4Ah	0	0	0	1	0	x	1	x	1	0	8254-2 Speed control Timer 2
4Bh	0	0	0	1	0	x	1	x	1	1	8254-2 Command Mode register
60h	0	0	0	1	1	0	0	0	x	0	8042 data I/O register
61h	0	0	0	1	1	0	0	x	x	1	Port B/C In/Outputs
64h	0	0	0	1	1	0	0	1	x	0	8042 status/command register
70h	0	0	0	1	1	1	0	x	x	0	CMOS address register
70h	0	0	0	1	1	1	0	x	x	0	NMI enable register (bit 8 low)
71h	0	0	0	1	1	1	0	x	x	1	CMOS data I/O register
80h	0	0	1	0	0	x	0	0	0	0	DMA Page register SPARE
81h	0	0	1	0	0	x	0	0	0	1	DMA Page register CH 2 page
82h	0	0	1	0	0	x	0	0	1	0	DMA Page register CH 3 page
83h	0	0	1	0	0	x	0	0	1	1	DMA Page register CH 1 page
84h	0	0	1	0	0	x	0	1	0	0	DMA Page register SPARE
85h	0	0	1	0	0	x	0	1	0	1	DMA Page register SPARE
86h	0	0	1	0	0	x	0	1	1	0	DMA Page register SPARE
87h	0	0	1	0	0	x	0	1	1	1	DMA Page register CH 0 page
88h	0	0	1	0	0	x	1	0	0	0	DMA Page register SPARE
89h	0	0	1	0	0	x	1	0	0	1	DMA Page register CH 6 page
8Ah	0	0	1	0	0	x	1	0	1	0	DMA Page register CH 7 page
8Bh	0	0	1	0	0	x	1	0	1	1	DMA Page register CH 5 page
8Ch	0	0	1	0	0	x	1	1	0	0	DMA Page register SPARE
8Dh	0	0	1	0	0	x	1	1	0	1	DMA Page register SPARE
8Eh	0	0	1	0	0	x	1	1	1	0	DMA Page register SPARE
8Fh	0	0	1	0	0	x	1	1	1	1	DMA Page register REFRESH page
A0h-A1h	0	0	1	0	1	x	x	x	x	Y	8259a Interrupt 2 controller
C0h-CFh	0	0	1	1	0	Y	Y	Y	Y	x	8237a-5 word DMA controller
F0h	0	0	1	1	1	x	0	x	x	0	Clear numeric processor busy
F1h	0	0	1	1	1	x	0	x	x	1	Reset numeric processor
F8h-FFh	0	0	1	1	1	1	1	Y	Y	x	80287 command ports

I/O subsystem Bit usage:

ADDR 61h Port B <<READ/WRITE>>
- 0 r/w + Timer 2 Gate speaker
- 1 r/w + Speaker data
- 2 r/w + Disable/Clear failsafe timer
- 3 r/w + Disable/Clear I/O channel error
- 4 ro + refresh detect
- 5 ro + Timer channel 2 output
- 6 ro + I/O channel error
- 7 ro + Fail safe timer interrupt

ADDR 70h CMOS clock address/NMI Mask register
- 0-5 CMOS address bits
- 7 -NMI enable

INTERRUPT CONTROLLER

The 8259A interrupt controllers subsystem handles interrupt requests from the system bus, the system timer, the keyboard, and the numeric coprocessor. Interrupt requests from controller 2 are cascaded into IRQ2 of controller 1. Controller 1 is a MASTER controller, controller 2 is a SLAVE as indicated by the SP/EN input to the devices. The arbitration between controllers is communicated over the CASx lines during the time between the interrupt acknowledge cycles. The interrupt levels for each line are shown below in priority order:

SW int	Interrupt	
INT 8	IRQ0-1	SYSTEM TIMER (8253 TIMER 0)
INT 9	IRQ1-1	KEYBOARD CHAR AVAILABLE
na	IRQ2-1	Interrupt from CTLR2
INT 70	IRQ8-2	CMOS clock interrupt
INT 71	IRQ9-2	BUS PIN B04 (software redirected to INT A)
INT 72	IRQ10-2	BUS PIN D03
INT 73	IRQ11-2	BUS PIN D04
INT 74	IRQ12-2	BUS PIN D05
INT 75	IRQ13-2	Numeric Coprocessor (Software redirected to INT 2)
INT 76	IRQ14-2	BUS PIN D07
INT 77	IRQ15-2	BUS PIN D06
INT B	IRQ3-1	BUS PIN B25
INT C	IRQ4-1	BUS PIN B24
INT D	IRQ5-1	BUS PIN B23
INT E	IRQ6-1	BUS PIN B22
INT F	IRQ7-1	BUS PIN B21

The interrupt controllers are located on the I/O data bus IOD<7:0> in order to provide adequate buffering from the system bus. Because of this, the interrupt acknowledge cycle requires the D4-SPPI PAL to decode the CIORD* signal active.

NON MASKABLE INTERRUPT CIRCUITS

The NMI (Non Maskable Interrupt) input to the processor is activated from the expansion bus I/OCHK circuit described below. The NMI input can be masked off by the hardware by setting the NMI Mask register (Add 70h bit 7) to a 1. In order to receive an interrupt the mask register must be set to a 0. Note that this address is shared by the CMOS clock address register so that it is necessary to reprogram the address register before each access to the CMOS clock.

EXPANSION BUS INTERRUPT line (A1)

The expansion bus IOCHK* circuit contains an error latch and an enable latch (port 61h bit 3). The error latch state can be read on port 61h bit 6 where a 1 indicates the error. This latch can be cleared by setting the I/O CHECK disable latch to a 1 momentarily. To prevent any I/O CHECK errors from generating an interrupt, set the I/O CHECK enable latch to a 1 to disable the error circuit.

FAILSAFE TIMER INTERRUPT

The failsafe timer NMI circuit contains an interrupt latch and an enable latch (port 61h bit 2). The interrupt latch state can be read on port 61h bit 7 where a 1 indicates the interrupt. This latch can be cleared by setting the failsafe timer enable latch to a 1 momentarily. To prevent any failsafe timer interrupts from generating an interrupt, set the failsafe timer enable latch to a 1 to disable the interrupt circuit. This circuit can be permanently disabled by turning SW1-1 OFF.

SPEED CONTROL TIMER

The speed control timer is used to slow down the cpu execution rate as described in the NON PROCESSOR operations section. To enable the speed reduction, the 8042 keyboard processor port 2 bit 3 is set to a low state and the timer is programmed for MODE 1 with a count between 2 and 38h. The larger the count, the slower the system will be. If a count greater than 38h is entered, then the system may lock up (speed goes to zero). This speed control also depends on the refresh rate as programmed into the refresh timer. If the refresh timer is programmed faster than it's normal value (19 decimal) then the maximum speed count will be less (or the system will lock up).

NUMERIC COPROCESSOR INTERRUPT AND BUSY

The Numeric coprocessor interrupt and busy subsystem is designed to make the 80287/80387 error handling system as much like previous products as possible. In normal operation, the 80287/80387 will execute it's instructions and set the BUSY7* line active until the instruction is complete. The D4-SNCP PAL will enable the BUSY* line in response to prevent the CPU from sending any more 80287/80387 instructions to the numeric coprocessor.

If an error occurs during the execution of the instruction, the ERROR* line will go active and the BUSY7* line will go inactive. In this case the PAL will cause an interrupt (IRQ13) when ERROR* goes active. To prevent another 80287/80387 instruction from being executed before the error interrupt subroutine is entered, the BUSY* line is then set (even though the BUSY7* input goes inactive).

When the interrupt subroutine is entered, the software should do an output instruction to port F0h to reset the error enable latch (the data written is not important). This in turn clears the interrupt and resets BUSY so processing can continue. The enable error latch (which is cleared by the port F0 write) will remain disabled until software clears the error condition and the ERROR* line goes inactive, enabling the latch and further interrupts.

Due to the design of the 80386, there exists a possibility that the CPU may lock up during some coprocessor instructions which cause an error. The system also contains a timeout circuit which will break the lock up if necessary. If the IRQ13 line is active for more than 15usec and the CPU completes no bus cycles in that time, the BUSY* line is set inactive to break the lock. In this case, the interrupt routine will then be entered before the next instruction.

If a coprocessor is not installed (as indicated by the switch SW1-2 setting off), then the D4-SNCP PAL will simulate it's presence by setting the BUSY* line active for 15usec after each write to the 80287/80387 address space. This prevents the 80386 from locking up while waiting for a response from the 80287/80387.

The 80287 can be reset (hardware reset) seperately from the 80386 by writing to I/O port 0F1h. The data written is not important. The 80387 cannot be reset by the above method, it is reset only at powerup. The only method of initializing the 80387 is the FINIT instruction.

The system board includes a switch (SW1-7) which is used to select between the 80387 and the 80287. This switch MUST be in the correct position for proper operation. If this switch is set to the 80387 position, and the 80387 is not installed, the system will crash. The proper settings are shown below.

SW1-2	SW1-7	80287	80387	
On	On	In	Out	normal operation of 80287
On	Off	Out	In	normal operation of 80387
Off	On	Out	Out	Normal operation without coprocessor
Off	On	Out	In	Normal operation without coprocessor
On	On	In	In	Not recommended (but 287 works)
On	Off	In	In	Not recommended (Improper operation)
Off	On	In	In	Not recommended (error message)
Off	Off	In	In	Not recommended (error message)
On	On	Out	???	Installation error message
Off	On	In	Out	Installation error message
Off	Off	Out	In	Installation error message
On	Off	???	Out	System lockup on x87 instruction
Off	Off	???	Out	System lockup on x87 instruction

KEYBOARD INTERFACE

The keyboard interface system consists of a Universal Peripheral Interface IC (8042 or 8742), a D4-SKEY PAL, and several small components to make connection to the keyboard. The primary device is the UPI, which is a self contained processor. This device serializes and deserializes the codes to and from the keyboard and does several other system functions. Included in these functions are the reporting of the switch settings from the input port (on command), and controlling the CPU reset line and slowdown lockout line. The UPI is also programmed to control the LOWA20 line (for limiting the CPU address to 1 Mbyte) but this function is taken over by the D4-SKEY PAL.

The D4-SKEY PAL watches the commands to the UPI and intercepts those having to do with the LOWA20 line. It then drives that line and prevents the UPI from getting the commands by disabling the keyboard write line (KEYWR*). This response is done within a few DCLK cycles instead of the several hundred UPI clock cycles required by the UPI software.

The PAL circuit is designed to be disabled (in case of compatibility problems) by the removal of a single zero ohm resistor connecting the KA20* line to ground. This line (KA20*) is the enable signal to the D4-SKEY PAL. When this line goes high (by removing the resistor) the LOWA20 and the KEYWR* lines are not driven by the PAL, the UPI resumes driving the LOWA20 line and a resistor between IOWC* and KEYWR* provides the write signal to the UPI to allow normal function of the UPI on the LOWA20 commands.

8049 INPUT PORT

0	Not defined
1	Not defined
2	80287 installed switch
3	80287 speed switch
4	Switch 4
5	Switch 5
6	Switch 6
7	Keyboard inhibit switch

8049 OUTPUT PORT

0	Reset 80286 CPU when low
1	Force address wrap past FFFFFh to 00000 when low.
2	Not Used
3	Enable slowdown when low
4	Keyboard Output buffer full (interrupt to 8259)
5	Keyboard Input buffer full (not used)
6	Keyboard clock line (output)
7	Keyboard data line (output)

8049 TEST PORT

0	Keyboard clock line
1	Keyboard data line

SPEAKER INTERFACE

The speaker interface allows the speaker to be driven from two sources, the 8253 timer 2, or the processor through port 61h bit 1. In addition, the timer can be enabled and disabled from port 61h bit 0. In order to use the timer to generate a tone, it is necessary to program it to the desired frequency (the input clock rate is 1.193 mhz), and set port 61h bits 0 and 1 to a 1. If the speaker is to be toggled directly by the CPU, port 61h bit 0 should be set to a zero and bit 1 should be toggled.

REFRESH TIMER

The system refresh is obtained by doing a DMA request from memory about every 15 usec. The timing is derived from the system clock and the refresh timer 1. In order to achieve the required refresh rate for dynamic memories (128 cycles in 2 milliseconds) the timer must be programmed to 18 or 19.

desired divider value is (.002/128)*1193182 = 18.64
actual refresh rate for 18 is 18*128/1193182 = 1.931 msec
actual refresh rate for 19 is 19*128/1193182 = 2.038 msec

A divider value of 18 results in a refresh rate slightly higher than necessary but this is better than breaking the specified refresh time as a divider value of 19 does.

SYSTEM TIMER

The system timer 0 is connected directly to the interrupt controller so that system timing functions (time of day, Floppy motor timeout etc.) can be done. It is normally programmed by software to a frequency of 18.20678 Hz.

CMOS CLOCK CIRCUITS

The System CMOS clock circuits are used for two purposes. One is to provide an accurate time of day clock, the other is to provide a small amount of permanent memory which is not lost during power off times. The main IC which provides these functions is the MC146818 real time clock chip from Motorola. There is also a CMOS inverter package which is used for an oscillator and to provide a quality chip select to prevent spurious writes during power cycling. The inverter (4069) is used in a series type Pierce oscillator with a 32768 Hz crystal. This circuit is very sensitive due to the extremely small currents used to maintain oscillation and will not work properly if the printed circuit board is dirty or if test instruments probe any of the nodes connected to the crystal.

The power provided to the CMOS circuits is designed to be maintained during power off periods by a battery. To do this, a diode switching circuit is used to switch from the output of a special regulator to the battery source. A diode is used to reduce the battery voltage from the battery connecter to between 4.5v and 5.5v at the clock ICs. The regulator is a shunt type from the +12v supply and provides 6.2v before the diode. With the power on, the voltage at the clock ICs should be about 5.5v. The choice of voltages should prevent the battery from providing the power to the clock circuits when the unit is on. This is necessary because the current drain from the clock is several orders of magnitude higher during system operation than during shutdown.

One additional diode is used to guarantee that the clock ICs do not "latch up" during power cycling with no battery (which could destroy the ICs). This diode guarantees that the Vcc to the clock is never more that 0.7v less than the voltage on the inputs thus preventing the turn on of the spurious SCRs in the CMOS circuits.

The battery voltage range at the battery connector is shown below:

	minimum	maximum	absolute maximum	
1)	5.0v	6.0v	6.2v	
2)				Normally Keyed
3)				
4)	0.0v	0.0v	0.0v	Ground

The absolute max spec is for a battery that is new, and should not be maintained for more than 24 hours at 100 ua. After this time, the normal min/max voltage spec applies.

The current drain on the battery varies with voltage and clock operating mode, but is usually about 50-90 ua after running the diagnostic setup. The maximum current should be under 150 ua.

SWITCH SETTINGS

The processor board has one DIP switch with six individual switches. The function of the switches is as follows;

1) Failsafe timer enable (when ON).
   This switch is normally on.
2) 80287 coprocessor installed (when ON).
   This switch must be ON when the 80287 is installed and OFF when the 80287 is not installed.
3) 4mHz 80287 operation (when ON).
   If an 80287 dash 1,2,8,10 is used then the switch should be OFF. If dash 3 or 6 is used then the switch must be ON.
4) Switch 4 (see software spec for usage)
5) Switch 5 (see software spec for usage)
6) Switch 6 (see software spec for usage)

PROCESSOR POWER REQUIREMENTS

The processor board uses 5v, and 12v power. It distributes power for other components of the system from the -5v, -12v and aux 12v provided by the power supply. With no other components (except the speaker) connected to it, the processor uses 22 milliamp at 12v, and 2.4 amps at 5v. The maximum expected power requirement should be 24 ma at 12v, and 3.0 amps at 5.0v.

ROM MEMORY SYSTEM

The ROM memory system on the memory board consists of four sockets for 28 pin ROMs or EPROMs and decoding logic to enable them. The ROMs can be either 8K, 16K, or 32K x 8 bits in size depending on the arrangement of jumpers xx to xx. The ROM sockets are arranged in two sets of ROMs (16 bits wide) designated SYSTEM ROMs 1 (always present and including address (OFFFF0h) and system ROMs 2 (located at lower address than SYSTEM ROMs 1). There is also a jumper for each bank to select between static and dynamic ROMs. The jumper setting for each type of device is shown below.

8k ROM	PROGRAMMABLE active HI CS ON 26,27
16k ROM	PROGRAMMABLE active HI CS ON 27
32k ROM	
8K EPROM	INTEL 2764 TYPE
16K EPROM	INTEL 27128 TYPE
32K EPROM	INTEL 27256 TYPE

		Standard configuration
ROMS1 (system ROMs):	use jump block ER1:	1 2=3 4=5 6 7=8 9
ROMS2 (option ROMs):	use jump block ER2:	1 2=3 4 5=6 7 8=9

8k Device	1=2 3	4=5 6	
16k Device	1 2=3	4=5 6	
32k Device	1 2=3	4 5=6	
Static device			7=8 9
Dynamic device			7 8=9

The addresses of the ROMs for the three ROM size configurations are shown below.

address	8k devices	16k devices	32k devices
0E0000H	SYSTEM ROMs 2	SYSTEM ROMs 2	SYSTEM ROMs 2
0E2000H	SYSTEM ROMs 2	SYSTEM ROMs 2	SYSTEM ROMs 2
0E4000H	SYSTEM ROMs 2a	SYSTEM ROMs 2	SYSTEM ROMs 2
0E6000H	SYSTEM ROMs 2a	SYSTEM ROMs 2	SYSTEM ROMs 2
0E8000H	SYSTEM ROMs 2b	SYSTEM ROMs 2a	SYSTEM ROMs 2
0EA000H	SYSTEM ROMs 2b	SYSTEM ROMs 2a	SYSTEM ROMs 2
0EC000H	SYSTEM ROMs 2c	SYSTEM ROMs 2a	SYSTEM ROMs 2
0EE000H	SYSTEM ROMs 2c	SYSTEM ROMs 2a	SYSTEM ROMs 2
0F0000H	SYSTEM ROMs 1	SYSTEM ROMs 1	SYSTEM ROMs 1
0F2000H	SYSTEM ROMs 1	SYSTEM ROMs 1	SYSTEM ROMs 1
0F4000H	SYSTEM ROMs 1a	SYSTEM ROMs 1	SYSTEM ROMs 1
0F6000H	SYSTEM ROMs 1a	SYSTEM ROMs 1	SYSTEM ROMs 1
0F8000H	SYSTEM ROMs 1b	SYSTEM ROMs 1a	SYSTEM ROMs 1
0FE000H	SYSTEM ROMs 1b	SYSTEM ROMs 1a	SYSTEM ROMs 1
0FC000H	SYSTEM ROMs 1c	SYSTEM ROMs 1a	SYSTEM ROMs 1
0FE000H	SYSTEM ROMs 1c	SYSTEM ROMs 1a	SYSTEM ROMs 1

The designation "1a", "1b", "1c" etc. means that the contents of the ROM can be found duplicated at this address.

ROM/EPROM speed requirement

The required speed for the ROM or EPROM is given below:

```
Address access time for ROM/EPROM
5 x CLK16 cycle                    312
ALE delay in PAL                 - 15
ALE delay in F00                 -  7
address latch delay als573       - 20
buffer prop delay ls244          - 20
DATA latch setup time            - 10
Latch enable delay in PAL        +  5
CMD* delay from CLK16 in PAL     +  5
ACCESS TIME                 ******** 250

OE access time for ROM/EPROM
OE/CS access time for ROM/EPROM (jumpered dynamic)
4 x CLK16 cycle                    250
CMD* from CLK16* in PAL          - 15
MRDC* from CMD* in PAL           - 25
OE* from MRDC* in PAL            - 25
buffer prop delay ls244          - 20
DATA latch setup time            - 10
Latch enable delay in PAL        +  5
CMD* delay from CLK16 in PAL     +  5
ACCESS TIME                 ******** 165

CS access time for ROM/EPROM (jumpered static)
5 x CLK16 cycle                    312
ALE delay in PAL                 - 15
BALE delay from ALE in F00       - 10
ROM* from BALE in PAL            - 25
buffer prop delay ls244          - 20
DATA latch setup time            - 10
Latch enable delay in PAL        +  5
CMD* delay from CLK16 in PAL     +  5
ACCESS TIME                 ******** 242
```

D4 OPTION BOARD SLOT SPECIFICATIONS. (no memory on motherboard)

```
Slot
1 2 3 4 5 6 7 8
x . . . . . . .       32 bit.
. . x x . x x .       16/8 bit.
. x . . x . . x       8 bit only.
x . . . x x x x       drop down to gold finger edge.
. . . . . . . .       drop down to motherboard surface.
. x x x . . . .       no drop down available.
x x x x x x x .       full size
. . . . . . . x       short slot (6 inch)

1 . . . . . . .       Used for standard memory board
  2 . . . . . .       Available
    3 . . . . .       Available
      4 . . . .       Available
        5 . . .       VDU
          6 . .       Hard Disk
            7 .       Floppy/Serial/Printer
              8       Available
  L8;R78
```

EXPANSION BUS DEFINITION

BUS Pin	Signal Name	Description

A01 IOCHK* This input signal is used to signal the CPU about parity or other serious errors on adapter cards plugged into the expansion bus. This signal should be driven low by an open collector type output capable of sinking 20 mA when an uncorrectable system error occurs.

A02-A09 SD7-SD0 These bidirectional signals are the low 8 bits of the system data bus. They should be used exclusively by all eight bit devices to transfer data. Sixteen bit devices should use these lines to transfer only the low half of a data word when the address line A0 is low. These may be driven by an expansion bus adapter acting as a bus master.

A10 BUSRDY This input signal is used to lengthen a bus cycle from it's standard time if a bus adapter cannot respond quickly enough. It should be pulled low by an open collector type device as soon as a slow addressed device is selected and held low until the device has responded. Bus cycles are lengthened by an integral number of (BCLK) cycles. This line should not be held low for more than 2.5 microseconds. This line should be driven by an open collector device capable of sinking 20 mA.

A11 AEN This output signal when inactive (low) indicates that the CPU or other adapter mounted bus master has control of the bus. When active, the DMA controller has control of the bus. It is often used to disable devices which must not respond during a DMA cycle.

A12-A31 SA19-SA0 These bidirectional signals address memory or I/O devices within the system. They form the low order 20 bits of the 24 bit address bits that the system offers. These lines are enabled onto the bus while BALE is high and are latched when BALE goes from a high to a low state. These may be driven by an expansion bus adapter acting as a bus master.

B02 RESDRV This output signal is used to reset the hardware during powerup or power failure. It is active high.

B04 IRQ9
B21 IRQ7
B22 IRQ6
B23 IRQ5
B24 IRQ4
B25 IRQ3
D03 IRQ10
D04 IRQ11
D05 IRQ12
D06 IRQ15
D07 IRQ14 These input lines are used to interrupt the CPU to request some service. The interrupt is recognized when the line goes from a low to a high and remains there until the appropriate interrupt service routine is executed.

B06 DRQ2
B16 DRQ3
B18 DRQ1
D09 DRQ0
D11 DRQ5
D13 DRQ6
D15 DRQ7 These input lines are used to request a DMA service from the DMA subsystem or to gain control of the system bus from the main CPU (Dma ReQuest). The request is made when the line goes from a low to a high and must remain there until the appropriate DAKx (Dma AcKnowedge) line goes active.

B08 NOWS* This input line (No Wait State) is used to inform the system that standard wait states can be deleted for cycles when this line is made active. The line must be pulled low before the falling edge of BCLK in order to be recognized. This line should be driven by an open collector device capable of sinking 20 mA.

B11 SMWTC* This output line (standard memory write) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MWTC*.

B12 SMRDC* This output line (standard memory read) is active (low) only when an address from 000000h to 0FFFFFh is decoded. This line is derived from MRDC*.

B13 IOWC* This output line (I/O write) indicates (when low) when an I/O device is to accept the data from the data bus. It may be driven by an expansion bus adapter acting as a bus master.

B14 IORC* This output line (I/O read) indicates (when low) when an I/O device is to send data to the data bus. It may be driven by an expansion bus adapter acting as a bus master.

B15 DAK3*
B17 DAK1*
B26 DAK2*
D8 DAK0*
D10 DAK5*
D12 DAK6*
D14 DAK7* These output lines (Dma AcKnowedge) indicate that a request for a DMA service from the DMA subsystem has been recognized. The acknowledge is indicated by a LOW on this line. This line should be used to decode the DMA device with the IORC* or IOWC* line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to pull GRAB* low.

B19 REFRESH* This output signal is used to indicate (when low) a refresh cycle in progress. It should be used to enable the SA0-SA7 address lines to the row address inputs of all banks of dynamic memory so that when the MRDC* goes active, the entire system memory is refreshed at one time. It may be driven by an expansion bus adapter acting as a bus master.

B20 BCLK This output signal is provided to allow synchronization to the main processor clock. Its frequency will be approximately 8MHz with a duty cycle of 50%.

B27 T/C This output signal (when high) indicates that the terminal count of a DMA operation has been reached. It should be decoded with the appropriate DACKx line for proper operation.

B28 BALE This output signal (when high) indicates that a valid address is present on the LAxx address lines. The LAxx address lines or any decodes developed from them should be latched at the falling edge of BALE. This line is always high when a DMA or bus master operation is occurring.

B30 OSC This output signal is a clock for use in timing applications. It's frequency is 14.31818 MHz and duty cycle is appoximately 50%.

C1 SBHE* This output signal (System Bus High Enable) indicates (when low) that the high half of the SDx data bus should transfer the data on adapters which support the full 16 bit data bus. It may be driven by an expansion bus adapter acting as a bus master.

C2-C8 LA23-LA17 These output signals (Latchable Address) are used to decode memory which must respond with zero or one wait state. They are only guaranteed to be valid when BALE is high. These may be driven by an expansion bus adapter acting as a bus master.

C9 MRDC* This output line (memory read) indicates (when low) when a memory device is to send data to the data bus. This signal is active over the entire address space of the system. It may be driven by an expansion bus adapter acting as a bus master.

C10 MWTC* This output line (memory write) indicates (when low) when a memory device is to accept the data from the data bus. This signal is active over the entire address space of the system. It may be driven by an expansion bus adapter acting as a bus master.

C11-C18 SD08-SD15 These bidirectional signals are the high 8 bits of the system data bus. Sixteen bit devices should use these lines to transfer the high half of a data word when the line SBHE* is low. These may be driven by an expansion bus adapter acting as a bus master.

D1 M16* This input line (Memory is 16 bits) signals the system that the addressed memory is capable of transferring 16 bits of data at once. When this line is made active, during a memory read or write, the standard one wait state memory cycle will be run. This line should be derived from the LAxx address lines. This line should be driven low by an open collector device capable of sinking 20 mA.

D2 IO16* This input line (I/O is 16 bits) signals the system that the addressed I/O device is capable of transferring 16 bits of data at once. When this line is made active, during an I/O read or write, the standard one wait state I/O cycle will be run. This line should be driven low by an open collector device capable of sinking 20 mA.

D17 GRAB* This input signal is used to indicate that an adapter mounted bus master is controlling the bus. An adapter may pull this line low when the appropriate DAKx line is made active, signalling that a master request is granted. The system address, data and control lines will be floated, allowing the adapter to begin controlling them one full BCLK period after GRAB is made active. At least one more full BCLK period should be allowed after putting a valid address on the bus before activating any of the control lines. This line should be driven by an open collector device capable of sinking 20 mA.

B01,B10,B31,D18 GND These lines are connected to the system AC and DC ground. The maximum current allowed on any single contact is 1.5 amps.

B03,B29,D16 +5 Vdc These lines are connected to the system power supply for 5 volts. In addition to the maximum power available from the supply, the maximum current allowed on any single contact is 1.5 amps.

B5 -5 Vdc This line is connected to the system power supply for minus 5 volts. This supply is intended for low current usage only.

B7 -12 Vdc This line is connected to the system power supply for minus 12 volts. This supply is intended for low current usage only.

B9 +12 Vdc This line is connected to the system power supply for 12 volts. In addition to the maximum power available from the supply, the maximum current allowed on this contact is 1.5 amps.

BUS TIMING INFORMATION

This information assumes that the system clocks are at a constant 8mHz. Since in some cases this is not true, some cycles may have more time available than indicated.

CPU 8 bit command active time (standard wait state)	
9 x CLK16 cycle	567
CPU 8 bit command active time (NO standard wait state)	
3 x CLK16 cycle	187
CPU 16 bit memory command active time (standard wait state)	
4 x CLK16 cycle	250
CPU 16 bit I/O command active time (standard wait state)	
3 x CLK16 cycle	187
CPU 16 bit memory command active time (NO wait state)	
2 x CLK16 cycle	125
CPU extra wait state size	
2 x CLK16 cycle	125
Address access time from SAx address lines, 16 bit bus read cycle.	
5 x CLK16 cycle	312
ALE* active delay in PAL	- 15
ALE* TO ALE in F00	- 6
address latch delay als573	- 20
Latch setup time als573	- 10
CMD from CLK16* in PAL	+ 6
BCKx from CMD in PAL	+ 8
ACCESS TIME ********	275

Address access time from SA19-SA0 address lines, 8 bit bus read cycle.

11 x CLK16 cycle		687
ALE* active delay in PAL		- 15
ALE* TO ALE in F00		- 6
address latch delay als573		- 20
Copy buffer delay ls245		- 15
Latch setup time als573		- 10
CMD from CLK16* in PAL		+ 6
BCKx from CMD in PAL		+ 8
ACCESS TIME	********	635

Access time from BALE active, 16 bit bus read cycle.

5 x CLK16 cycle		312
ALE* active delay in PAL		- 15
BALE from ALE in F00		- 9
Latch setup time als573		- 10
CMD from CLK16* in PAL		+ 6
BCKx from CMD in PAL		+ 8
ACCESS TIME	********	292

MRDC* Access time, 16 bit bus read cycle.

4 x CLK16 cycle		250
MRDC* from CMD in PAL		- 15
Latch setup time als573		- 10
BCKx from CMD in PAL		+ 8
ACCESS TIME	********	233

IORC* access time, 16 bit bus read cycle.

3 x CLK16 cycle		187
IORC* from CMD in PAL		- 15
Latch setup time als573		- 10
BCKx from CMD in PAL		+ 8
ACCESS TIME	********	170

MRDC*, IORC*, access time, 8 bit bus read cycle.

9 x CLK16 cycle		562
MRDC* from CMD in PAL		- 15
Copy buffer delay ls245		- 18
Latch setup time als573		- 10
BCKx from CMD in PAL		+ 8
ACCESS TIME	********	527

SMRDC* access time, 8 bit bus read cycle.

9 x CLK16 cycle		562
MRDC* from CMD in PAL		- 15
SMRDC* from MRDC* in LS125		- 18
Copy buffer delay ls245		- 18
Latch setup time als573		- 10
BCKx from CMD in PAL		+ 8
ACCESS TIME	********	509

Data hold time from MRDC*, IORC*, 8 and 16 bit cycles

data hold from BCKx ALS573		7
BCKx delay from CMD in PAL max		15
DCMD from CMD in PAL min		- 8
command from CMD in PAL min		- 8
Required data hold	**********	6

LAx address valid to 16 bit memory command setup

3 * CLK16		187
CPU address out from CLK16 max		- 40
Address buffer delay ALS245 max		- 17
CMD from CLK16* in PAL		+ 6
command from CMD in PAL		+ 5
SETUP	*********	141

LAx address valid to M16* active requirement

3 * CLK16		187
CPU address out from CLK16 max		- 40
Address buffer delay ALS245 max		- 17
M16* setup required to ALE in PAL		- 25
SETUP	*********	105

BALE valid to 16 bit memory command setup

1 * CLK16		62
ALE* active delay in PAL		- 15
BALE from ALE* in F00		- 9
CMD from CLK16* in PAL		+ 6
command from CMD in PAL		+ 5
SETUP	*********	49

BALE valid to required M16*

1 * CLK16		62
ALE* active delay in PAL		- 15
BALE from ALE* in F00		- 9
M16* setup in PAL		- 25
SETUP	*********	13

SAx address valid to 16 bit memory command setup

1 * CLK16		62
ALE* active delay in PAL		- 15
BALE from ALE* in F00		- 9
CMD from CLK16* in PAL		+ 6
command from CMD in PAL		+ 5
address latch delay ALS573		- 20
SETUP	*********	29

SAx address valid to I/O, 8 bit command setup

2 * CLK16		125
ALE* active delay in PAL		- 15
BALE from ALE* in F00		- 9
CMD from CLK16* in PAL		+ 6
command from CMD in PAL		+ 5
address latch delay ALS573		- 20
SETUP	*********	92

SA<19-0> address hold from command

1 * CLK16		62
CMD from CLK16* in PAL		- 15
command from CMD in PAL		- 15
ALE* active delay in PAL min		+ 5
ALE* TO ALE in F00		+ 2
address latch delay als573 min		+ 7
HOLD	*********	46

CPU write data setup to MWTC* active, 16 bit bus memory cycle.

CLK16 time		62
MWTC* in PAL delay min		5
BENx delay in PAL max		- 25
data buffer delay LS245		- 40
SETUP	*********	2

CPU write data setup to IOWC* active

2 * CLK16		125
MWTC* in PAL delay min		5
BENx delay in PAL max		- 25
data buffer delay LS245		- 40
SETUP	*********	65

CPU write data setup to MWTC*, IOWC* active, 8 bit bus

MWTC* to CPYEN* in PAL delay		- 25
data buffer delay LS245		- 40
SETUP	*********	- 65

CPU write data setup to MWTC*, IOWC*, inactive, 16 bit bus memory cycle.

5 * CLK16 time max		312
BENx* delay in PAL max		- 25
data buffer delay LS245		- 40
MWTC* in PAL delay min		5
SETUP	*********	252

CPU write data setup to MWTC*, IOWC*, inactive, 8 bit bus memory cycle LOW BYTE.

9 * CLK16 time max		562
BENx* delay in PAL max		- 25
data buffer delay LS245		- 40
MWTC* in PAL delay min		5
SETUP	*********	502

CPU write data setup to MWTC*, IOWC*, inactive, 8 bit bus memory cycle HIGH BYTE.

9 * CLK16 time max		562
CDPYEN* delay in PAL max		- 25
data buffer delay LS245		- 40
SETUP	*********	497

Refresh MRDC* active time

DCLK cycle time		250

Refresh address setup to MRDC* active

2 * CLK16		125
ls590 delay max		- 45
LS244 DELAY (SA8,SA9)		- 18
ls125 delay min		+ 7
SETUP (SA8,SA9)	*********	69

```
Refresh address hold from MRDC* inactive
        ls590 delay min                          +  5
        ls125 delay max                          - 20
        SETUP                  **********        - 15

Refresh wait state BUSRDY low delay from MRDC* active
        2 * CLK16                                 125
        f175 delay max                           - 10
        ls125 delay max                          - 20
        f125 setup max                           -  3
        Max allowed delay      **********          92

Refresh wait state BUSRDY high setup to BCLK rising
        f125 setup max                              3
        F08 delay                                 6.6
        SETUP                  **********          10

CPU memory or I/O command wait state
BUSRDY high setup to BCLK rising
        F74 setup max                               3
        SETUP                  **********           5

CPU 16 bit memory command wait state
BUSRDY low delay from command active
        3 * CLK16                                 187
        CMD from CLK16* in PAL                   - 15
        command from CMD in PAL                  - 15
        F74 preset delay                         - 11
        F175 setup max                           -  3
        Max allowed delay      **********        143

CPU 16 bit I/O command wait state
BUSRDY low delay from command active
        2 * CLK16                                 125
        CMD from CLK16* in PAL                   - 15
        command from CMD in PAL                  - 15
        F74 preset delay                         - 11
        F175 setup max                           -  3
        Max allowed delay      **********         81

CPU 8 bit command wait state
BUSRDY low delay from command active
        8 * CLK16                                 500
        CMD from CLK16* in PAL                   - 15
        command from CMD in PAL                  - 15
        F74 delay max                            - 11
        F175 setup max                           -  3
        Max allowed delay      **********        456

CPU minimum command active from BUSRDY high after added wait state.
        2 * CLK16                                 125
        CMD from CLK16* in PAL                   +  6
        command from CMD in PAL                  +  8
        F74 setup min                            +  0
        Command active         **********        139
```

CPU maximum command active from BUSRDY high after added wait state.

4 * CLK16		250
CMD from CLK16* in PAL		+ 15
command from CMD in PAL		+ 15
F74 setup max		+ 3
Command active	**********	283

NOWS* delay from MRDC* or MWTC* 16 bit memory cycles

1 * CLK16		62
CMD from CLK16* in PAL		- 15
command from CMD in PAL		- 15
F74 setup min		- 3
Max allowed delay	**********	29

DMA memory read, I/O write command additional wait state
BUSRDY low delay from memory read command active

4 * CLK16		250
f74 delay max		- 11
ls125 delay max		- 20
LS243 delay max		- 18
f74 delay BUSRDY to DRD1 max		- 11
f175 setup		- 3
Max allowed delay	**********	187

DMA I/O read, memory write command additional wait state
BUSRDY low delay from I/O read command active

8 * CLK16		500
I/O write delay from DCLK max		-190
ls243 delay max		- 15
f74 delay BUSRDY to DRD1 max		- 11
f175 setup		- 3
Max allowed delay	**********	281

DMA MRDC* active time

2 x DCLK cycle		500

DMA IORC* active time

3 x DCLK cycle		750

DMA MWTC*, IOWC* active time

2 x DCLK cycle		500
8237 Write command shrinkage		100
Active cycle time	**********	400

System memory read access time from MRDC* (Non CPU cycles)

M-IO from MRDC* in PAL		15
4 x CLK32 (DMIO to MCAS*)		125
MCAS* to CASx* in F32 delay max		15
CAS access time in RAM max		25
Data buffer delay F657 (mem card)		10
Data buffer delay LS245		15
Data buffer delay ALS245 (copy buf)		15
Access time	**********	220

Data setup to MWTC* for system RAM (Non CPU cycles)

M-IO from MWTC* in PAL		- 10
4 x CLK32 (DMIO to MCAS*)		-125
MCAS* to CASx* in F32 delay max		- 10
Data buffer delay F657 (mem card)		10
Data buffer delay LS245		15
Data buffer delay ALS245 (copy buf)		15
Data setup before MWTC* **********		-100

Required I/O data access time from IORC* for DMA write to RAM

4 * CLK16 cycle time (IORC* to MWTC*)		250
System RAM data setup before MWTC*		100
DMA I/O read access time *********		350

DATA valid after IOWC* low during DMA read from RAM

DMRQ* from DCLK in F74 delay		11
XMRDC* from DMRQ* in ls125 delay		18
MRDC* from XMRDC* in ls243		15
System memory access time from MRDC*		220
XIOWC* from DCLK in 8237 min?		- 70
IOWC* from XIOWC* in LS243		- 15
DMA data valid from IOWC* low	********	179

DATA setup to IOWC* high during DMA read from RAM

2 x DCLK cycle time		500
DMA controller Write low shrinkage		- 100
DMA data valid from IOWC* low		- 179
Data setup to IOWC* high	********	221

32 BIT EXPANSION BUS DEFINITION

BUS Pin	Signal Name	Description

E38 PARIT*

This input signal is used to signal the CPU about parity errors. This signal has a 20kohm pullup resistor and may be driven low by either an open collector type output or a normal output capable of sinking 4.0 mA and sourcing 1.0 mA when an uncorrectable system error occurs.

E2-F5 PD0-PD7

These bidirectional signals are the 8 bits of the processor data bus selected at an address that ends in 00 (binary). They should be used for the transfer of memory data when the 32 bit bus is selected. These lines should be driven during 32 bus memory read cycles when qualified by the BE0* signal going active. At other times this bus should not be driven. During a write cycle the data on these lines is valid only when BE0* is active. The bus should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state when driven by the motherboard and a maximum capacitive loading of 40pF. The 32 bit board must be able to drive 120pF and sink 4.0mA and source 1.0mA when driving these lines.

E6-F9 PD8-PD15

These bidirectional signals are the 8 bits of the processor data bus selected at an address that ends in 01 (binary). These lines are qualified by BE1* similar to PD0-PD7 and BE0* described above. The electical parameters are the same as PD0-PD7 described above.

E10-F13 PD16-PD23

These bidirectional signals are the 8 bits of the processor data bus selected at an address that ends in 10 (binary). These lines are qualified by BE2* similar to PD0-PD7 and BE0* described above. The electical parameters are the same as PD0-PD7 described above.

E14-F17 PD24-PD31

These bidirectional signals are the 8 bits of the processor data bus selected at an address that ends in 11 (binary). These lines are qualified by BE3* similar to PD0-PD7 and BE0* described above. The electical parameters are the same as PD0-PD7 described above.

E18-F28 PA2-PA23

These output signals (in addition to PA31) address memory devices and special control registers on the 32 bit memory bus. They form the high order 22 bits of the 24 bit standard address that the system offers. The bus should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E36 PA31

This output signal (in addition to PA2-PA23) addresses special control registers or system memory on the 32 bit memory bus. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E35 LOWA20

This output signal (when low) indicates when the address line PA20 should be ignored and the address decoded as if the PA20 line was low. When high, the PA20 line is decoded as normal. This is used to provide software compatibility for those programs that expect only a 1 megabyte address space. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

F30 BE0*

This output signal (when low) indicates when the 32 bit memory board should operate on the PD0-PD7 data lines. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E30 BE1*

This output signal (when low) indicates when the 32 bit memory board should operate on the PD8-PD15 data lines. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

F29 BE2*

This output signal (when low) indicates when the 32 bit memory board should operate on the PD16-PD23 data lines. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E29 BE3*

This output signal (when low) indicates when the 32 bit memory board should operate on the PD24-PD31 data lines. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

B02 RST*

This output signal is used to reset the hardware during powerup or power failure. This signal is not synchronous with the CLK32 or CLK16* lines. It is active low.

E33 CLK32

This output signal is the main processor clock. Its frequency will be 32mHz with a duty cycle of about 50%. This line should be used as the timing reference for all processor memory cycles. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

F33 CLK16*

This output signal provides a reference for the internal processor clock phase. Its frequency will be 16mHz with a duty cycle of about 50%. This line will be high during CPU phase one and low during phase two. The line should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

F34 M32*

This input signal (when low) indicates that the 32 bit memory board has decoded an address which it will handle. This line should be decoded ONLY off the address and LOWA20 lines as it will be used during both CPU cycles and other bus master cycles. This signal has a 20kohm pullup resistor to hold it inactive when a 32 bit board is not installed and should be driven by an output capable of sinking 4.0 mA and sourcing 1.0 mA with a 50pF load.

F36 BHLDA

This output signal when inactive (low) indicates that the CPU has control of the bus. When active, some other bus master has control of the bus. This line should be used to determine the protocal used by the memory board for a memory cycle. The signal should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E31 ADS*

This output signal (when rising) indicates that valid status and address has been put on the bus by the CPU and the 32 bit memory board should begin (or complete) it's cycle if it is selected (M32* set low). This line is always high when a DMA or bus master operation is occurring. The signal should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

F31 M-IO

This output signal is one of the status lines which indicate the type of cycle that is in progress. Refer to the status cycle type table for the type of cycle indicated. The signal should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E32 D-C

This output signal is one of the status lines which indicate the type of cycle that is in progress. Refer to the status cycle type table for the type of cycle indicated. The signal should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

F32 W-R

This output signal is one of the status lines which indicate the type of cycle that is in progress. Refer to the status cycle type table for the type of cycle indicated. The signal should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E34 MRDY*

This input signal is used to signal the end of a memory cycle when the 32 bit board is accessed by the CPU. This signal has a 20kohm pullup resistor to hold it inactive when a 32 bit board is not installed and should be driven by an output capable of sinking 4.0 mA and sourcing 1.0 mA with a 50pF load.

F38 NAM*

This input signal is used to signal the CPU when the 32 bit board is finished with the address and status information and the CPU may put out it's next address. This signal has a 20kohm pullup resistor to hold it inactive when a 32 bit board is not installed and should be driven by an output capable of sinking 4.0 mA and sourcing 1.0 mA with a 50pF load.

F37 READY*

This output signal indicates the end of a CPU cycle by either the 32 bit memory board or the system board. The signal should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

E37 NA*

This output signal indicates when the system board or the memory board is done with the address and status information and the CPU may put out it's next address. The signal should have a maximum of 1.0mA load in the low state and 0.4mA load in the high state and a maximum capacitive loading of 40pF.

F1,F39,F40 GND

These lines are connected to the system AC and DC ground. The maximum current allowed on any single contact is 1.5 amps.

E1,E39,E40 +5 Vdc

These lines are connected to the system power supply for 5 volts. In addition to the maximum power available from the supply, the maximum current allowed on any single contact is 1.5 amps.

Cycle types as indicated by status:

BHLDA	M-IO	D-C	W-R	
L	L	L	L	CPU Interrupt Acknowledge
L	L	L	H	Code never produced
L	L	H	L	CPU I/O read
L	L	H	H	CPU I/O write
L	H	L	L	CPU Memory code read
L	H	L	H	CPU halt or shutdown
L	H	H	L	CPU Memory data read
L	H	H	H	CPU Memory data write
H	L	L	L	Code never produced
H	L	L	H	Non CPU refresh read
H	L	H	L	Non CPU memory write
H	L	H	H	Non CPU memory read (note 1)
H	H	L	L	Code never produced
H	H	L	H	Non CPU refresh cycle (Before or after)
H	H	H	L	Non CPU not produced (note 1)
H	H	H	H	Non CPU No cycle in progress

Note 1: possible occurance on transition to/from memory write.
Note 2: other status lines are not guaranteed to be high until after the transition of BHLDA from low to high

BUS TIMING INFORMATION

Status inactive setup to BHLDA high

D4-SMSC turnon pal min		4
SETUP	*********	4

Status inactive hold to BHLDA low

CLK16* cycle time		62
386 HOLDA delay min		+ 4
D4-SMSC delay max		- 15
HOLD	*********	51

Refresh cycle time (M-IO low time)

2 * BCLK cycle		250
ls125 delay delta		+/- 10
D4-SCMD pal min		+/- 5
CYCLE time max	*********	235
CYCLE time min	*********	265

Refresh address setup to M-IO low

BCLK cycle		125
ls590 delay max		- 25
ls244 delay max		- 18
ls245 delay max		- 18
ls125 delay min		+ 7
D4-SCMD pal min		+ 5
SETUP	*********	76

Refresh address hold from M-IO high

ls590 delay min		+ 5
ls245 delay min		+ 5
ls125 delay max		- 20
D4-SCMD pal max		- 15
HOLD	**********	- 25

Data setup before M-IO low during BHLDA high write cycle

MWTC* to M-IO in D4-SCMD pal delay min		+ 5
286 product data setup to MWTC*		- 48
data delay in ls245		- 18
SETUP	**********	- 61

Required data access time from M-IO during BHLDA high read cycles

286 product access time from MRDC*		200
D4-SCMD pal max		- 15
data delay in ls245 max		- 18
REQUIRED ACCESS TIME	**********	167

Minimum cycle time (M-IO low) during BHLDA high

286 product MRDC* low	250

Minimum total cycle time (M-IO low to M-IO low) during BHLDA high

286 product MRDC* low	375

Maximum cycle time (M-IO low) during BHLDA high

286 product MRDC* low	10000

Required MRDY* setup to CLK32 during CPU cycle

386 setup time min		20
F08 delay max		7
SETUP	**********	27

Required MRDY* hold from CLK32 during CPU cycle

386 hold time min		3
F08 delay min		- 2
HOLD	**********	1

Required NAM* setup to CLK32 during CPU cycle

386 setup time min		10
F08 delay max		7
SETUP	**********	17

Required NAM* hold from CLK32 during CPU cycle

386 hold time min		20
F08 delay min		- 2
HOLD	**********	18

Other setup, hold, and delay times from the CPU should be taken directly from the INTEL 80386 specifications.

The 32 bit bus is intended for use by a memory board which is able to respond to CPU requests for data up to 32 bits at a time. This board is also expected to operate at very high cycle rates. Since the master CPU operates at 16mHz clock rate, and uses two clock cycles for a fastest possible memory cycle, the memory board would have to do full speed memory cycles in 125 nsec. Since the CPU allows pipelining of the address and status for the next cycle during the current cycle, the memory board should take advantage of this to gain an effective clock cycle to do address decoding etc. The remainder of this discussion assumes the use of CPU pipelining.

The 32 bit memory board is required to indicate to the system board when an address from the 32 bit bus will be handled by the memory board (assumeing that the cycle type is a memory cycle). This is accomplished by the M32* line. The system board combines this line with the status from the CPU and determines if a legal 32 bit memory cycle is being started. If it is, the system board will do nothing with the CPU, leaving all control to the memory board. If the status indicates some cycle other than memory (even if M32* is active) or if M32* is inactive, the system board logic will run the complete cycle to the CPU including the driving of the NA* and READY* signals.

The system board uses the CPU pipelining ability to get a start on operations. Since the system board cannot know if the next cycle is for the 32 bit memory or system board, it always starts the CPU pipelining with the NAB* signal. Therefore it is required that the memory board understand this and not finish a pipelined memory cycle before the system board is done with a system cycle.

The expected way that the memory board determines that it can run a cycle is to wait for the rising edge of ADS*. This will ensure the completion of any system board cycle and prevent collision of the control logic on the two systems. Memory operations not requireing the driving of MRDY* or the presence of valid write data, can be done before the rising edge of ADS*. Since NAM* will have no direct effect on the CPU until after a previous cycle is complete, it may be driven whenever necessary. Note that since M32* is to be a direct decode from address, it must be driven regardless of ADS*.

If the 32 bit memory board is to operate with no wait states, it will be necessary to drive NAM* as soon as a valid memory cycle is detected (NAM* must be synchronized with the CPU clock). If wait states are inserted then NAM* can be driven later in the memory cycle.

When the 32 bit memory board is finished with a cycle, it must assert MRDY* to tell the CPU that it is complete. During a read cycle, the data should be gated onto the bus during this time.

During non processor cycles (BHLDA is high) the memory board must run the memory cycles at least as fast as the original 286 memory boards because there is no way to add wait states to external bus masters from the 32 bit board. The required access time and cycle time are listed in the timing tables.

When BHLDA is high, the protocal for accessing the memory changes. The M-IO line becomes a memory strobe, and the D-C and W-R lines become equivalent to a refresh control signal and a write enable signal. Note that on the leading edge of BHLDA, that the other status lines may not be valid. Therefor it will be necessary to provide some sort of glitch protection during this transition. Also be aware that the data is not guaranteed to be valid until some time after the M-IO line (memory strobe) appears. This is probably not a problem for dynamic memory, because the RAS to CAS delay will exceed the data setup time, but may be a problem for other memory designs.

PAGE MODE D4 DYNAMIC RAM BOARD

The dynamic memory subsystem for D4 is designed to get the most out of the 80386 processor and still use relatively inexpensive dynamic memories. To do this, the memory subsystem provides the following features:

32 bit wide memory data path.

One megabyte of standard memory using 256k x 1 DRAM ICs and One megabyte of upgrade memory and one of two option boards.

Option RAM board design allows two megabytes of additional memory using 256k x 1 DRAM ICs.

2nd Option RAM board design allows eight megabytes of additional memory using 1024k x 1 DRAM ICs or 256k x 4 DRAM ICs.

16 mHz operation of the processor/memory interface.

Two wait states on the first CPU memory cycle following a hold or idle state. (INITIAL CYCLE).

Zero wait states when sequential memory cycles fall within the same 2048 byte address page. (PAGE HIT CYCLE).

Two wait states when sequential memory cycles do NOT fall within the same 2048 byte address page. (PAGE MISS CYCLE).

Seperate Parity checking on each byte of the 32 bit double word.

Diagnostic port allows the determination of the specific bytes within the double word on which a parity error occurred.

ROM "replacement" ability; 128k bytes of the RAM may be used to replace the system ROMs to increase the speed of the ROMs to RAM speed.

The ROM "replacement" RAM area can be protected from being written by errant software.

This "Page Mode" usage of the dynamic RAM generally averages to about one wait state with typical software or an average cycle time of 187 nsec. Note that "sequential" memory cycles means that the CPU begins requesting a new memory cycle before the current cycle is complete. If the CPU inserts an idle state between cycles because it is busy, the memory system will terminate the "PAGE HIT CYCLE" and revert to an "INITIAL CYCLE".

The system responds to the system DMA and refresh as expected, but since these are much slower than CPU cycles the memory subsystem runs standard multiplexed RAM cycles with no wait states on refresh or DMA.

The memory system can execute 11 different types of memory cycles depending on the conditions of the CPU and DMA. A listing of cycles follows;

1) Initial read cycle from Idle or bus Hold.
2) Initial read cycle from system board cycle.
3) Initial write cycle from Idle or bus Hold.
4) Initial write cycle from system board cycle.
5) Read Page Hit cycle.
6) Write Page Hit cycle.
7) Read Page Miss cycle.
8) Write Page Miss cycle.
9) Refresh cycle.
10) DMA read cycle.
11) DMA write cycle.

The logic for the state to state transitions and the generation of the master memory strobes is contained entirely within one PAL (Programmed Array Logic) device (D4-RCTL). The logic for determining the hit/miss status of a cycle consists of two latches to remember the previous page address and two identity comparitors to check that the current address matches. Since the CPU is operated in the "pipelined address" mode, the address changes before the memory cycle is finished. The column (address within the page) address and byte enables are therefore latched by two more latches. Address multiplexing is accomplished by three multiplexor ICs, and the multiplexed address is buffered by additional buffers (one for each bank of 36 DRAMs). Two additional PAL devices are used to decode the system address, one provides the signal (M32*) which tells everybody that the memory board will control the bus, and the other decodes the address for the two banks of memory on the main memory board.

Data buffering and parity checking is done by four parity trancievers. These devices seperate the memory data bus from the cpu data bus and generate the parity for the DRAMs during write cycles and check the parity during read cycles. The logic that controls the buffers always generates or checks all four bytes even when only a single byte in memory is being accessed. For write operations, the resulting data is ignored by the DRAMs which are not selected. For read operations, a set of pullup resistors on the data bits assures a legal (EVEN) parity check. This also implies that an incomplete bank of DRAM which was enabled, would not cause parity errors during software tests.

ADDRESS DECODING

The memory subsystem responds to the following addresses (address range given in hexadecimal):

ADRESS RANGE	size	BANK	address decoded;
000000-03FFFF	256K	0	always.
040000-07FFFF	256K	0	when the 512k jumper is active (2-3).
080000-09FFFF	128K	0	when the 640k jumper is active (5-6).
0E0000-0FFFFF	128K	0	when ROM replacement active (Note 3).
100000-13FFFF	256K	0	(Note 1).
100000-13FFFF	256K	1	(Note 2).
140000-1FFFFF	768k	1	when the 1M jumper is active (8-9).
200000-2FFFFF	1024k	2	bank 2 on 2M option board when present.
300000-3FFFFF	1024k	3	bank 3 on 2M option board when present.
200000-5FFFFF	4096k	2	bank 2 on 8M option board when present.
600000-9FFFFF	4096k	3	bank 3 on 8M option board when present.
F40000-F7FFFF	256k	0	when the 512k jumper is inactive (1-2).
F80000-F9FFFF	128k	0	when the 640k jumper is inactive (4-5).
FA0000-FDFFFF	256k	0	always.
FE0000-FFFFFF	128k	0	always (Note 3).

80C00000	1 byte	diagnostic byte (read) address.
80C00000	1 byte	control byte (write) address.

Note 1) Actually addresses 000000-03FFFF when LOWA20 is inactive.
Note 2) This is not addressed when LOWA20 is inactive.
Note 3) When ROM replacement is active, writing to this address range can be disabled.

The diagnostic byte (at 80C00000h read only) has several functions. When reading the byte, the value returned is as follows:

bit 0	parity status of byte 0 (0 is error)
bit 1	parity status of byte 1 (0 is error)
bit 2	parity status of byte 2 (0 is error)
bit 3	parity status of byte 3 (0 is error)
bit 4	512k jumper status (0 is active)
bit 5	640k jumper status (0 is active)
bit 6	1M jumper status (0 is active)
bit 7	2 or 8 Mbyte option board (0 is installed)

The control byte (at 80C00000h write only) is shown below.

bit 0	ROM replacement (0 replaces)
bit 1	ROM space write protect (0 protects)
bit 2	reserved (write a 1)
bit 3	reserved (write a 1)
bit 4	reserved (write a 1)
bit 5	reserved (write a 1)
bit 6	reserved (write a 1)
bit 7	reserved (write a 1)

The control byte is also used to clear the diagnostic byte parity status. When writing this byte (with any value) the parity status bits will be reset to ones.

The 128 kbytes from OFE0000h to OFFFFFFh is used to simulate a system ROM. In the original 286 products, this space was occupied (double mapped) by the system ROMs. For the D4 machines, this space is occupied by RAM on this board. To provide compatibility with previous products, the system ROM should be copied to this space. To allow faster execution of ROM resident software, this board provides the ROM "replacement" function. When replacement is enabled, the RAM board decodes address range 00E0000h to 00FFFFFh and puts the 128k of RAM here, replacing the system ROM. After POWERUP, the ROM replacement function is disabled.

Because normal system ROMs could not be written, a write protect function is being included in the RAM board for the two address spaces mentioned above. When replacement is not enabled, only OFE0000h to OFFFFFFh is protected (the normal rom space still contains the unwritable ROM). When replacement is active, both spaces can be protected. After POWERUP, the write protect funtion is disabled.

The diagnostic byte parity status should only be read with the system board IOCHK disabled because reading the port may cause a parity error. As a result of this, the status will only be accurate the first time it is read after a parity clear operation. Before doing a memory test, the control byte should be written to clear the parity status, and after reading the diagnostic byte, the status should be cleared again.

In normal operation, if a parity error occurs, the PARIT* line from the memory card is set active which in turn sets the IOCHK* line to the system active. The IOCHK* line (error) from the memory card is automatically cleared by the first write to memory covered by the board (normally the stack push from the NMI). The parity status is still available until the diagnostic byte is read, so the byte (and board if it is the memory board) in error can be determined.

JUMPER SETTINGS

E123 jumpers

1=2 3 4=5 6 7=8 9	256K	base	000000-03FFFFh
	OK	extended	
1 2=3 4=5 6 7=8 9	512K	base	000000-07FFFFh
	OK	extended	
1 2=3 4 5=6 7=8 9	640K	base	000000-9FFFFFh
	OK	extended	
1=2 3 4=5 6 7 8=9	256K	base	000000-03FFFFh
	1024K	extended	100000-1FFFFFh
1 2=3 4=5 6 7 8=9	512K	base	000000-07FFFFh
	1024K	extended	100000-1FFFFFh
1 2=3 4 5=6 7 8=9	640K	base	000000-9FFFFFh
	1024K	extended	100000-1FFFFFh

The following jumper settings are to be avoided at all cost;

1 2 3=4 5 6 7 8 9	destroy power supply
1 2 3 4 5 6=7 8 9	destroy power supply

OPTION BOARD PRESENT BITS

8M	2M			
H	H	OK		
H	L	2048K	200000-3FFFFFh	
L	H	6144K	400000-9FFFFFh	(NOTE: The 8 Meg board asserts
L	L	8192K	200000-9FFFFFh	both 8M and 2M strobes)

DETAIL CYCLE DESCRIPTION

INITIAL READ CYCLES FROM IDLE. All CPU memory cycles start with the processor presenting an address, status, and address strobe (ADS*). The memory system decides whether to respond to these in the D4-RM32 PAL. This device decodes the address and jumpers and asserts the M32* line active. The system board uses this line to disable itself and the memory board control PAL (D4-RCTL) uses the line (in combination with the status and ADS*) to start a cycle.

In the initial cycle case, the control state machine begins by switching the DRAM address multipexor to the ROW address via the signal SWMUX*. One CLK32 cycle later, the Master Row Address Strobe (MRAS*) is asserted. MRAS* is combined with a decoded bank select signal (RSx*) to form the complete RASx* strobe for the memories.

The bank select signal is decoded in a PAL (D4-RRAS) from a set of latched row addresses. The row address latches are of the "fall through" type, they are open to address changes when MRAS* is inactive (high). The main purpose of the latches is to provide a memory of the last row address for development of the hit/miss signal but they also buffer the processor address for the bank decode PALs to prevent overloading of the CPU.

Once RASx* is active, the SWMUX* signal changes back to the column address (one CLK32 cycle later to satisfy row address hold times). At the same time, the NAM* signal (next address) is set active to tell the CPU that it may put the next address onto the bus (two CLK32 cycles later).

After one CLK32 cycle, the column address latch is closed to prevent the column address from changing during the CAS* cycle. Also the MRD* signal is set active to enable the data buffer to the CPU. After an additional clock cycle, the master Column Address Strobe (MCAS*) is set active, enabling DRAM output buffers. At the same time, the processor ready signal is set active (MRDY*) (and the NAM* is set inactive) signalling the presence of data and the end of the cycle to the CPU. Also at the same time, the processor begins to put the next address and status on the bus (if it is ready to).

Two clock cycles later, the memory cycle ends by bringing the MCAS*, MRD*, and MRDY* inactive, and CLAT signal active. During the two cycles, the data from the DRAMS propagates through the data buffers and parity logic and is set up to the CPU. The parity status is checked at the end of this period by the rising edge of MRD*.

The total time from CPU address strobe to the end of MRDY* is eight CLK32 cycles, or four processor states. Since the CPU can execute a memory access in two states, we have inserted two wait states.

INITIAL READ FROM SYSTEM BOARD. The only difference from the initial read from idle is that the memory cycle must wait to begin until the system board is finished with it's cycle. This is determined by ADS* going high. The cycle starts as before with SWM* going active, but MRAS* does not go active until ADS* is sensed inactive. Since the system board can respond to wait states on the system bus, this period of time could be rather long. Once MRAS* goes active, the cycle completes as before.

READ HIT CYCLE. The hit cycles begin during the previous memory cycle (of any CPU type). The M32* signal is active as before and the new row address must be the same as the last row address held in the row latches. The equality is determined by the signal HIT* being active. The ADS*, M32*, status, and HIT* are sampled at the same edge of CLK32 that terminates the previous cycle. If all is well (READ HIT), the MRAS* signal will continue active. Since the MRAS* signal and the particular RAS*** signal is still active, the DRAM has already decoded the row address and internally fetched it to the column selector. All that is necessary is to wait till the column address has changed and settled and the CAS* precharge time has elapsed before another read can occur.

Since the CPU must remain in pipelined state, the NAM* signal is set active again at the beginning of the READ HIT cycle.

The column latch is closed again (CLAT goes inactive) one CLK32 cycle after the beginning of the cycle to prevent the column address from changing during the CAS* cycle. Also the MRD* signal is set active to enable the data buffer to the CPU. After an additional clock cycle, the master Column Address Strobe (MCAS*) is set active, enabling DRAM output buffers. At the same time, the processor ready signal is set active (MRDY*) (and the NAM* is set inactive) signalling the presence of data and the end of the cycle to the CPU. Also at the same time, the processor begins to put the next address and status on the bus (if it is ready to).

Two clock cycles later, the memory cycle ends by bringing the MCAS*, MRD*, and MRDY* inactive, and CLAT signal active. During the two cycles, the data from the DRAMS propagates through the data buffers and parity logic and is set up to the CPU. The parity status is checked at the end of this period by the rising edge of MRD*.

The total time from the end of the previous CPU memory cycle to the end of MRDY* is four CLK32 cycles, or two processor states. Since the CPU can execute a memory access in two states, we have inserted zero wait states.

READ MISS CYCLES. The miss cycles begin during the previous memory cycle (of any CPU type). The M32* signal is active as before and the new row address are different than the last row address held in the row latches. The inequality is determined by the signal HIT* being inactive. The ADS*, M32*, status, and HIT* are sampled at the same edge of CLK32 that terminates the previous cycle. If all is not well (READ MISS), the MRAS* signal will be set inactive.

Once MRAS* is set inactive, the RAS* precharge time must be met. To do this, the control state machine waits two CLK32 cycles and then begins by switching the DRAM address multipexor to the ROW address via the signal SWMUX*. One CLK32 cycle later, the Master Row Address Strobe (MRAS*) is asserted.

Once MRAS* is active, the SWMUX* signal changes back to the column address (one CLK32 cycle later to satisfy row address hold times). At the same time, the NAM* signal (next address) is set active to tell the CPU that it may put the next address onto the bus (two CLK32 cycles later).

After one CLK32 cycle, the column address latch is closed to prevent the column address from changing during the CAS* cycle. Also the MRD* signal is set active to enable the data buffer to the CPU. After an additional clock cycle, the master Column Address Strobe (MCAS*) is set active, enabling DRAM output buffers. At the same time, the processor ready signal is set active (MRDY*) (and the NAM* is set inactive) signalling the presence of data and the end of the cycle to the CPU. Also at the same time, the processor begins to put the next address and status on the bus (if it is ready to).

Two clock cycles later, the memory cycle ends by bringing the MCAS*, MRD*, and MRDY* inactive, and CLAT signal active. During the two cycles, the data from the DRAMS propagates through the data buffers and parity logic and is set up to the CPU. The parity status is checked at the end of this period by the rising edge of MRD*.

The total time from the end of the previous CPU memory cycle to the end of MRDY* is eight CLK32 cycles, or four processor states. Since the CPU can execute a memory access in two states, we have inserted two wait states.

WRITE CYCLES. The four types of write cycles are very similar to the read cycles discussed above. The difference is in two places. Instead of MRD* being set active, the MWE* signal is set. The MCAS* is enabled one clock cycle later to allow an adequate data setup time to the DRAM ICs and only lasts for one CLK32 cycle.

REFRESH. The three types of non CPU cycles are signaled by the MHLDA signal. When this signal goes active, the meaning of the status lines from the system board is changed. As a result, the memory board operates differently.

The status line which controls the actual memory cycle is (M-IO). Since this line is completely asynchronous to the CLK32 clock, synchronization is necessary to prevent metastable states and glitches which would destroy the contents of the DRAM. The M-IO line is fed through a 74F74 flip flop which is clocked by CLK32 before being sent to the D4-RCTL PAL state machine as the signal DMIO.

Refresh is determined by the state of the D-C line (refresh when low). When the state machine senses D-C low and DMIO active, MRAS* is set active. Because the address multiplexor was not switched to the row address, the column address lines are fed to the DRAM. The reason for this is that the column lines are the low order address lines from the system board, and they contain the refresh row address.

One CLK32 cycle later the SWM* signal is set active. This changes the DRAM address, but has no effect on the refresh cycle. The SWM* (and CLAT) signals are being used only as state lines to count time in the state machine.

One CLK32 cycle later the CLAT signal is set inactive and one more clock later the SWM* is set inactive. After one more clock, the MRAS* signal is set inactive giving a total time of four clocks for MRAS* active. The CLAT signal remains low until DMIO is inactive to prevent the MRAS* cycle from restarting.

DMA READ CYCLE. The DMA read cycle begins when HLDA goes active and D-C remains high. The SWM* is set active to get the row address to the DRAM and the state machine then waits for the DMIO, M32*, and W-R lines to go active signaling a DMA cycle. When this occurs, the MRAS* goes active to strobe in the row addresses. One clock later, SWM* goes inactive to set up the column addresses to the DRAM. After one more clock, MCAS* goes active and the data begins to come out of the DRAM.

On the next clock, the CLAT signal goes inactive and on the next clock MRAS* goes inactive. This leaves MRAS* active for four CLK32 cycles. The CLAT signal will remain inactive (low) and the MCAS* will remain active until DMIO goes inactive. Holding MRD* and MCAS* active insures that the data will remain until the DMA device needs it.

DMA WRITE CYCLE. The DMA write cycle begins when HLDA goes active and D-C remains high. The SWM* is set active to get the row address to the DRAM and the state machine then waits for the DMIO, M32*, and W-R lines to go active signaling a DMA cycle. When this occurs, the MRAS* goes active to strobe in the row addresses. One clock later, SWM* goes inactive to set up the column addresses to the DRAM. After one more clock, MCAS* goes active and the data is written to the DRAM.

On the next clock, the CLAT signal goes inactive and on the next clock MRAS* goes inactive. This leaves MRAS* active for four CLK32 cycles. On the following clock, the MCAS* signal goes inactive to terminate the write cycle. The CLAT signal will remain inactive (low) until after DMIO goes inactive to prevent the cycle from repeating.

ALL DMA CYCLES. On all of the above DMA cycles, SWM* will go active whenever the HOLDA and D-C lines are high. To prevent interference with the CPU cycles at the end of the hold state, the NAM* line is used as a state memory of the hold state. NAM* goes active one clock cycle after SWM* goes active (during HOLDA) and remains active until HOLDA goes inactive. The CPU portion of the state machine will do nothing unusual until both NAM* and SWM* go inactive.

TIMING ANALYSIS FOR PAGE DRAM BOARD

M32* setup to CLK32 for cycle start.

2 x CLK32	62.5
CPU address delay	- 40.0
D4-RM32 PAL delay	- 12.0
D4-RCTL PAL setup	- 10.0
MARGIN **********	+ 0.5

HIT* setup to CLK32 for cycle start.

2 x CLK32	62.5
CPU address delay	- 40.0
F521 delay	- 11.0
F32 delay	- 6.6
D4-RCTL PAL setup	- 10.0
MARGIN **********	- 5.1

NAM* output setup to CLK32 on system board.

CLK32	31.2
D4-RCTL PAL delay	- 10.0
F32 delay (sys board)	- 6.6
CPU setup (sys board)	- 10.0
MARGIN **********	4.6

Read data access from RAS*

5 x CLK32	156.2
MRAS* delay D4-RCTL	- 10.0
F32 + 33 res delay (200pF load)	- 12.0
DRAM delay from RAS	-100.0
data delay through F657	- 8.0
data setup to 386	- 10.0
MARGIN **********	+ 16.2

Read data access from CAS*

2 x CLK32	62.5
MCAS* delay D4-RCTL	- 10.0
F32 + 33 res delay (200pF load)	- 12.0
DRAM delay from CAS	- 25.0
data delay through F657	- 8.0
data setup to 386	- 10.0
MARGIN **********	- 2.5

Read data access from Column address

4 x CLK32	125.0
CLAT delay D4-RCTL	- 10.0
F573 delay	- 13.0
F158 delay	- 7.0
BUF + 33 res delay (300pF load)	- 25.0
DRAM delay from col add	- 45.0
data delay through F657	- 8.0
data setup to 386	- 10.0
MARGIN **********	+ 7.0

Parity check access from CAS*

2 x CLK32	62.5
F32 + 33 res delay (200pF load)	- 12.0
DRAM delay from CAS	- 25.0
err delay through F657	- 22.5
F00 delay	- 6.6
F175 setup	- 3.0
F32 delay MIN	+ 3.0
MARGIN **********	- 3.6

Row address setup to RAS*

1 x CLK32	31.2
F158 delay	- 9.5
BUF + 33 res delay (300pF load)	- 25.0
F32 + 33 res delay (200pF load)	+ 5.0
MARGIN **********	1.7

Column address setup to CAS*

2 x CLK32	62.5
F573 delay	- 13.0
F158 delay	- 7.0
BUF + 33 res delay (300pF load)	- 25.0
F32 + 33 res delay (200pF load)	+ 5.0
MARGIN **********	22.5

Write data setup to CAS*

3 x CLK32	93.7
MCAS* delay D4-RCTL	+ 4.0
F32 + 33 res delay (200pF load)	+ 5.0
CPU data delay	- 50.0
parity delay in F657	- 16.0
MARGIN **********	36.7

DMA Read data delay (external bus master).

286 product access from MRDC*	200
MRDC* to M-IO delay	- 15
data delay in ls245 max	- 18
4 x CLK32	-125
MCAS* delay D4-RCTL	- 10.0
F32 + 33 res delay (200pF load)	- 12.0
DRAM delay from CAS	- 25.0
data delay through F657	- 8.0
MARGIN **********	- 13.0

DMA write data setup to CAS*

4 x CLK32	125
parity delay in F657	- 16.0
System board data setup	- 61.0
MARGIN **********	48.0