SHARP SERVICE MANUAL

CODE: 00ZPC6220SM-E

PERSONAL COMPUTER

MODEL PC-6220

OPTION: CE-621NK
CE-621A
CE-621B
CE-621EV
CE-621F

CONTENTS

SHARP CORPORATION

CHAPTER 1. OUTLINE OF THE PC-6220

1-1. Features

1) Equipped with a 20MB hard disk as a standard component.

The PC-6220 is equipped with a 20MB hard disk as a standard component.

This is great enough for salesmen to store customer information and product information and for busy business men to store conference materials, reports, and other information, allowing them to be retrieved at once when needed.

2) World's lightest, thinnest (letter size) book type personal computer with HDD.

The PC-6220 is in letter size (11.0"W x 8.5"W x 1.4"H/279mm Wide x 216mm Deep), smaller than A4 size. Its thickness is only 34mm, and the volume is approx. 60% of the conventional note size personal computers with FDD. It can be put in a half side of an attache case, and even in a clutch bag. Its light weight (2kg) and the battery drive system allows easy carrying in business trip.

3) Black-and-white TST LCD with backlight

The black-and-white Triple Super Twist Liquid Crystal Display (TST LCD) with back light (side light) gives clear screen in 16 gradations, allowing to be used in a hotel room or other insufficiently illuminated place.

The screen size is greater than any other conventional note size personal computers and displays more lines of characters. (PC-6220: 640 x 480 dots)

4) MODEM, memory and other built-in options available

Built-in options are available such as a MODEM board (2400bps, class 5), CRT interface. Max. 2MB additional memory can be added (total 3MB) without extending the external dimensions.

5) The expansion units (option) provide as high a level of expansion as laptop PC's of higher class.

The combination with expansion units (option) such as a 3.5 inch FDD and expansion slot (AT spec. half and full size card), provides as high a level of expansion as laptop PC's of higher class. This allows to use a variety of PC/AT peripheral devices and to connect with a host computer, forming a LAN system.

6) System configuration

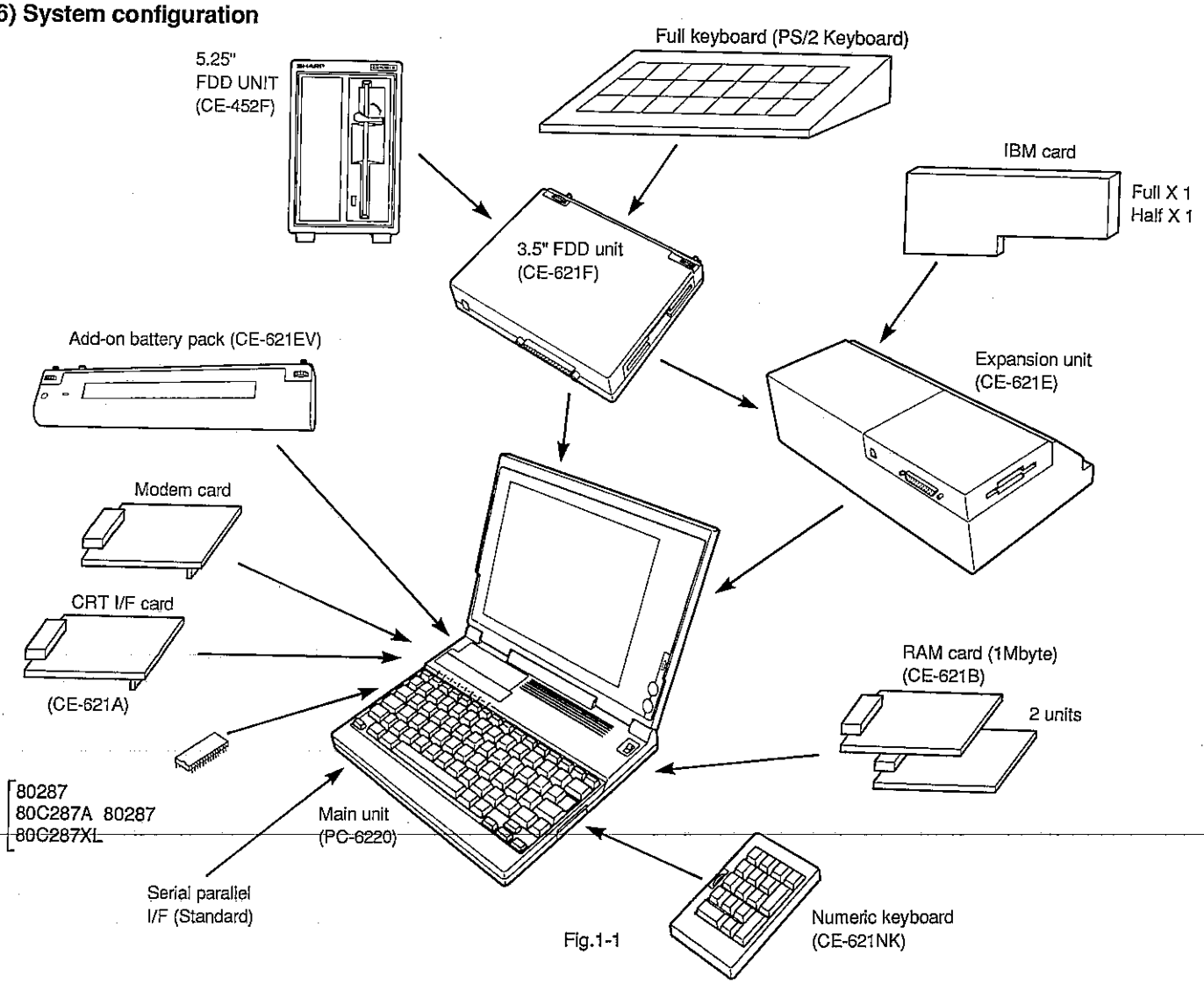


Fig.1-1

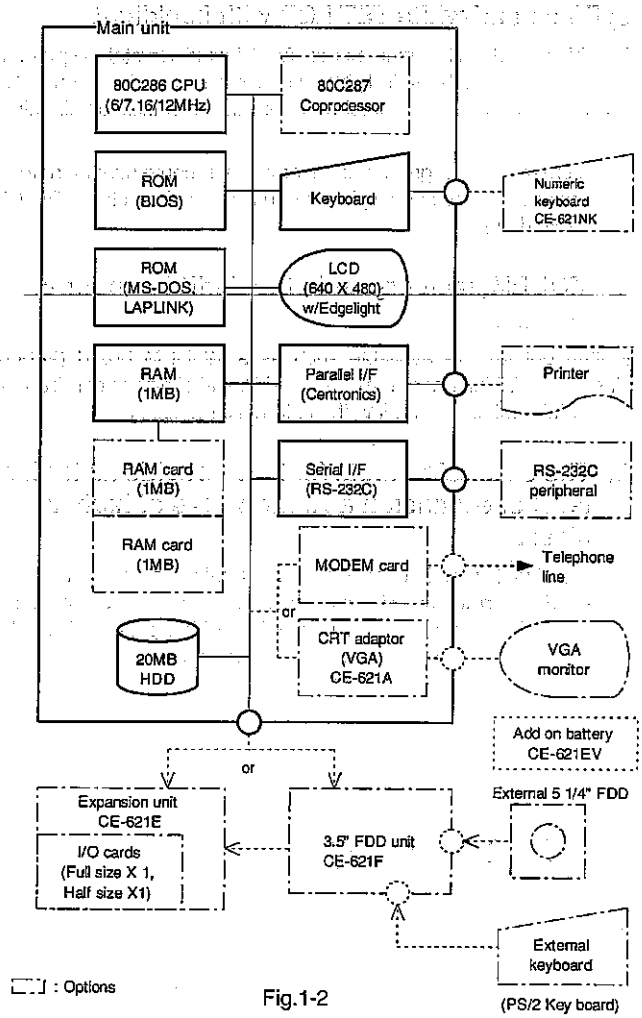


Fig.1-2

1-2. Specification

1) Hardware

CPU: 80C286 (6/7.16/12MHz)
- Clock speed can be changed in Setup screen.

CO-PROCESSOR: Socket for 80C287A, 80C287XL, 80287

ROM: 1M byte Mask ROM x 1
- Contents: IPL, Self check, Setup, AT BIOS, VGA BIOS, DOS system, Utility Software

RAM: 1M byte standard
- 1M bit PS-RAM x 8
- 640K byte for conventional, 360K byte for Expanded or Extended memory
- LIM/EMS 4.0 support
- Bus width: 16 bit
- 1 wait state (12MHz) 0 wait state (6/7.16MHz)

Expandable up to 3M byte in 1M byte increments by optional RAM card. (CE-621B)
- Two (2) RAM cards can be installed as a Maximum.

DATA STORAGE: 2.5 inch 20M byte Hard disk drive
- Average access time: 23m sec.

DISPLAY: TST (Triple Super Twisted) LCD with CCFT (Cold Cathode Fluorescent Tube) backlight
- Resolution: 640 x 480 pixels
- VGA compatible
- 16 Gradations
- Viewing area: 8" x 6"
- Aspect ratio: 1:1
- Dot pitch: 0.31 mm
- LCD contrast and backlight brightness are adjustable by each volume.
- Selectable normal/reverse screen by hardware switch.

CRT I/F (optional) (CE-621A)
- Analog RGB output
- VGA compatible
- D-sub 15 pin female connector
- Selectable LCD/CRT mode by Hardware switch.
- LCD and CRT can not be used simultaneously.
- Alternative use with MODEM card.

KEYBOARD: IBM 101/102 like keyboard layout
- 79 keys (US layout)
  80 keys (UK/German layout)
- Integrated numeric keypad
- 'Set Up' key for Setup screen
- Fn key for special function
- 12 programmable function keys
- 19mm pitch (type writer key part), 2mm stroke
- Detachable structure for installing internal options. (Co-processor, RAM cards)

INTERFACE: Serial (RS-232C) x 1
- D-sub 9 pin male connector
- Baud rate, data bits, stop bits and parity are selectable in Setup screen.

Parallel (centronics) x 1
- Specialized 26 pin connector
- With conversion adaptor to D-sub 25 pin female standard connector

Numeric keypad x 1 (CE-621NK)
- Optional Numeric keypad can be connected.

SLOT/CONNECTOR: 1 slot for internal options
- Optional MODEM card or CRT adaptor can be connected.

2 slots for RAM cards
- Optional 1M byte RAM cards can be connected.

1 Expansion connector
- Optional 3.5" FDD unit or Expansion unit can be connected.

POWER SUPPLY: Ni-Cd battery
- Rechargeable and replaceable
- 9.6 V, 11.5 WH
- 2 hours fast charging in charge mode and trickle charging while operating.

AC adaptor
- Input: 100V – 240V AC 50/60Hz
- Output: 15V DC
- AC cord is detachable from AC adaptor.

Add-on batery pack (optional) (CE-621EV)
- Rechargeable with AC adaptor for main unit.
- 3.5 hours fast charging in charge mode and tricle charging while operating.

BATTERY LIFE: Only with internal battery:
1.7H
- Hard disk access 10%, backlight midium, without options.

With internal battery and add-on battery:
4.7H
- Hard disk access 10%, backlight midium, without options.

POWER SAVE FUNCTION:

CPU:
- Standby mode

Hard disk drive:
- Spindle motor off

Backlight:
- Backlight timeout

LOW BATTERY ALARM: 1st-step:
With the battery in the normally charged state, LOW BATTERY indicator remains off.

2nd-step:
When the battery is more than roughly 90% discharged, LOW BATTERY indicator turns red and an alarm beeps for about 15 seconds.

3rd-step:
After LOW BATTERY indicator blinking and an alarm beeping for about 30 seconds, the system will shut off the power automatically.

CHARGING INDICATOR:

Main unit:
CHARGE indicator blinks while the battery is being charged, and illuminates when the battery is at least 90% charged.

Add-on battery pack:
CHARGE indicator blinks while the battery is being charged, and illuminates when the battery is at least 70% charged.

POWER CONSUMPTION:

Typ. 7 W (without options)

2) Mechanical

CONNECTORS:

External connectors for:

Serial interface:	D-sub 9 pin connector
Parallel interface:	Specialized 26 pin connector
Numeric keypad:	Specialized 10 pin connector
AC adaptor:	2 conductor phone jack
System expansion bus:	120 pin connector
Add-on battery pack:	4 pin connector

Internal connectors for:

Modem card or CRT adaptor:	68 pin connector
RAM card x 2:	50 pin connector

SWITCHES: Power switch (seesaw switch)
LCD standard/reverse screen switch 9slide switch)
LCD/CRT select switch (slide switch)
Speaker controll switch
Switch on the main PWB
BUZZER ON/OFF HIGH
BUZZER Volume swich HIGH/LOW

VOLUMES: LCD contrast adjust volume (rotary volume)
LCD brightness adjust volume (rotary volume)

LEDS: Power indicator (green or orange)
Low battery indicator (red)
Charge indicator (green)
FDD indicator (green)
HDD indicator (green)
Caps lock indicator (green)
Num lock indicator (green)
Scroll lock indicator (green)

DIMENSIONS:
8.5"(D) x 11.0"(W) x 1.4"(H)
216mm(D) x 279mm(W) x 34mm(H)

WEIGHT: 2 Kg (4.4 lbs)
(Including battery, excluding AC adaptor)

Key board Layout

a) US version

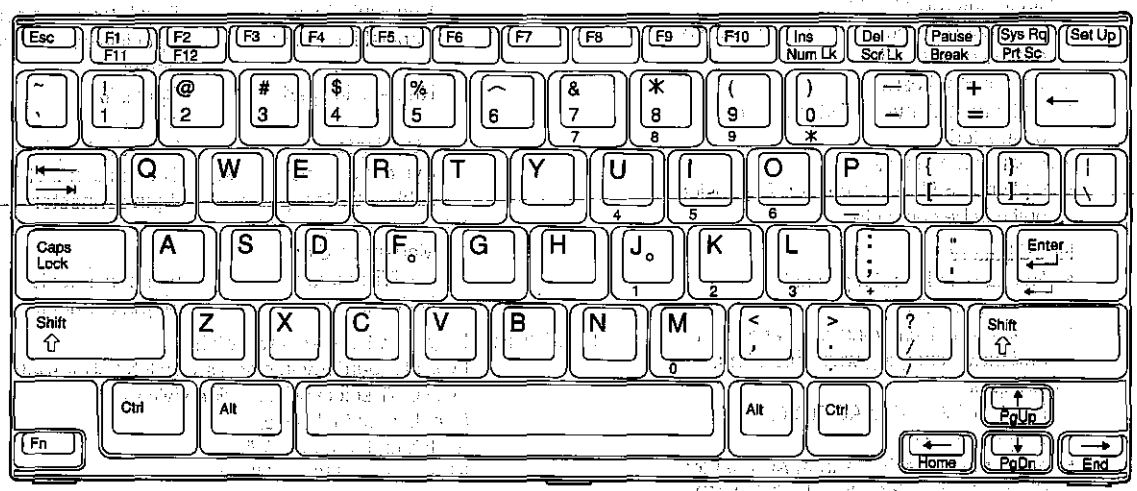


Fig.1-3

b) UK version

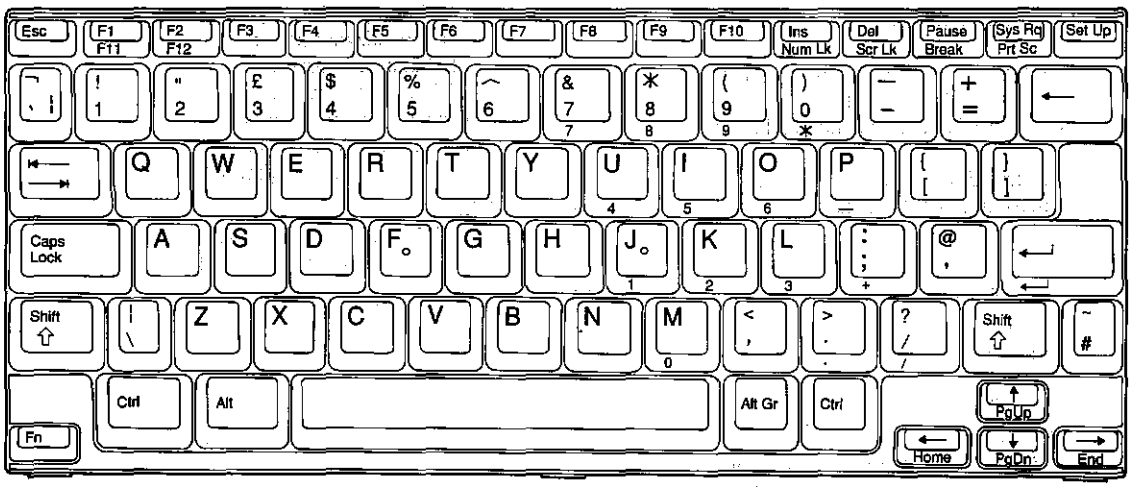


Fig.1-4

c) German version

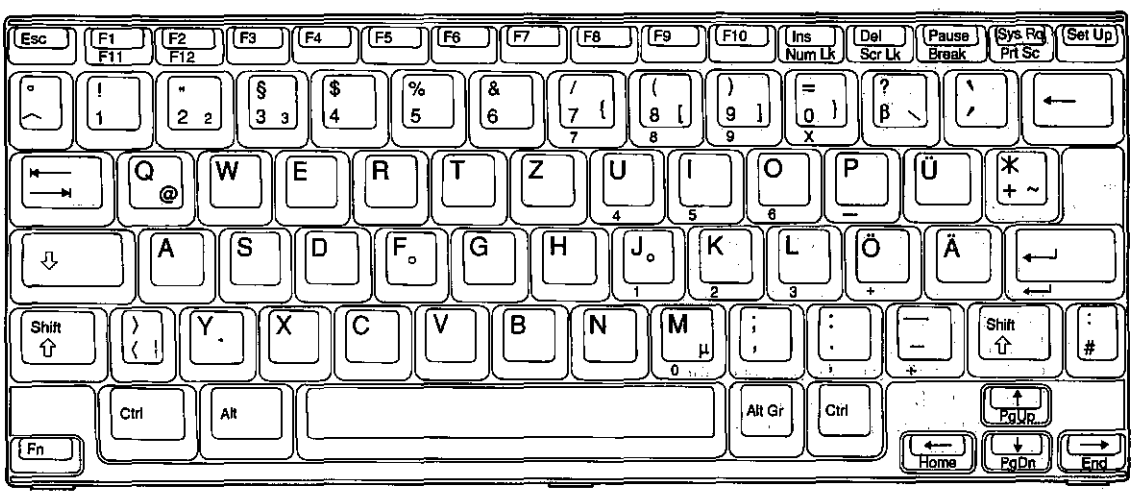


Fig.1-5

3) Software

OPERATING SYSTEM: MS-DOS 4.01
- Including SHELL 1.01
- Compressed and stored in Mask ROM
- MS-DOS must be installed into Hard Disk when initializing the system.
- Language: English

BUILT-IN SOFTWARE: LAP-LINK 2.16 self install version
- Stored in Mask ROM
- With connecting cable (To serial D-sub 9 or 25 pin connector)
- Language: English

4) Operational and storage range

Operational range:
50 to 95 degrees F
10 to 35 degrees C
20 to 80% humidity (Non-condensing)

Storage range:
–4 to 140 degrees F
–20 to 60 degrees C
10 to 90% humidity (non-condensing)

1-3. Software description

1) BIOS

The BIOS of the PC-6220 is included in a 1MBit one-time ROM.

The system BIOS and the video BIOS are stored in the ROM and attached to a separate PWB other than the main PWB.

Special function of the BIOS in PC-6220 are described below:

1-1) Power saving

The PC-6220 is equipped with three levels of power saving.

① Display power saving

② Hard disk power saving

③ System power saving

These power saving functions are performed with the time-out values set by SETUP. The system power saving can be also executed by key input. Some application software may not work correctly with system power saving function. If there are any problems in the power saving function, Please disable the function by SET_UP.

1-2) Automatic setting of hardware

The PC-6220 hardware setting is performed for the following items.

① Built-in VGA mode setting

② Display adapter setting

③ Each device I/O port setting

④ FDD/HDD assignment

⑤ Built-in memory setting

The following items are automatically detected and proper settings are made automatically.

① FDD presence

② FDD type

③ HDD type

④ Main memory and expansion memory capacity

When no FDD is connected, BIOS level emulation is performed. Then the machine works as if two FDDs are connected without disk insertion.

1-3) ROM disk

To use ROM disk, set Drive C to ROM disk in hardware installation.

With the ROM disk, only the following three items can be executed.

① MS-DOS installation

② Diag. program execution

③ Setup execution

1-4) Special functions with key operation

- SETUP key : "SET UP" 0DH character line is displayed.
- CTRL + ALT + SETUP : Setup program execution
- Fn + SETUP : Displayed pallet number change
- (Fn + PAUSE) : System power saving execution/return (CTRL + ALT + PAUSE)
- CTRL + ALT + ↑ : CPU clock UP (6 → 7.16 → 12 MHz)
- CTRL + ALT + ↓ : CPU clock down (12 → 7.16 → 6MHz)

2) Setup

2-1) Setup procedure

There are following two procedures for entering the setup mode.

① Execute SET UP command of MS DOS.

② Press CTRL + ALT + SETUP keys while the system is operating. This procedure is effected by the key interruption. When, therefore, the control exits from the setup mode, the system is rebooted.

2-2) Setup contents

◎ Clock
Time setting of the real time clock is made in Hour/Minute/Second/AM or PM and Year/Month/Day. The days of the week are automatically set.

◎ Display
This setup is made for the built-in VGA.

☆ Cursor type: Underline/Under bar/Block
Set the cursor from when booting the system or when changing the video mode.

☆ LCD mode: Standard/Expanded
Set the LCD screen displayed size when booting the system or when changing the video mode.

◎ Keyboard
This setup is made for the keyboard.

☆ NUM LOCK: ON/OFF
NUM LOCK state at booting is set.

☆ CAPS LOCK: ON/OFF
CAPS LOCK state at booting is set.

☆ SCROLL LOCK: ON/OFF
SCROLL LOCK at booting is set.

☆ Repeat rate: Standard/Fast
Keyboard repeat rate at booting and after setup is set.

◎ Serial I/O
Serial I/O at booting and after setup is set.

☆ Internal SIO
Baud rate: 9600 – 110
Data bits: 8/7
Stop bits: 2/1
Parity bits: None/Odd/Even
Various settings of built-in SIO are performed.

☆ Optional SIO
Baud rate: 9600 – 110
Data bits: 8/7
Stop bits: 2/1
Parity bits: None/Odd/Even
Optional SIO (Modem card) settings are performed.

◎ Power saving
The following power saving functions are set.

☆ Display timeout: 1 – 10 minutes/Always ON
When the keyboard has not been pressed and no disk drives have not been accessed for the specified period, the display unit goes into the low power mode.

☆ System timeout: 1 – 10 minutes/Always ON
When the keyboard has not been pressed and no disk drives have not been accessed for the specified period, the system is temporarily stopped goes into the standby mode.
The power consumption in system timeout is lower than display timeout.

☆ HDD timeout: 30 sec – 10 minutes/Always ON
When the hard disk has not been accessed for the specified period, the hard disk motor is stopped to cut power consumption.

◎ System configuration
System settings are performed.

☆ QUICK BOOT: ON/OFF
Memory check and other time-consuming checks are skipped and only minimum system checks are made for quick boot of the system.

☆ SPEED KEY : ENABLE/DISABLE
Used to set enable/disable of changing the CPU speed by the keyboard operation.

☆ STANDBY KEY: ENABLE/DISABLE
Used to set enable/disable of transition to the system power saving mode by the keyboard operation.

☆ CPU SPEED: 12/7.16/6 MHz
Used to set the CPU clock speed at booting and after setup. Since AT bus clock is also changed at this setting, the bus clock is also displayed.

Setup default parameters

SHARP PERSONAL COMPUTER SET-UP
PROGRAM

Clock		Power Saving		Serial I/O	
Time: 2:07:06 p.m.		Display Timeout:	1 minute	Standard SIO	
Date: TUE MAY 08, 1990		HDD Motor Off:	1 minute	Baud Rate:	9600
		System Timeout:	Always ON	Data Bits:	8
Display				Stop Bits:	1
		System Configurations		Parity:	None
Cursor Type:	Underline				
LCD Mode:	Standard	CPU Speed:	12MHz	Optional SIO	
		BUS Speed:	6MHz	Baud Rate:	9600
Keyboard		Quick Boot:	On	Data Bits:	8
		Standby Key:	Enable	Stop bits:	1
Caps Lock:	Off	Speed Key:	Enable	Parity:	None
Num Lock:	Off				
Scroll Lock:	Off				
Repeat Rate:	Fast				

1. Position Cursor using cursor keypad 2. Press Space Bar to change 3. Press Set-Up Key to exit

3) Hardware installation

3-1) Hardware installation procedure

There are three procedures for hardware installation.

① Perform hardware installation during user diagnosis.

② Press ENTER key when "Invalid Configuration Information" error, etc. occurs.

③ Press CTRL + ALT + SET UP keys during setup operation.

3-2. Hardware installation

◎ Display configuration

☆ Display mode: VGA/EGA/CGA/MDA/HGC
Used to set built-in VGA.

☆ Display adaptor: Internal VGA/CGA80/CGA40/MDA/Others
Used to set the display adaptor state when the expansion box is connected. By this setting, the display adaptor can be used instead of the built-in VGA when the built-in VGA is not used and the expansion box is connected.
If the expansion box is not connected, the built-in VGA is used regardless of this setting.

◎ Drive assignment

☆ Drive A: Optional 3.5"FDD External 5.25"FDD

☆ Drive B: External 5.25FDD" Optional 3.5"FDD
Used to set FDD assignment. When the expansion FDD is not connected, the option FDD is assigned to Drive A regardless of this setting.

☆ Drive C: Internal HDD ROM disk

☆ Drive D: None Internal HDD
Used to set the internal HDD and ROM disk assignment and to set the booting drive assignment when FD is not inserted.

◎ I/O configuration

Used to set hardware I/O port.

☆ Parallel Port: PORT1/PORT2/DISABLE
Used to set port address of the internal parallel port.

☆ Internal SIO Port: PORT1/PORT2/DISABLE

☆ Optional SIO Port: PORT1/PORT2/DISABLE
Used to set SIO port address.

☆ ROM disk I/O port: 1?8H ~ 1?BH (?: 0 ~ F)
Used to set I/O port address used by the ROM disk.
ROM disk port address is effective even though ROM disk is set to NONE.
ROM disk I/O port address may be changed to prevent butting when a card is inserted into the expansion box.

☆ EMS I/O port: 2?8H ~ 2?BH (?: either of 0, 1, 4, 5, 6, A, B, E)
EMS I/O port is effective even though EMS is not used.
EMS port address may be changed to prevent butting when a card is inserted into the expansion box.

◎ Memory configuration

For memory setting, commercially available memory can be used for the expansion box. Therefore, the user must register the size of internal memory connected currently.

☆ Internal memory size: XX MB 1 ~ 3MB
The user must register the total size of Sharp memory.
Each memory capacity is assigned and displayed according to this total memory.

☆ Boundary address: XXXXXXXH
Used to set boundary of releasing memory address to the expansion box. According to this value, the sizes of 1Mb memory and EMS memory are determined.

☆ With the above items, the following items are displayed.

◎ Main memory : 640KB
Main memory capacity is displayed. It is fixed to 640KB.

◎ Extended memory: XXXXXX KB (XX.X MB)
The memory capacity over 1MB is displayed. Memory in the expansion box is not displayed. Only Sharp memory is displayed.

◎ Expanded memory: XXXXXX KB (XX.X MB)
EMS memory capacity is displayed. Memory in the expansion box is not displayed. Only Sharp memory is displayed.

◎ Disabled memory: XXXXX KB
Depending on the memory boundary set value, 256KB memory may be disabled.

4) Others

4-1) Default values of hardware installation and setup

To reset parameters of hardware installation and setup to the default values, press CTRL + SPACE keys. Then the displayed parameters will be reset to their default values. To reset all the parameters, press CTRL + SPACE keys for each of hardware installation and setup screens. Data and Time, however, will not be reset to the default values.

4-2) Starting ROM disk

Press CTRL + ALT + SETUP keys and perform setup. While setup is executed, press CTRL + ALT + SETUP keys again, the set goes into hardware installation.

Then set drive C to ROM disk, and drive D to hard disk, and start the set again.

4-3) When the screen is not clear on starting

The PC-6220 stores the pallet value on power off. Therefore, some pallet value setting just before power off may result in unclear screen. In this case, press Fn + SETUP.

1-4. BIOS POST (Power On Self Test) check

Error detection and report

When the system is started, BIOS POST program is executed.

In POST, operations of the system RAM interruption and various devices including peripheral devices are checked. The operation checks are classified into two groups according to error report.

1) Error report by I/O port 80h (MFG port) and beep sound

2) Error report by message displayed on the screen

For the tests which use the I/O port 80h (MFG port) and beep sounds, the test items and the output data to the port 80h are shown in the following table.

For the test item with "NONE" in the column of Beep sound, the system does not stop. For the other test items, when any error occurs, beep sound is generated and the system is stopped.

(Note) Figures in the column of beep sound shows the number of beep. For example, "1-3-4" shows "1 beep sound, pause, 3 beep sounds, pause, and 4 beep sound."

Test items	PORT 80h	Beep sound
CPU register test	01h	None
RTC RAM read/write test	02h	1-1-3
BIOS ROM check sum test	03h	1-1-4
System timer (8254) test	04h	1-2-1
DMAC initializing test	05h	1-2-2
DMA page register test	06h	1-2-3
RAM refresh test	08h	1-3-1
First 64KB system RAM test start	09h	None
First 64KB RAM plural data lines error	0Ah	1-1-1
First 64KB RAM control logic error	0Bh	1-3-4
First 64KB RAM address line error	0Ch	1-4-1
First 64KB RAM parity test	0Dh	1-4-2
First 64KB RAM data line error (BIT0)	10h	2-1-1
First 64KB RAM data line error (BIT1)	11h	2-1-2
First 64KB RAM data line error (BIT2)	12h	2-1-3
First 64KB RAM data line error (BIT3)	13h	2-1-4
First 64KB RAM data line error (BIT4)	14h	2-2-1
First 64KB RAM data line error (BIT5)	15h	2-2-2
First 64KB RAM data line error (BIT6)	16h	2-2-3
First 64KB RAM data line error (BIT7)	17h	2-2-4
First 64KB RAM data line error (BIT8)	18h	2-3-1
First 64KB RAM data line error (BIT9)	19h	2-3-2
First 64KB RAM data line error (BITA)	1Ah	2-3-3
First 64KB RAM data line error (BITB)	1Bh	2-3-4
First 64KB RAM data line error (BITC)	1Ch	2-4-1
First 64KB RAM data line error (BITD)	1Dh	2-4-2
First 64KB RAM data line error (BITE)	1Eh	2-4-3
First 64KB RAM data line error (BITF)	1Fh	2-4-4
Slave DMAC register test	20h	3-1-1
Master DMAC register test	21h	3-1-2
Master interrupt mask register test	22h	3-1-3
Slave interrupt mask register test	23h	3-1-4
Interrupt vector setting	25h	None
Keyboard controller test	27h	3-2-4
RTC RAM power check sum test	28h	None
RTC RAM content validation test	29h	None
Display memory (VRAM) test	2Bh	3-3-4
Display initialization test	2Ch	3-4-1
Display line signal test	2Dh	3-4-2
Display ROM searching	2Eh	None
Display test complete	30h	None
Monochrome display allowed to use	31h	None
Color display (40 columns) allowed to use	32h	None
Color display (80 columns) allowed to use	33h	None

Hardware installation

SHARP PERFONAL COMPUTER HARDWARE INSTALLATION

Display Configuration		Drive Assignment	
Display Mode:	VGA Mode	Drive A:	External 3.5" FDD
Display Adaptor:	Internal VGA	Drive B:	External 5.25" FDD
		Drive C:	Internal HDD
		Drive D:	None
I/O Configuration		**Memory Configuration**	
Internal Serial Port:	Port 1	Internal memory Size:	1 MB
Optional Serial Port:	Port 2	Boundary Address:	110000h
Internal Parallel Port:	Port 1		
		* Main Memory:	640 KB
ROM Disk I/O Port:	1C8h-1CBh	* Extended Memory:	64 KB
EMS I/O Port:	218h-21Bh	* Expanded Memory:	320 KB
		* Disabled memory:	0 KB

1. Position Cursor using cursor keypad 2. Press Space Bar 3. Press Set-Up Key to exit

Fig. 1-7

CHAPTER 2. Disassembly and assembly

2-1. Precautions

Before disassembly, remove the AC adaptor and the built-in Ni + cad battery. A precise screwdriver is required for disassembly.

Since some screws and component parts are very small, tidy up the work table and be sure not to lose the components.

2-2. Keyboard section

Disassembly

1) With the LCD section closed, remove the two black screws at the bottom. (Fig. 2-1) (Screw: a)
2) Open the LCD section, pull the function keys side of the keyboard towards you, unlock the connector of keyboard on the main P.W.B. keyboard and remove the FPC.

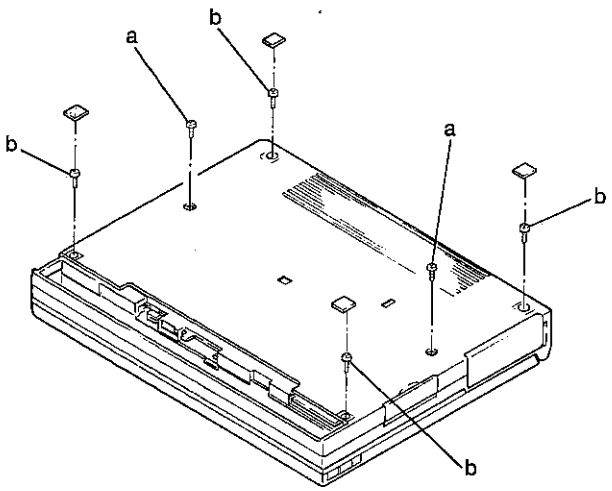


Fig. 2-1

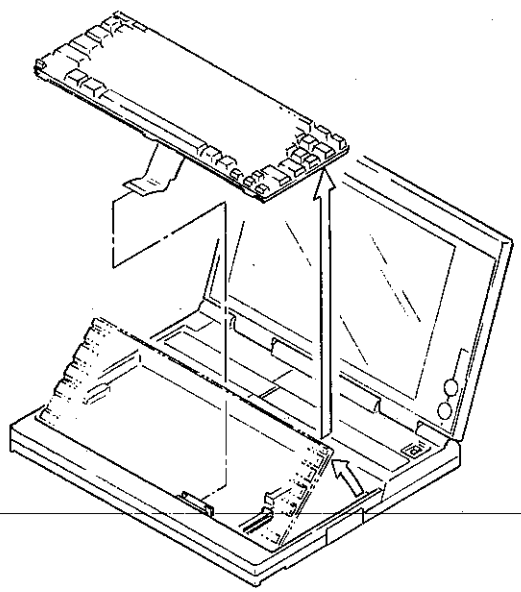


Fig. 2-2

Assembly

1) Attach the keyboard to the set by reversing the disassembly procedure. Be sure to fully insert the FPC cable of the keyboard and lock the connector.

2-3. Upper/lower cabinet disassembly

Disassembly

1) Remove the keyboard according to procedure 2-2.
2) Remove screw which are fixing the upper cabinet and the main PWB. (Fig. 2-3) (Screw: c)

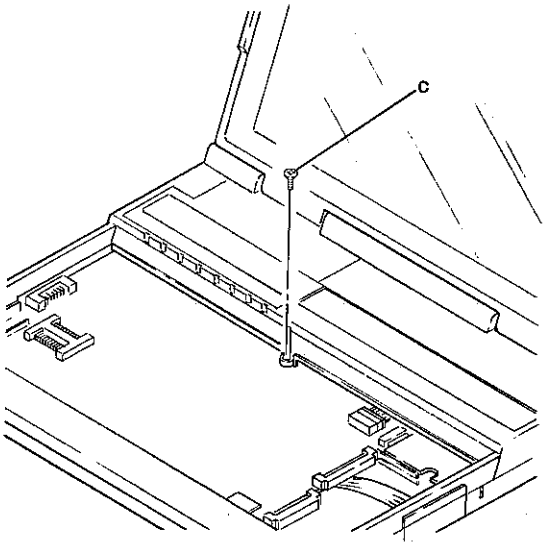


Fig. 2-3

3) Remove the connector covers. (4 covers: Key pad, battery, expansion bus, parallel)
   Keep the RS-232C cover open.
4) Close the LCD section and place the set upside down.
5) Remove the four rubber cushions fixed to the bottom by duplex tape. Then remove the four screws which are fixing the lower cabinet and the upper cabinet. (Fig. 2-1) (Screw: b)
6) Remove the screw at the back. (Fig. 2-4)

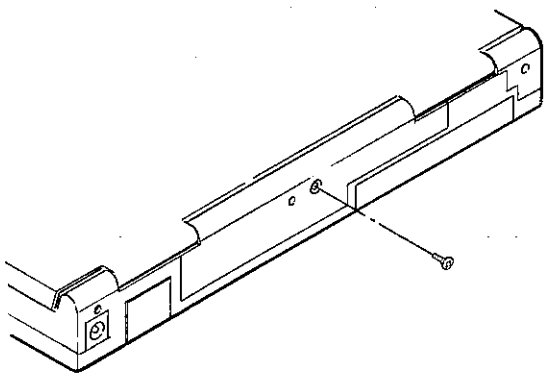


Fig. 2-4

7) Remove the engagement section of the upper and lower cabinets. Since the upper and lower cabinets are connected with LCD cables, etc., place the set as shown in Fig. 2-5 and remove the connectors.

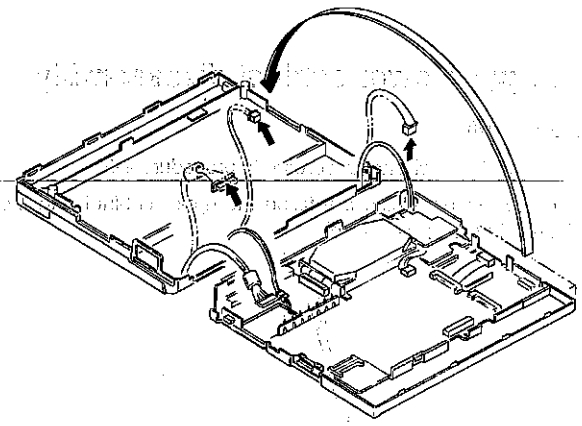


Fig. 2-5

Assembly

1) Assemble the upper and lower cabinets by reversing the disassembly procedures.
2) Attach the keyboard to the set.

2-4. Hard disk replacement

Since the hard disk is a precision device, be careful handling it. Especially when it is removed from the set, it is easily susceptible to electrostatics and vibrations.

Disassembly

1) Remove the keyboard.
2) Separate the upper cabinet from the lower cabinet.
3) Remove the three screws (H) which are fixing the hard disk unit.

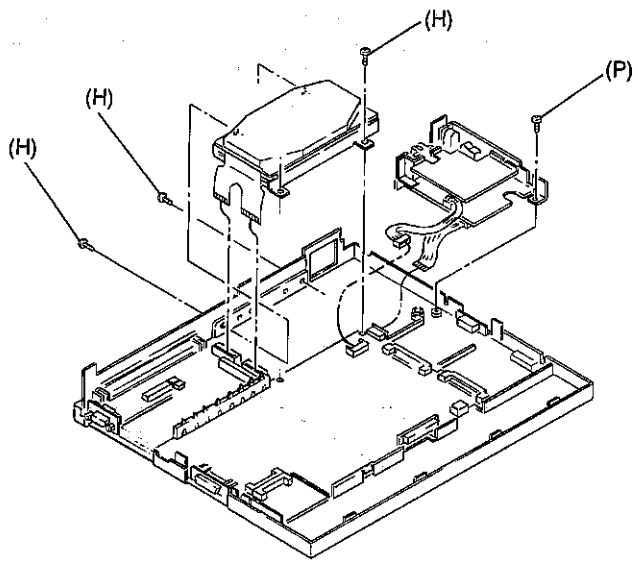


Fig. 2-6

4) Unlock the connector of hard disk on the main P.W.B. and carefully remove the FPC.
Handle the power cable with care. If disassembly is difficult because of the power cable, remove the power unit and disassemble.

Installation

1) Install the hard disk by reversing the disassembly procedure.
2) The fixing screw of the hard disk may be easily damaged by excessive tightening. So, slowly turn it until it stops and carefully tighten it.
3) Attach the upper and lower cabinets to the set.
4) Attach the keyboard to the set.

2-5. Power unit

Disassembly

1) Remove the keyboard.
2) Separate the upper cabinet from the lower cabinet.
3) Remove the screw (P) which is fixing the power unit, then remove the power unit.
Remove the two connectors. (Fig. 2-6)
When it is difficult to remove the connectors, remove the hard disk first.

Installation

1) Install the power unit by reversing the disassembly procedure.
2) Attach the upper and lower cabinet to the set.
3) Attach the keyboard to the set.

2-6. Main PWB

Disassembly

1) Remove the keyboard.
2) Separate the upper cabinet from the lower cabinet.
3) Remove the hard disk unit and the power unit.
4) Remove the ROM PWB.
5) Remove the buzzer connector.
6) Remove the four screws (M).

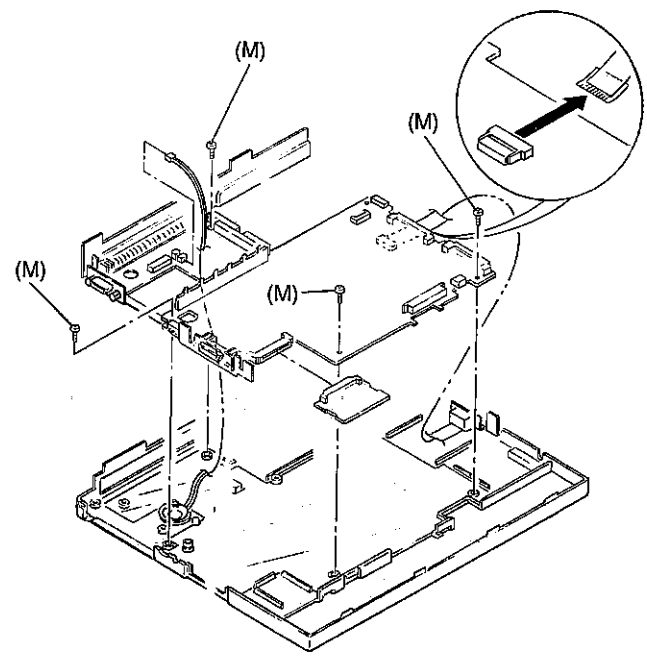


Fig. 2-7

7) With the main PWB hanging in the air, unlock the connector of the key pad on the soldering surface of the PWB, and remove the FPC.

Note: When treating the main PWB, be careful to electrostatics. When soldering is performed, be sure to clean and remove soldering dust from the PWB surface. Then install the PWB.

Installation

1) Install the PWB by reversing the disassembly procedure.
The fixing screw of the lower cabinet may be easily damaged by excessive tightening. So, slowly turn it until it stops and carefully tighten it.
2) Install the hard disk unit and the power unit.
3) Attach the ROM PWB.
4) Attach the upper and lower cabinets.
5) Attach the keyboard to the set.

2-7. LCD section and upper cabinet

Disassembly

<Caution>
For disassembly of the LCD unit, be sure to follow the procedure below. If not, the cabinet may be damaged.

1) Remove the keyboard. (See procedure 2-2.)
2) Separate the upper cabinet from the lower cabinet. (See procedure 2-3.)
3) Remove the four screws which are fixing the tilt mechanism.

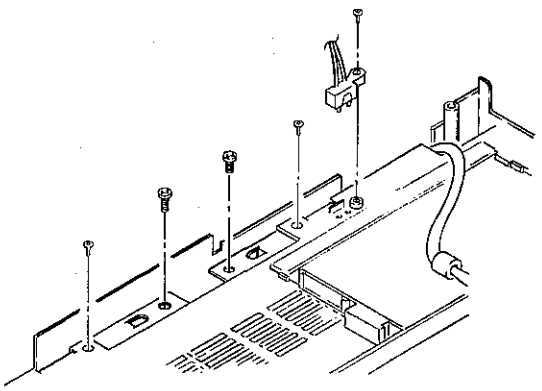


Fig. 2-8

4) Move a tilt mechanism to the center with a screwdriver, and remove it upwards.
Then remove the other tilt mechanism in the same manner.

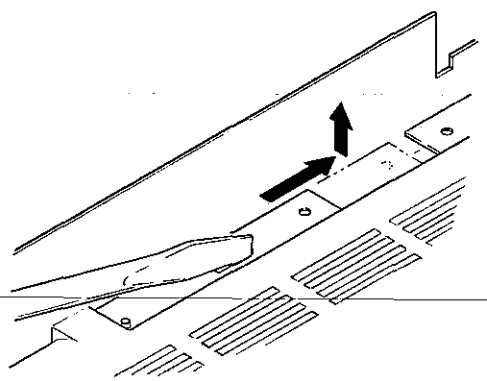


Fig. 2-9

5) Operate the LCD release lever, unfix the upper cabinet and the LCD section, and separate the upper cabinet from the LCD section.
In this case, be careful not to damage two LCD cables. Though this procedure can be performed without removing the open sensor switch in the LCD section, it is advisable to remove it in advance to protect the cable from being damaged.

Installation

1) Install the upper cabinet and the LCD section by reversing the disassembly procedure.
When installing the tilt mechanism, set the shaft horizontally in parallel to the angle bottom and insert into the LCD section. (Fig. 2-10)

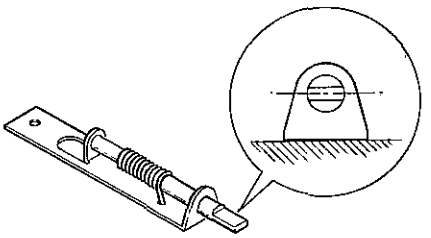


Fig.2-10

2) Attach the upper and lower cabinets to the set.
3) Attach the keyboard to the set.

2-8. LCD section

Disassembly

<Caution>
For disassembly of the LCD unit, be sure to follow the procedure below. If not, the cabinet may be damaged.

1) Remove the keyboard. (See procedure 2-2.)
2) Separate the upper cabinet from the lower cabinet. (See procedure 2-3.)
3) Remove the upper cabinet. (See procedure 2-7.)
4) Remove the four rubber cushions fixed with duplex tape on the LCD section, and remove the four screws which were covered by the four rubber cushions. (Fig. 2-11)

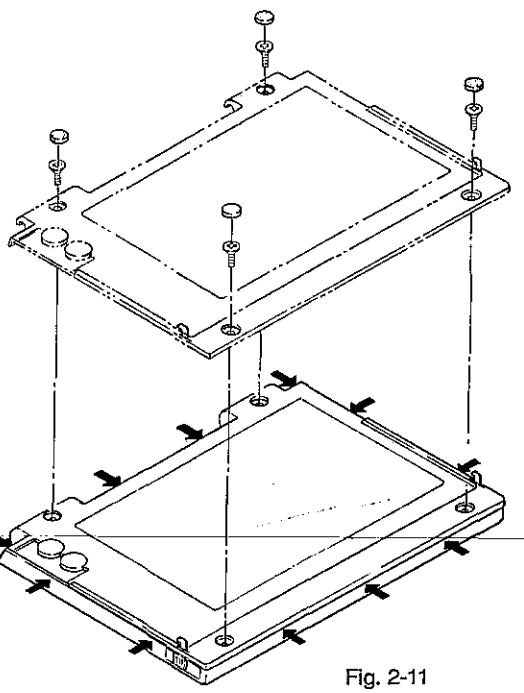


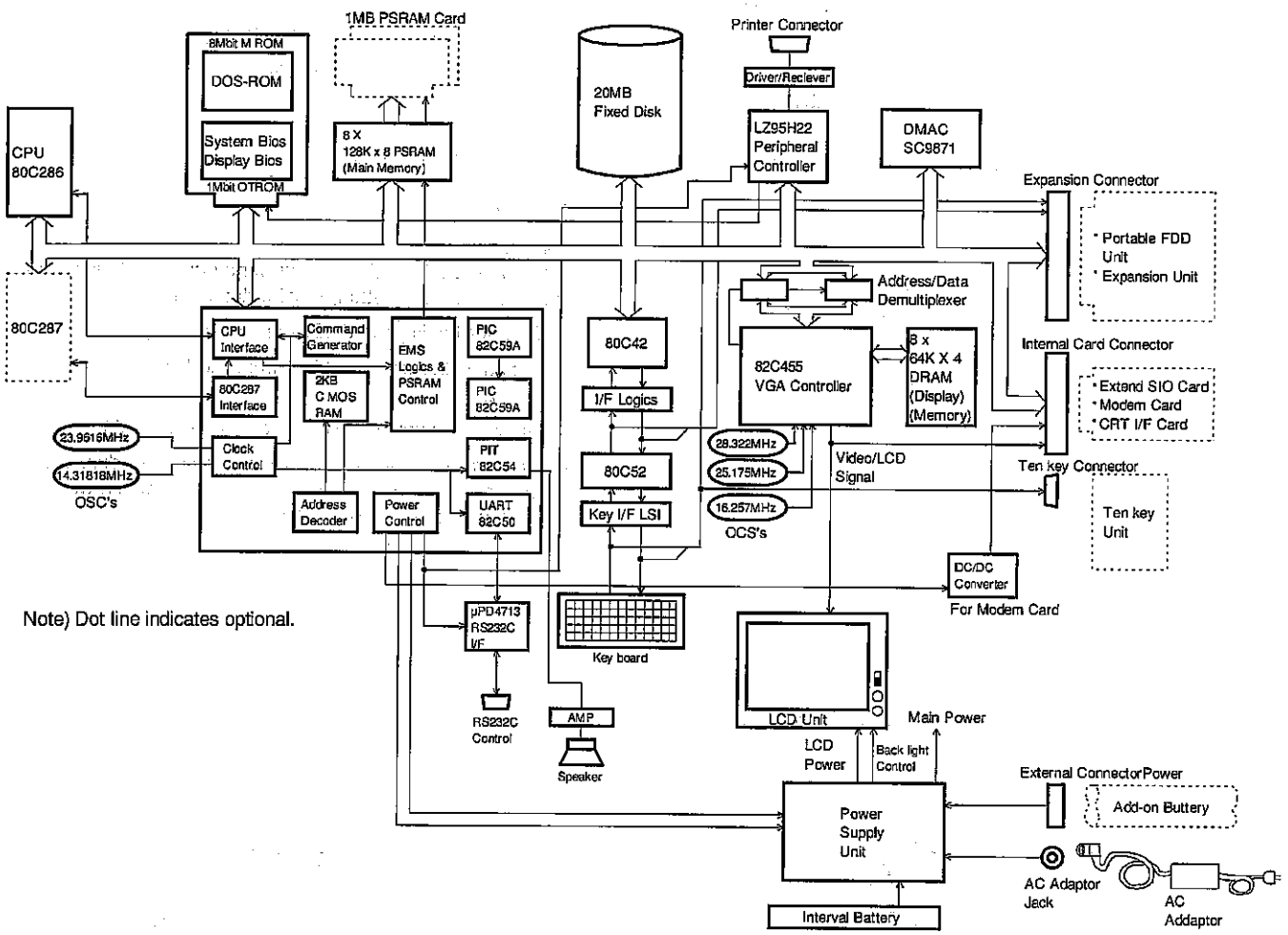
Fig. 2-11

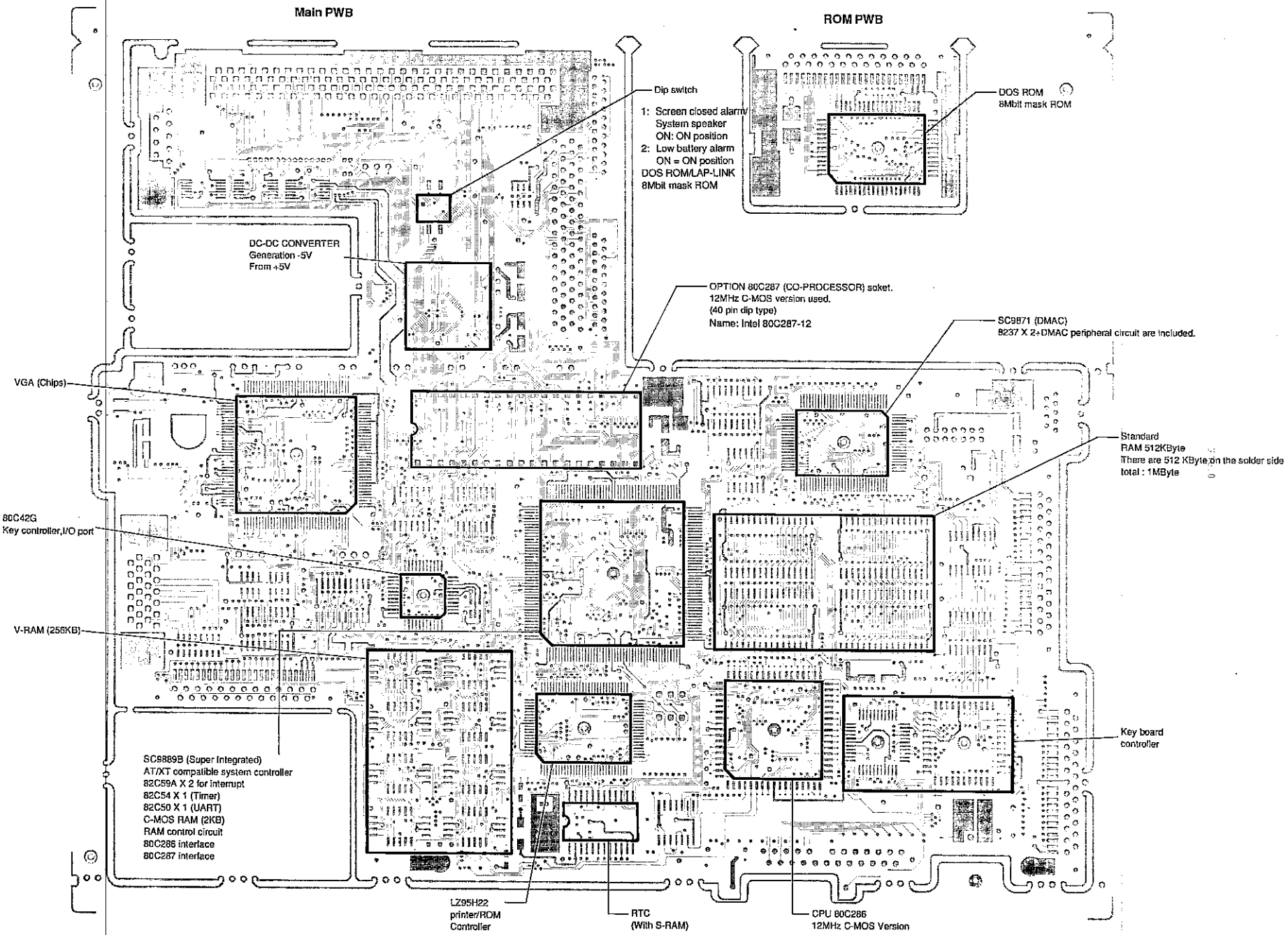
5) Remove the front and rear cabinets of the LCD section. The pawl which is fixing the cabinets is shown with (⬅) in Fig. 2-11.
6) Remove the fixture which fixes the LCD section and the body.
7) Remove the reflection plate of the backlight.
8) Remove the fixing screws and the connectors of the illumination control PWB and the backlight convertor PWB, and remove the PWB's.

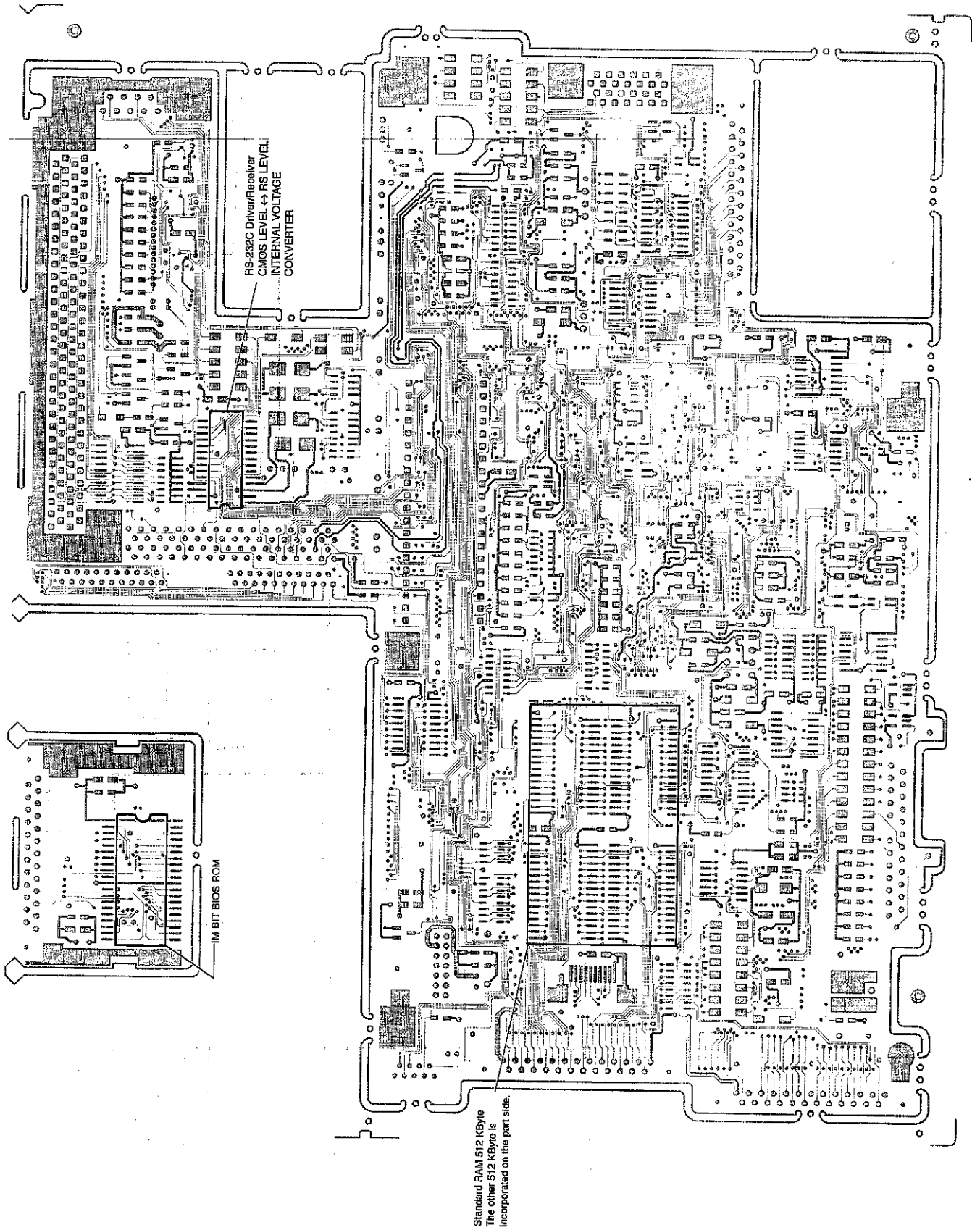
Assembly

1) Assemble the LCD unit by reversing the disassembly procedure. Carefully check that there is no fingerprint on the LCD section. If there is, clean with a cloth and alcohol. The cloth must be fine and smooth, such as glass wiper cloth.
2) Attach the upper cabinet to the set.
3) Attach the lower cabinet to the set.
4) Attach the keyboard to the set.

CHAPTER 3. System block diagram




Main PWB
ROM PWB
Dip switch
1: Screen closed alarm
System speaker
ON: ON position
2: Low battery alarm
ON = ON position
DOS ROM/LAP-LINK
8Mbit mask ROM
DOS ROM
8Mbit mask ROM
DC-DC CONVERTER
Generation -5V
From +5V
OPTION 80C287 (CO-PROCESSOR) soket.
12MHz C-MOS version used.
(40 pin dip type)
Name: Intel 80C287-12
SC9871 (DMAC)
8237 X 2+DMAC peripheral circuit are included.
VGA (Chips)
Standard
RAM 512KByte
There are 512 KByte on the solder side
total : 1MByte
80C42G
Key controller,I/O port
V-RAM (256KB)
Key board
controller
SC9889B (Super Integrated)
AT/XT compatible system controller
82C59A X 2 for interrupt
82C54 X 1 (Timer)
82C50 X 1 (UART)
C-MOS RAM (2KB)
RAM control circuit
80C286 interface
80C287 interface
LZ95H22
printer/ROM
Controller
RTC
(With S-RAM)
CPU 80C286
12MHz C-MOS Version


RS-232C Driver/Receiver
CMOS LEVEL ↔ RS LEVEL
INTERNAL VOLTAGE
CONVERTER
1M BIT BIOS ROM
Standard RAM 512 KByte
The other 512 KByte is
incorporated on the part side.

CHAPTER 4. Theory of operation

4-1. Processor

4-1-1. CPU

This unit employs 12MHz version of 80C286 as the CPU, which operates at three speeds: 6MHz, 7.16MHz, and 12MHz. Its selection is possible at any time by writing into the port by the program.

One period from falling to next falling of a clock which is inputted to the CPU is called as "phase." There are two phases: phase 1 (ϕ1) and phase 2 (ϕ2). The CPU recognizes the next phase to the rising of a reset signal as phase ϕ2, and repeats phase 1 and phase 2 alternately until the reset signal rises again.

The combination of ϕ1 and ϕ2 is called as "state." There are four states: status state (Ts), command state (Tc), idle state (Ti), and hold state (Th). Ts shows the cycle where the CPU is trying to make status signal (*S0, *S1) active. Tc shows the cycle where command signals (*MEMW, *MEMR, *IOW, *IOR, *INTA) are made active to perform data transmission. (The signals, however, are not always made active.) When the CPU make access to a device, a continuous state composed of one Ts called cycle and one or more Tc's. One cycle is executed by repeating the following steps.

① First, the CPU generates address.

② Then the CPU generates status signal which shows the cycle to be executed. (TS)

③ The system control LSI (SC9889A/B) decodes address and status and outputs the necessary control signals (command signal, select signal of memory and each device). (TC)

④ The SC9889B controls each buffer according to data transmission direction, and transmits data from the CPU/device to the device/CPU. (Tc)

⑤ After completion of transmission, the SC9889B returns the ready signal to the CPU and completes the cycle. (The last Tc)

Fig. 4-1 shows the outline of the cycle.

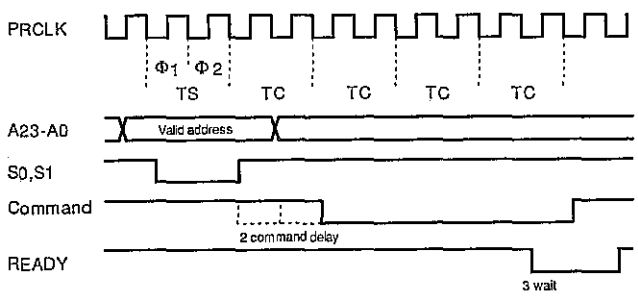


Fig. 4-1

• 80C286 Description

Features

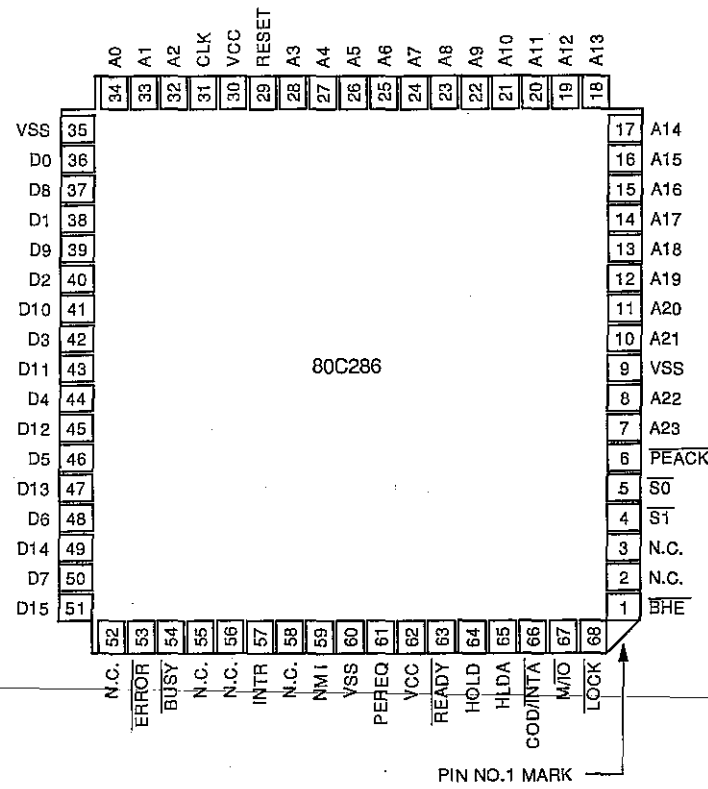
- Compatible with NMOS 80286
- Static CMOS Design for Low Power Operation
  - ▶ ICCSB = 5mA Maximum
  - ▶ ICCOP = 220mA Maximum (80C286-12)
- High Performance Processor (Up to 12 Times the 8086 Throughput)
- Large Address Space:
  - ▶ 16 Megabytes Physical
  - ▶ 1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two 80C86 Upward Compatible Operating Modes:
  - ▶ 80C286 Real Address Mode
  - ▶ Protected Virtual Address Mode
- Compatible with 80287 Numeric Data Co-processor
- Wide Range of Clock Rates:
  - ▶ DC to 12.5MHz (80C286-12)
- High Bandwidth Bus Interface (16 Megabyte/Sec)
- Available in 68 Pin PGA (Pin Grid Array) and PLCC (Plastic Leaded Chip carrier) Packages

Description

The Harris 80C286 is a static CMOS version of the NMOS 80286 microprocessor. The 80C286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 12.5MHz 80C286 provides nine times or more throughput than the standard 5MHz 8086. The 80C286 includes memory management capabilities that map 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286 is upwardly compatible with 80C86 and 80C88 software (the 80C286 instruction set is a suparset of the 30C86/80C88 instruction set). Using the 80C286 real address mode, the 80C286 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286's integrated memory management and protection mechanism. Both modes operate at full 80C286 performance and execute a superset of the 80C86 and 80C88 instructions.

The 80C286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80C286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.



Top view

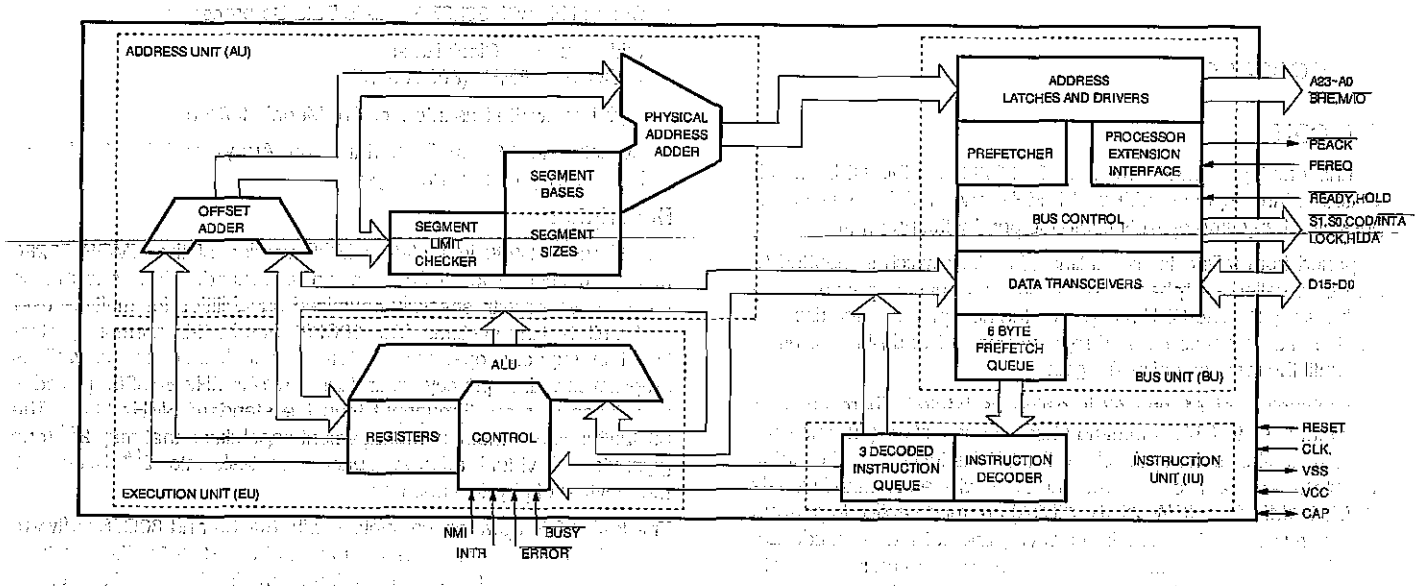


Table 4-1 80C286 Pin description

Signal	Pin No.	I/O	Name and Function
Vcc	30, 62	I	System power: +5V power supply.
Vss	9, 35, 60	I	System ground: 0V
RESET	29	I	System Reset clears the internal logic of the 80C286 and is active HIGH. The CPU may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET remains active, the output pins of the CPU enter the state shown below: 80C286 Pin State During Reset Pin Value: 1 (HIGH) — Pin Names: $\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A23 – A0, $\overline{BHE}$, LOCK Pin Value: 0 (LOW) — Pin Names: M/$\overline{IO}$, COD/$\overline{INTA}$, HLDA Pin Value: 3-state OFF — Pin Names: D15 – D0 Operation of the 80C286 begins after a HIGH to LOW transition of RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the CPU for internal initializations before the first bus cycle to fetch a code from the power-on execution address is performed. A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.
CLK	31	I	System Clock provides the fundamental timing for 80L286 systems. It is divided by two inside the CPU to generate the processor clock. The internal divide-by two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D15-D0	51 – 36	I/O	Data Bus inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
A23-A0	7, 8, 10 – 28 32 – 34	O	Address bus outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred pins D7-D0. A23-A16 are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
$\overline{BHE}$	1	O	Bus High Enable indicates transfer of data on the upper bytes of the data bus, D15-D8. Eight-bit oriented devices assigned to the upper bytes of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active LOW and floats to 3-state OFF during bus hold acknowledge. $\overline{BHE}$ and A0 Encodings $\overline{BHE}$ Valu / A0 Value / Fuaction L / L / Word transfer L / H / Byte transfer on upper half of data bus (D15 – D8) H / L / Byte transfer on lower half of data bus (D7 – D0) H / H / Reserved

<table>
<tr><th>Signal</th><th>Pin No.</th><th>I/O</th><th>Name and Function</th></tr>
<tr><td>$\overline{S1}$, $\overline{S0}$</td><td>4, 5</td><td>O</td><td>Bus Cycle status indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is a Ts state whenever one or both are LOW. $\overline{S1}$ and $\overline{S0}$ are active LOW and float to 3-state OFF during bus hold acknowledge.
<table>
<tr><th colspan="5">80C286 Bus Cycle Definition</th></tr>
<tr><th>COD/$\overline{INTA}$</th><th>M/$\overline{IO}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>L</td><td>Interrupt acknowledge</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>H</td><td>Reserved</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>L</td><td>Reserved</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td><td>If A1 = 1 then halt; else shutdown</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td><td>Memory data read</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>Memory data write</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>Reserved</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>I/O read</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>I/O write</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>L</td><td>Reserved</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>Memory instruction read</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>L</td><td>Reserved</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>None; not a status cycle</td></tr>
</table></td></tr>
<tr><td>M/$\overline{IO}$</td><td>67</td><td>O</td><td>Memory-I/O Select distinguishes memory access from I/O access. If HIGH during Ts, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/IO floats to 3-state OFF during bus hold acknowledge.</td></tr>
<tr><td>COD/$\overline{INTA}$</td><td>66</td><td>O</td><td>Code/Interrupt Acknowledge distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ floats to 3-state OFF during bus hold acknowledge. Its timing is the same as M/$\overline{IO}$.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>68</td><td>O</td><td>Bus Lock indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80C286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active LOW and floats to 3-state OFF during bus hold acknowledge.</td></tr>
<tr><td>$\overline{READY}$</td><td>63</td><td>O</td><td>Bus Ready terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge.</td></tr>
<tr><td>HOLD
HLDA</td><td>64
65</td><td>I
O</td><td>Bus Hold Request and Hold Acknowledge control ownership of the 80C286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80L286 will float its bus drivers to 3-state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80C286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH.</td></tr>
<tr><td>INTR</td><td>57</td><td>I</td><td>Interrupt Request requests the 80C286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80C286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.</td></tr>
<tr><td>NMI</td><td>59</td><td>I</td><td>Non-Maskable Interrupt Request interrupts the 80C286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.</td></tr>
<tr><td>PEREQ
$\overline{PEACK}$</td><td>61
6</td><td>I
O</td><td>Processor Extension Operand Request and Acknowledge extend the memory management and protection capabilities of the 80C286 to processor extensions. The input requests the 80C286 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH and floats to 3-state OFF during bus hold acknowledge. $\overline{PEACK}$ may be asynchronous to the system clock. PEACK is active LOW.</td></tr>
<tr><td>$\overline{BUSY}$
$\overline{ERROR}$</td><td>54
53</td><td>I
I</td><td>Processor Extension Busy and Error indicate the operating condition of a processor extension to the 80L286. An active $\overline{BUSY}$ input stops 80C286 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The 80C286 may be interrupted while waiting for BUSY to become inactive. An active $\overline{ERROR}$ input causes the 80C286 to perform a processor extension interrupt when execution WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.</td></tr>
</table>

4-1-2. Numerical calculation processor (OPTION)

This unit can connect with the optional 80C287 numerical calculation processor (NPX). The NPX operates on 12MHz. The NPX is an expansion of the 80C286 CPU architecture. The CPU regards the NPX as an I/O device occupying 0F8h – 0FFh. The NPX itself has no bus control function. When, therefore, the NPX requires data, PEREQ signal is made active to request the CPU to transmit data. The CPU makes *PEREQ active to inform the NPX that it has accepted the request, then the CPU executes data transmission. For the NPX, data are transmitted as the form of IOR/IOW.

When the CPU meets a command to the NPX (ESC command in a certain format) during decoding, it informs the NPX of it as IOW. During the execution of this command, the NPX makes *BUSY signal active to control the CPU not to transmit ESC command any more. If there is any erroneous calculation during processing, the NPX makes *ERROR signal and *BUSY signal low simultaneously to show the error. The SC9889A/B LSI latches the *BUSY signal and informs the CPU, which stops processing of the commands following the error. The error is transmitted through interruption level 13 (IRQ13) to the CPU. The error treatment by the CPU differs from different application program, and the following two ports are used.

Address	Data	Operation
0F0h (IOW)	No meaning	Clears latched *BUSY signal.
0F1h (IOW)	No meaning	Hard reset the NPX in addition to the above.

The port is not effective when reading.

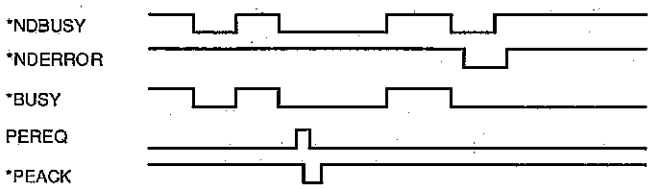


Fig. 4-2

4-2. System control LSI (SC9889B)

The LSI controls all the system using the following functions. The details of the functions are given later.

- CPU interface
- ROM access control
- RAM access control
- HOLD control
- Interruption controller
- Timer
- Serial interface
- RTC & C-MOS RAM
- PORT B
- Power control

4-2-1. CPU interface

This function is divided into the following five blocks:

- Clock control
- Ready control
- Reset control
- Command generator
- Data control

The clock control block forms PRCLK (which is supplied to the CPU) with 14.31818MHz and 23.9616MHz input clocks. With synchronizing the CPU operation phase, PRCLK is divided in 2/4 to generate DMACLK. PRCLK is switched into 11.9808MHz, 14.31818MHz, and 23.9616MHz by the software. According to its selection, SYSCK and DMACLK frequencies are changed. Table 4-2 shows the relationship.

CPU operating frequency	PRCLK	SYSCK	DMACLK
6MHz	11.9808	5.9904	2.9952
7.16MHz	14.3182	7.1591	3.5795
12MHz	23.9616	5.9904	2.9952

Unit: MHz

Table 4-2

Clock used in this LSI includes PRCLK to moderate request for setup time of control signals from the CPU to the LSI.

Since This LSI has CLK stop function, clock before output is used for the circuit which must not be stopped. (SYSCK, DMACLK, clock stop circuit, clock select circuit)

Fig. 4-3 shows synchronizing timing of PRCLK, SYSCK, and DMACLK.

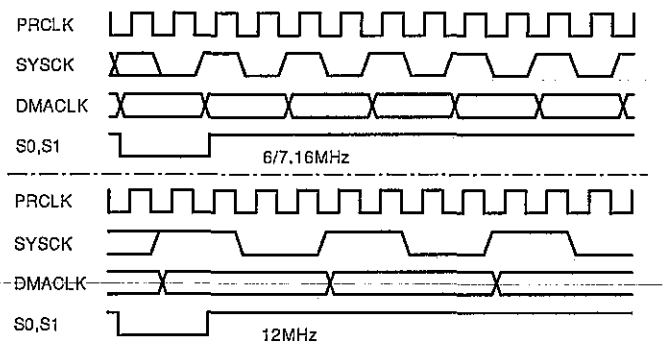


Fig. 4-3

The clock control section generates clocks which are supplied to the timer inside the LSI and the serial interface section. 14.31818MHz is divided into 12 and 1.19MHz is supplied to the timer section. 23.9616MHz is divided into 13 and 1.8432MHz is supplied to the serial interface section.

The ready control section controls cycle length and command signal start timing according to each device access time, address setup time and CPU operating clock. Table 4-3 shows the relationships between the cycle length (wait number) and command starting timing (command delay number) and CPU operating speed and device kinds.

Operating frequency (MHz)	12		7.16/6	
Device	Wait	Command delay	Wait	Command delay
Internal RAM (Conventional memory)	1	0	0	0
Internal RAM (Expanded/EMS)	2	0	0	0
ROM	1	0	0	0
V-RAM (8 bit)	7	0	4	0
V-RAM (16bit)	2	0	1	0
Other 8bit memory	11	3	4	0
Other 16bit memory	5	3	1	0
80C287	0	0	0	0
Display device (8bit), system I/O (0 – 0FFH)	7	2	4	1
Display device (16bit)	2	2	1	1
Other 8bit I/O	11	5	4	1
Other 16bit I/O	5	5	1	1
INTA	2	0	1	0

Table 4-3

The reset control section generates reset signal of the CPU and the system. The reset signal to the CPU are generated by the following three factors:

(1) When PWRGOOD signal is low at power OFF or in case of abnormality.

(2) When writing in the port by the software.

(3) When shut down cycle is detected.

In the case of (1), when PWRGOOD signal becomes low, RESCPU signal is made high and kept high with external pull-up resistor (1Kohm). When PWRGOOD signal becomes high, RESCPU is driven high. In phase 2 after 128clock cycles, RESCPU falls to start the CPU.

In the case of (2), this process is performed by the software when the CPU mode is returned from the protect mode to the real mode. That is, when wring is made into I/O address 064h – 0FEh, the LSI decodes it and makes RESCPU line high for about 6 – 7ms to reset the CPU.

In the case of (3), the unit is started in a certain cycle of CPU, which is called shutdown cycle. This cycle is generated when the CPU cannot treat more processes in occurrence of an exception during double fault exception processing. The CPU informs external devices of this state using *S0 = 0, *S1 = 0, M/IO = 1, and A1 = 1. The LSI detects this sign and makes RESCPU high for 16 clock cycles to reset the CPU.

BRESET signal (system reset) is made high only in the case of (1) to initialize the system. It remains low in the cases of (2) and (3).

The command generator section decodes status signal (*S0, *S1) and M/IO signal from the CPU to form command signal required in the cycle, and output it according to command delay/wait numbers determined by the ready control section.

There are five command signals and their compositions are shown as follows in Table 4-4.

	*S0	*S1	M/IO
•*MEMW	0	1	1
•*MEMR	1	0	1
•*IOW	0	1	0
•*IOR	1	0	0
•*INTA	0	0	0

Table 4-4

In this table, *INTA signal (interrupt acknowledge cycle) is used only in the LSI. SO it does not output externally.

The data control section controls buffers according to data transmission direction in each operation mode of CPU operation, DMA operation, and MASTER operation. Fig. 4-4 shows the data bus configuration of this unit. (L), (I), (E), and (S) in Fig. 4-4 show device locations of Local, Internal, External, and Slot respectively.

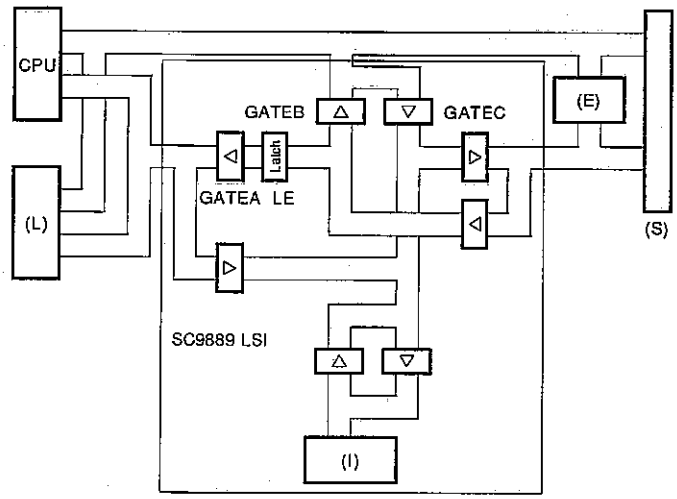


Fig. 4-4

Each device has its effective bus width. I/O device makes *IOCS16 low and memory makes *MEMCS16 low to transmit to the LSI. Address of internal I/O in the RAM or ROM, however, are fixed and decoded in side the LSI without using these signals.

The bus master makes three kinds of access to each device: word, even byte, and odd byte. These kinds of access are classified as in Table 4-5.

Access kind	A0	BHE
Word	0	0
Even number byte	0	1
Odd number byte	1	0
Invalid	1	1

Table 4-5

Table 4-6 shows how GATEA, GATEB, and GATEC are controlled by the combination of the following four factors:

- Data transmission direction (Bus master → device, bus master ← device, memory → IO, memory ← IO in DMA)
- Location on the data but (L, I, E, S)
- Bus width (8 bit, 16 bit)
- Access kind (Word. even number byte, odd number byte)

High ("1") of GATEA/B/C means enable (bus drive).

CPU mode

Write (CPU → device)

In all combinations, GATEA = 0, GATEB = 0, GATEC = 1

Read (CPU ← device)

16/8	LOC	BHE	A0	GA	GB	GC
16	L	0	0	0	0	0
		1	0	0	0	0
		0	1	0	0	0
	I	0	0	1	1	1
		1	0	1	0	1
		0	1	1	1	1
	E/S	0	0	1	0	0
		1	0	1	0	0
		0	1	1	0	0
8	I	0	0	1	1	1
		1	0	1	0	1
		0	1	1	1	1
	E/S	0	0	1	1	0
		1	0	1	0	0
		0	1	1	1	0

Table 4-6(a)

DMA mode

I/O → memory

16/8	LOC	BHE	A0	GA	GB	GC
16	L/E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	0	1
8	E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	1

Table 4-6 (b)

Memory → I/O

16/8	LOC	BHE	A0	GA	GB	GC
16	L	0	0	1	1	0
		1	0	1	1	0
		0	1	1	1	0
	E/S	0	0	1	1	1
		1	0	1	1	1
		0	1	1	1	1
8	E/S	0	0	1	1	1
		1	0	1	1	1
		0	1	1	1	1

Table 4-6 (c)

MASTER mode

Write (Master → device)

16/8	LOC	BHE	A0	GA	GB	GC
16	L/I/E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	1
8	I/E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	0

Table 4-6 (d)

Read (Device → Master)

16/8	LOC	BHE	A0	GA	GB	GC
16	L	0	0	1	1	0
		1	0	1	1	0
		0	1	1	1	1
	I	0	0	0	0	0
		1	0	0	1	0
		0	1	0	0	0
	E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	1	1
8	I	0	0	0	1	0
		1	0	0	1	0
		0	1	0	0	0
	E/S	0	0	0	1	1
		1	0	0	1	1
		0	1	0	0	1

Table 4-6 (e)

4-2-2. Memory sub system

This unit is equipped with 1MB RAM, 64KB system BIOS ROM, and 32KB display BIOS ROM as standard system memory.

The RAM is composed of eight pseudo-static RAM's of 128KB x 8.Two optional 1MB memory cards can be added to expand memory to max. 3MB. System BIOS and display BIOS are provided in the ROM (128KB x 16). The ROM is provided in a ROM board separate from the main board and connected to the main board via 50-pin connector. Fig. 4-5 shows the memory map.

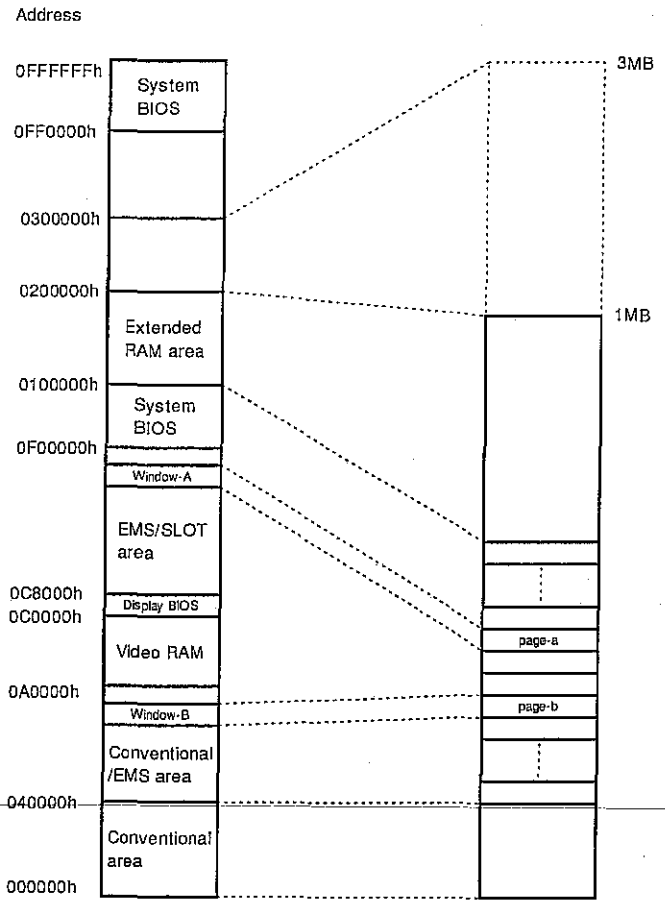


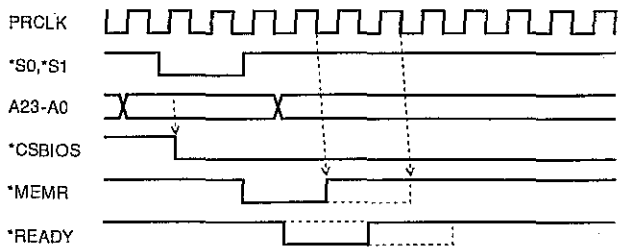
Fig. 4-3

(1) ROM

ROM address signal is supplied by latching the CPU address at the rising of the status signal by the peripheral control LSI (LZ95H22).

The reason why status signal instead of other signals is used for latch is to decrease weight by supplying outputs to the ROM. The upper side of data signal is connected to the CPU data. For the lower side of data, ROM access buffer is used to delay data transmission to reduce the weight number. The chip select signal (*CSBIOS) of ROM is generated by the SC9889A/B LSI.

Immediately after reset, the CPU makes access to the highest position (0FFFFF0h) of address area. When JMP FAR command is executed, access is made near 00FFFF0h. At that time, the chip select signal becomes low at 0FF0000h – 0FFFFFFh and 00F0000h – 00FFFFFh to select the same ROM. Since the display BIOS is included in the same ROM, the chip enable signal becomes active in the display BIOS area 00C0000h – 00C7FFFh. The output enable signal uses *MEMR signal. The data buffer enable signal in the lower side for only ROM reading uses ROM chip select signal and *MEMR signal. Fig. 4-6 shows ROM read timing.



Note: Waveform shown in dotted line is for 12MHz operation.

Fig. 4-4

(2) RAM

(2)-1. Pseudo-SRAM control

This chip supports control of a maximum 4MB of the pseudo-SRAM. Memory has three address spaces of the system area, EMS control area, and private area. The EMS control area can further be divided into three subsections of conventional area, extended area, and EMS area by the internal I/O register setting.

(1) System area

The area of 256KB is allocated to 000000H~03FFFFH as the conventional memory.

(2) EMS control area

Address can be allocated to three areas using the internal I/O register setting.

(a) Convectional memory setting
An address space of 384KB can be allocated to 040000 ~ 09FFFFH as a conventional memory area.

(b) Extended memory setting
Address space can be allocated after 100000H as an extended memory area.

(c) EMS area
To support the EMS version 4.0, 34 windows of 16KB increments can be mapped in 040000~09FFFH and 0C8000H~0EFFFH.

(3) Private area

Using the internal I/O register setting, a 256KB of address space is allocated to 0E0000H~0EFFFFH (accessed by bank select), which is to be used to save the VRAM contents during the resume and used by the system. The private area may be eliminated by the internal I/O register setting.

NOTE: With the current version of this LSI (TS1), it does not assure the interleave in the 12MHZ non-wait mode. Where, "0" must be written to INTLV of the SPRAMCFL register discussed later.

(2)-2. RAM configuration

(1) System area

Among 4MB memory area supported by the memory controller, a 256KB of address space 000000H~03FFFFH is allocated as a conventional memory, regardless of the internal I/O register setting.

(2) EMS control area

The maximum 4MB area, except for the system area and the private area, is allocated to the EMS control area, and mapped to the conventional area, extended area, and EMS area by the internal I/O register setting.

There are EMSCFR register, PSRAMCF register, and EMSSTAT register that controlled as the internal I/O registers and their bit definitions are shown next.

EMSCFR register

Bit	Signal name	Significance
0~2	SW0~2	EMS control register I/O address setting
3, 4	JP2, 3	Extended memory capacity setting (expansion)
5, 6	SW5, 6	Extended memory capacity setting
7		Reserved. Read/write possible

Table 4-7

PSRAMCF register

Bit	Signal name	Significance
0	RESERVED	Reserved. Read/write possible
1	INTVL	Pseudo-SRAM interleave access enable
2	*PCS3EN	256KB standard RAM usage setting
3, 4	JP0, 1	Extended memory capacity setting
5	VPTMEM	Private memory access enable
6, 7	MAP0, 1	Private memory bank select

Table 4-8

EMSSTAT register

Bit	Signal name	Significance
0~2	SW0~2	State of EMS control register I/O address allocation
3, 4	SW3, 4	Both SW3 and SW4 reads "1" at all times.
5, 6	SW5, 6	State of the extended memory capacity setting
7	EMSEN	EMS on/off setting

Table 4-9

The EMSCFR and PSRAMCF registers are allocated to 04H and 05H of the Sharp original port, and reset to "0" when reset.

SW0~2, and SW5~6 of the EMSSTAT register are read only bits which the data written in the EMSCFR register is read. EMSEN is a read/write bit that turns to "0" when reset.

When operated with the CPU clock at 24MHz, INTLV of the PSRAMCF register, is a bit which enables the non-wait access for the conventional memory and private memory interleave mode when the bit is set to "1".

(a) Conventional setting

To allocate the memory space 040000H~09FFFFH to a conventional memory, EMSEN of the EMSSTAT register must be set to "0" to disable the EMS.

(b) Extended setting

By setting SW5~6, JP2~3, of the EMSCFR register and JP0~1, and *PCS3EN of the PSRAMCF register, the memory space after 100000H can be allocated to the extended memory in a manner as shown next.

SW6	SW5	JP3	JP2	JP1	JP0	*PCS3EN	Extended memory
0	0	*	*	*	*	*	0MB
0	1	*	*	*	*	*	64KB (100000H~10FFFFH)
1	0	0	0	0	0	1	0MB
1	0	0	0	0	0	0	256KB (100000H~13FFFFH)
1	0	0	0	0	1	1	1MB (100000H~1FFFFFH)
1	0	0	0	0	1	0	1.25MB (100000H~23FFFFH)
1	0	0	0	1	0	1	2MB (100000H~2FFFFFH)
1	0	0	0	1	0	0	2.25MB (100000H~33FFFFH)
1	0	0	0	1	1	1	3MB (100000H~3FFFFFH)
1	0	0	0	1	1	0	3.25MB (100000H~43FFFFH)
1	0	0	1	*	*	1	3MB (100000H~3FFFFFH)
1	0	0	1	*	*	0	3.25MB (100000H~43FFFFH)
1	0	1	0	*	*	1	3MB (100000H~3FFFFFH)
1	0	1	0	*	*	0	3.25MB (100000H~43FFFFH)
1	0	1	1	*	*	1	3MB (100000H~3FFFFFH)
1	0	1	1	*	*	0	3.25MB (100000H~43FFFFH)
1	1	*	*	*	*	*	512KB (100000H~17FFFFH)

Table 4-10

*: don't care

* PCS3EN is the bit employed to specify the usage of the 256KB area within the standard RAM which may be used as a private area when "1" and as an EMS control area when "0".

(c) EMS setting

To turn on the EMS, EMSEN of the EMSSTAT register must be set to "1". To support the EMS version 4.0, the EMSADR register and the EMSDAT register are provided as internal registers, whose bit definition is shown in Table 4-11 and Table 4-12 respectively.

EMSADR register

Bit	Signal name	Significance
0~7	EMSADR0~7	EMS mapping register address

Table 4-11

EMSDAT register (EMS mapping register), ,

Bit	Signal name	Significance
0~7	EMSDAT0~7	EMS mapping register data
8~14	—	Undefined. Reads "0" at all times.
15	EMSPEN	EMS page enable bit

Table 4-12

The EMS control register for the EMSADR register, EMSDAT register, including the EMSSTAT register, is I/O address allocated by SW0~2 of the EMSSTAT register, which are set as shown in table 4-13.

SW2	SW1	SW0	EMSSTAT	EMSADR	EMSDATL	EMSDATH
0	0	0	208H	209H	20AH	20BH
0	0	1	218H	219H	21AH	21BH
0	1	0	248H	249H	24AH	24BH
0	1	1	258H	259H	25AH	25BH
1	0	0	268H	269H	26AH	26BH
1	0	1	2A8H	2A9H	2AAH	2ABH
1	1	0	2B8H	2B9H	2BAH	2BBH
1	1	1	2E8H	2E9H	2EAH	2EBH

Table 4-13

When reset, SW0~2 are reset to "0".

The EMSADR register is a 8-bit read/write register which is employed to point the 34 EMS mappings using EMSADR2~7. EMSADR2~7 is automatically incremented when the high side of the EMSDAT register is accessed. "0" is always read from EMSDAR0~1 and write is ignored.

The following shows the address setup range for the EMSADR register

40H, 44H, 48H, 4CH, 50H, 54H, 58H, 5CH, 60H, 64H, 68H, 6CH, 70H, 74H, 78H, 7CH, 80H, 84H, 88H, 8CH, 90H, 94H, 98H, 9CH, C8H, CCH, D0H, D4H, D8H, DCH, E0H, E4H, E8H, ECH

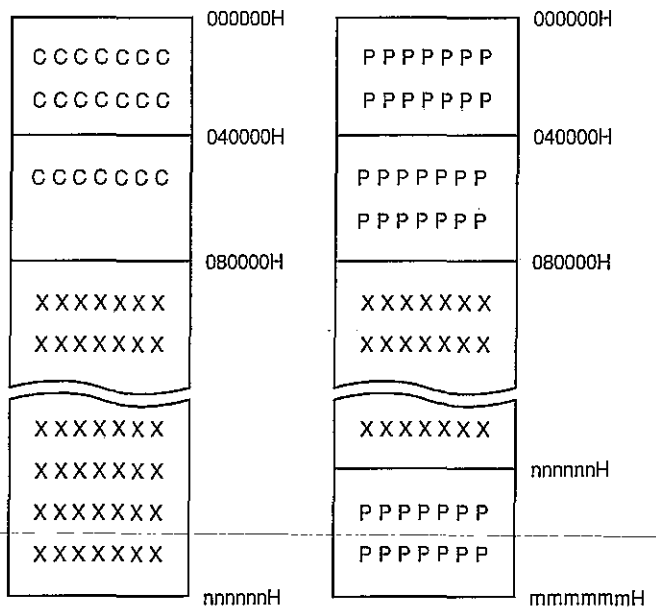
The EMSDAT register is a 16-bit read/write register in the CPU mode and 8-bit read/write register in the master mode, and there are 34 sections. The EMS mapping data is set in EMSDAT0~7 of the EMSDAT register and determines the page that mapped to the window of address space of 040000H~09FFFFH and 0C8000~0EFFFFH. Window can be set on or off for EMSPEN; sets on when "1". EMSDAT8~14 are read "0" at all times and write is ignored.

When the EMSADR register is out of the setup address range, EMSDAT0~15 is read "0" and write is ignored.

To obtain the EMS control area, subtract the system area and the private area from all memory area supported by the memory controller.

Its capacity is max. 3.75MB when the private memory is not used (*PCS3EN = 0).

Fig. 4-7 shows the mapping of the EMS control area.



Memory map for the conventional memory

Memory map for the EMS

Fig. 4-7

"C" represents conventional memory mapping, "X" represents extended memory mapping, and "P" represents expanded memory mapping. "nnnnnnH" is dependents to the extended area setting, "mmmmmmH" to the actually installed memory capacity.

The actually installed memory capacity may be set to "nnnnnnH" when mapping the conventional memory. For an example, the extended area for the 4MB memory, it should be set to 3.25MB and "nnnnnnH" is 3DFFFFH (in case *PCS3EN=0).

When mapping the EMS memory, the capacity under the actual memory capacity should be set to "nnnnnnH". For the 4MB of actually installed memory, the EMS area should be set to 0~3.25MB. If 0MB was set, all are mapped as the EMS memory.

(3) Private area

It may be possible with the internal I/O register setting to reserve a 256KB private area out of the memory controller supported 4MB memory.

To reserve the private area, set *PCS3EN of the PSRAMCF register to "1" and set 256KB of the internal standard RAM as the private memory. Set EMSEN of the EMSSTAT register to "0" and PVTMEM of the PSRAMCF register to "1", which is then mapped to the address space of 0E0000H~0EFFFFH.

To access the 256KB private memory, four banks must be selected using MAP0~1 of the PSRAMCF register.

4-2-3. Hold mediation and sleep function

This function mediates DMA request, refresh request, and HOLD request during sleep and applies HOLD to the CPU. It also delivers acknowledge for each request. The mediate circuit is composed of three sets the D-F.F. connected in series in two stages. The first F.F. samples each request to process it by determining priority between requests which are under process and requests which are sampled. Then the requests are sent to the second F.F. If there is any request which is under process, the other requests are kept waiting until the process is completed. When two or more requests are made simultaneously, DMA request has the first priority, and sleep request has the last priority.

The second F.F. and the AND of HOLD and HLDA signals are used as acknowledge of the requests.

The sleep function stops the clock which is supplied to the CPU until the interruption line becomes active after HLT command is executed in order to reduce power consumption of memory. When the unit goes into the sleep mode, HOLD signal is made high to request bus hold to the CPU. When the acknowledge (HLDA) signal returns, the clock is stopped in the first phase 2. This is because the power consumption is minimized in that state. Then the hold request is cancelled, and delay of 3SYSCK cycle is made in the externally attached circuit to drop HLDA signal which is inputted to the LSI. Since the clock is stopped, the CPU is kept hold. The LSI returns to the normal state. Though there is DMA request or refresh request in the sleep, they can be processed without competition. When the CPU executes HLT command S0 and S1 are made low and M/*IO and A1 are made high to show the hold state. The sleep controller detects it and the unit goes into the sleep mode in the following sequence.

(1) HOLD request is delivered to the CPU. When refresh request or DMA request is overlapped, the mediate circuit will mediate it.

(2) Hold acknowledge is confirmed to stop the CPU clock in synchronous with the falling of clock which is inputted to the controller in ϕ2.

(3) HOLD request (HOLD signal) by the sleep is cancelled. In this case, the CPU is kept hold.

(4) After the HOLD signal is made low by the external D-F.F. (3 stage), HLDA signal is delayed by 3 clocks of SYSCK. DMA in the sleep is transmitted and refresh is made in this state.

Escape from the sleep mode occurs when any interruption request including NMI is generated. When an interruption occurs, the CPU clock supply is resumed in synchronous with falling of the clock which is inputted to controller. The CPU starts execution of the command next to the HLT.

When the input from the EXPND terminal is low, it is regarded that the expansion unit is connected, and procedure (1) to (4) are prohibited and the sleep function is not performed.

4-2-4. Interrupt control

A pair of 82C59A interrupt controllers are internally contained in this chip for the interrupt control and supports 16 interrupt levels in conjunction with the cascade connection NMI. The NMI is port-B controlled.

As an 8-bit I/O device on the system bus (XD bus), a pair of 82C59A has address mapped to 020H~03FH on the master side and 0A0H~0BFH. In order to avoid contention with the CPU clock switch controlling I/O address 022H and 023H for the 82C59A on the master side, the selection is not done when the bit of the latch address is "1".

Table 4-14 shows the 82C59A interrupt outputs.

Master	Slave	Function
IRQ0		Timer output channel 0
IRQ1		Keyboard (output buffer full)
IRQ2		Interrupt from the slave side controller
	IRQ8	Real time clock interrupt
	IRQ9	VGA controller or INT0AH (IRQ2)
	IRQ10	Reserved (expansion slot)
	IRQ11	Reserved (expansion slot)
	IRQ12	Reserved (expansion slot)
	IRQ13	Co-processor
	IRQ14	Hard disk controller
	IRQ15	Reserved (expansion slot)
IRQ3		Serial port 2 (COM2)
IRQ4		Serial port 1 (COM1)
IRQ5		Parallel port 2
IRQ6		Floppy disk controller
IRQ7		Parallel port 1

Table 4-14

4-2-5. Timer

A single 82C54 interval timer is internally contained in this chip. The 82C54 is mapped to the I/O address 040H~05FH as an 8-bit I/O device on the system bus (XD bus). Three independent 16-bit counter on channels 0~2 of the 82C54 can be defined Table 4-15

Channel 0	System timer
GATE0 CLKIN0 CLKOUT0	Fixed ON 1/12 14.31818MHz clock 82C59A IRQ 0
Channel 1	Refresh request generator
GATE1 CLKIN1 CLKOUT1	Fixed ON 1/12 14.31818MHz clock Refresh request cycle
Channel 2	Speaker tone generator
GATE2 CLKIN2 CLKOUT2	Fixed ON 1/12 14.31818MHz clock Speaker drive

Table 4-15

4-2-6. Serial interface

The 82C50 UART is internally contained in this chip as a serial interface and supports a single channel RS-232C interface using the external RS-232C driver as an internal SIO. This also used for interface with the internal modem.

Two serial interfaces may be port allocated and set on or off, which the SIOCFR register is used for the RS-232C and the MDMCFR register for the internal modem. The SIOCFR register is a 7-bit read/write register which is allocated to 01H of the Sharp original port. The MDMCFR register is a 2-bit read/write register which is allocated to 03H of the Sharp original port.

Table 4-16 and 4-17 shows bit definition for SIOCFR and MOMCFR registers.

SIOCFR register

Bit	Signal name	Significance
0~2	FDD0~2	Reserved. Read/write possible.
3	*SIOEN	Internal SIO port allocation
4	SI01/*2	Internal SIO on/off setting
5	*INTKEY	Reserved. Read/write possible.
6	*LCDEN	Display device selection
7	—	Undefined. Reads "0" at all times.

Table 4-16

MDMCFR register

Bit	Signal name	Significance
0	OUTSEL	MORSTN output signal selection
1~3	—	Undefined. Reads "0" at all times.
4	*MDMEN	Internal modem on/off setting
5~7	—	Undefined. Reads "0" at all times.

Table 4-17

When reset, *SIOEN of the SIO CFR register and *MDMEN of the MDMCFR register are set to "1" and all others are reset.

*SIOEN and SIO1/*2 of the SIOCFR register may be revised of their contents when written to "02" to the Sharp original port. The inverted bit 4 of the 02H port corresponds to SIO1/*2 and bit 5 to SIOEN.

Table 4-18 shows the ports that are allocated by the setting of SIOCFR and MDMCFR registers vs. active input to IRQ3 and IRQ4 of the 82C59A.

*SIOEN	*MDMEN	SIO1/*2	Internal SIO	Internal modem	IRQ3 input	IRQ4 input
0	0	0	COM2	COM1	Internal SIO	Internal modem
0	0	1	COM1	COM2	Internal modem	Internal SIO
0	1	0	COM2	OFF	Internal SIO	External IRQ4
0	1	1	COM1	OFF	External IRQ3	Internal SIO
1	0	0	OFF	COM1	External IRQ3	Internal modem
1	0	1	OFF	COM2	Internal modem	External IRQ4
1	1	0	OFF	OFF	External IRQ3	External IRQ4
1	1	1	OFF	OFF	External IRQ3	External IRQ4

Table 4-18

The RS-232C interface serial input/output and control signals can be inverted with POLINV of the VGACNT register. When POLINV is at "1", the polarity inverts. The VGACNT register is allocated to 0EH of the Sharp original port whose bit definition is shown in Table 4-19.

VGACNT register

Bit	Signal name	Significance
0	POLINV	RS-232C input/output polarity inversion
1	DISVGA	Internal VGA on/off setting
2, 3	PWRDWN1, 2	VGA controller mode setting
4~7	RESERVED	Reserved. Read/write possible

Table 4-19

When reset, all are reset to "0".

To reset the internal modem that can be installed within the machine, the output from the MORSTN line is used. The 1-bit output of the MORSTN output port can be switched with the port select signal output using OUTSEL of the MDMCFR register. When OUTSEL is at "1", the bit 3 of the I/O address 202H port is issued. When "0", the decoded signal of the I/O address 202H is issued as a port select signal. The 202H port is a read/write internal I/O register whose big definition is shown Table 4-20.

202H port

Bit	Signal name	Significance
0~2	RESERVED	Reserved. Read/write possible
3	MORSTN	Internal modem reset signal
4	RESERVED	Reserved. Read/write possible
5~7	—	Undefined. Reads "0" at all times.

Table 4-20

When reset, bits 0~4 are reset.

4-2-7. RTC and CMOS RAM control

For this chip, RTC is controlled by AS, DS, R/W, and SCRTCN outputs. For setup expansion, a 2KB CMOS RAM is provided.
Among 11 bits address input of the 2KB CMOS RAM, the low 6 bits is connected to the I/O 070H port bits 0~5, and high 5 bits to the latch address bits 10~14. Which is to be selected, RTC or CMOS RAM, when the I/O 071H port is accessed is determined by the data in the I/O 70H bit 6. When "0", RTC is selected and "1" the CMOS RAM. See Fig. 4-8 for the mapping of the RTC and the CMOS RAM.

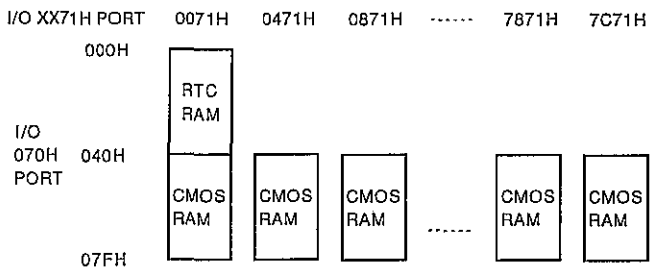


Fig. 4-8

4-2-8. Port-B

The port-B consists of a logic gate which is used for NMI occurrence control, speaker output control, and refresh detection by the parity and I/O channel checks.

4-2-9. Power control

The system power source is divided into several blocks to allow each block to be turned on/off separately. Therefore, the power control section is equipped with the port to turn off the power sections which are not used. For that purpose, VLCCNT, VBLCNT, VMDCNT, VIFCNT, VCCOFF, and *ONRSM are provided. The state where the power is supplied but no operation is requested is detected and if the state continues for a certain period, the power is automatically turned off.

For the power control port, a part of SOP (Sharp Original Port) assigned to 07Ch and 07Dh is used. Port number (called as index) is written into 07Ch of SOP and read/write is made with the data in 07Dh. When 07Dh is accessed, the index is cleared to be No. 0. therefore 07Ch must be set for each time. SOP related to the power control section is shown in Table 4-21 through 4-30.

PWRCNT register (Index 06Ch, R/W)

Bit	Signal name	Meaning
0	PCVIF	Printer/RS-232C interface IC control
1	PCVLCD	VGA controller and LCD power control
2	PCVCC	System power (Vcc) control
3	PCBL	Back light power control
4	PCVMD	MODEM power control
5 ~ 7	RESERVED	Reservation bit, Read/Write allowed

Table 4-21

When resetting, each bit of PCVIF, PCVCC, PCBL, and PCVMD are set to "1" and the others are reset.

ATSTBY register (Index 07Ch, R/W)

Bit	Signal name	Meaning
0	ASVIF	Auto I/F power off enable/disable setting
1	ASLCD	Auto power save enable/disable setting
2	ASVCC	Auto resume enable/disable setting
3 – 7	RESERVED	Reservation bit, Read/Write allowed

Table 4-22

When resetting, all are reset to "0."

RWRSTAT register (Index 08Ch, R/O)

Bit	Signal name	Meaning
0	PSVIF	Printer/RS-232C interface IC control state
1	PSLCD	LCD power (VLCD) state
2	PSVCC	System power (Vcc) state
3	PSBL	Back light power (VBL) state
4	PSVMD	MODEM power (VMDM) state
5 ~ 7	—	Reservation bit. Always reads "0."

Table 4-23

PWRTIM register (Index 09h, R/W)

Bit	Signal name	Meaning
0 – 3	PST0 ~ 3	Auto power save time setting
4 ~ 7	RESERVED	Reservation bit, read/write allowed.

Table 4-24

When resetting, PST3 – 0 are set to "1," and the others are reset. ,

RSMTIM register (Index 0Ah, R/W),

Bit	Signal name	Meaning
0 ~ 6	ART0 ~ 6	Auto resume time setting
7	RESERVED	Reservation bit, Read/Write allowed.

Table 4-25

When resetting, ART6 – 0 are set to "1," and bit 7 is reset.

RSMCNT register (Index 0Bh, R/W)

Bit	Signal name	Meaning
0	RSMEN	Resume mode setting
1	CIEN	Reservation bit, read/write allowed.
2	MRIEN	Reservation bit, read/write allowed.
3 ~ 7	RESERVED	Reservation bit, read/write allowed.

Table 4-26

When resetting, all are reset to "0."

RSTFCT register (Index 0Ch, R/O)

Bit	Signal name	Meaning
0	—	Not defined. Always reads "0."
1	RCR	System power (Vcc) OFF request effective state
2	RCCI	Internal SIO power ON factor state by CI input
3	RCMRI	Internal modem RI input power ON factor
4 – 7	—	Not defined. Always reads "0."

Table 4-27

EXSTAT register (Index 0Dh, R/O)

Bit	Signal name	Meaning
0	EXPND	Expansion unit contact state
1 – 7	—	Not defined. Always reads "0."

Table 4-28

VGACNT register (Index 0Eh, R/W)

Bit	Signal name	Meaning
0	POLINV	Internal SIO input/output polarity reversion
1	DISVGA	Internal VGA enable/disable setting
2	PWRDWN1	VGA controller mode setting (relax mode)
3	PWRDWN2	VGA controller mode setting (retire mode)
4 – 7	RESERVED	Reservation bit, read/write allowed.

Table 4-29

When resetting, all are reset to "0."

NMIFCT register (Index 0Fh, R/O)

Bit	Signal name	Meaning
0	RSMNMI	Resume NMI request effective state
1 – 7	—	Not defined. Always reads "0."

Table 4-29

Fig. 4-9 shows the outline of the power control section of this unit.

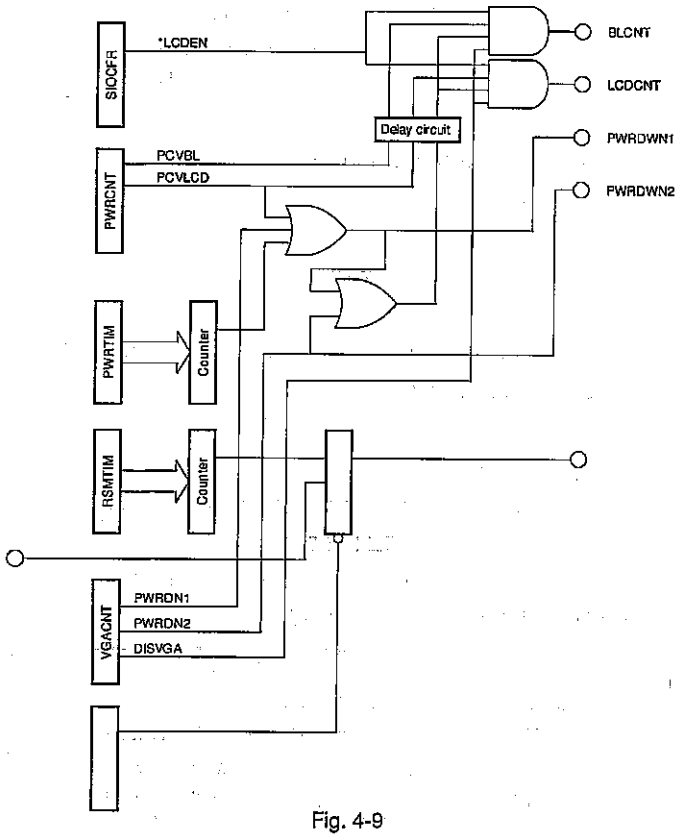


Fig. 4-9

The basic functions of the power control section are shown Table 4-31.

Control by the ports

Control item	Control signal	ON condition	OFF condition	Remarks	
LCD	*LCDEN	0	1	SOP1	bit 6
	DISVGA	0	1	SOPE	bit 1
	PCVLCD	1	0	SOP6	bit 1
	PWRDWN1	0	1	SOPE	bit 2
	PWRDWN2	0	1	SOPE	bit 3
	SHUT	1	0	Cover close external signal	
Back light	*LCDEN	0	1	SOP1	bit 6
	DISVGA	0	1	SOPE	bit 1
	PCVBL	1	0	SOP6	bit 3
	PWRDWN1	0	1	SOPE	bit 2
	PWRDWN2	0	1	SOPE	bit 3
	SHUT	1	0	Cover close external signal	
I/F power	PCVIF	1	0	SOP6	bit 0
Modem	PCVMD	1	0	SOP6	bit 4

Table 4-31

Control by the timer

This unit provides the following two functions using the basic functions in Table 4-32.

Control item	Control timer	Prohibit condition	Reload condition	
LCD back light	PWRTIM SOP9 Bit 3 – 0	ASLCD = 0 SOP7 bit 1	①	IRQ1 rising
			②	Internal SIO interruption
			③	Write to SOP6, 7, 9
I/F power	15 minutes fixed	ASVIF=0 SOP7 bit 0	①	Access to printer port
			②	Access to SIO
			③	Write to SOP6, 7
NMI	RSMTIM SOPA bit 6 – 0	ASVCC=0 SOP7 bit 2	①	IRQ1 rising
			②	Internal SIO interruption
			③	Write to SOP6, 7, A

Table 4-32

(1) Power save function
When the keyboard/mouse is not used for a certain period, LCD/back light power is turned off (auto power save). Each of LCD and back light power can be independently turned off by software.

(2) Standby function
The power to maintain the system state is kept ON and the other powers are turned off and the power consumption is minimized in the sleep mode. When an expansion unit is connected, this function cannot be used.

The power save function detects conditions which can be regarded as that the unit is not operated. If that conditions continues for a certain period, The LCD and the back light powers are automatically turned off. The power save controller includes one minute timer. Count is made when there is not interruption request from the key controller (8042), interruption from internal SIO set to COM2, or write access to SOP6, 7, 9. When a predetermined time is reached, LCDCNT signal and BLCNT signal are made low and the LCD and the back light are turned off. For versions outside Japan, PWRDWN1 signal is made high to set the VGA controller to the sleep mode and to stop the display cycle, reducing current consumption in V-RAM.

VGA controller operation mode can be directly set with internal I/O

register (SOP VGACNT register). The Mediate mode and the sleep mode are set by PWRDWN1 and 2 of VGACNT register. In the sleep mode, the display cycle is stopped but read/write from the bus master is enabled. In the Mediate mode, cycles to V-RAM other than refresh are prohibited. When either of PWRDWN1 or 2 is made high, both LCDCNT and BLCNT signals are made low to turn off the power of LCD/Back light.

VGA controller operation mode is as follows according to PWRDWN1 and 2 in Table 4-33.

PWRDWN2	PWRDWN1	LCD power	BL power	VGA controller	Remark
0	0	ON	ON	Normal mode	
0	0	ON	OFF	Normal mode	PWRCNT register PCBL = 0
0	0	OFF	OFF	Relax mode	Auto power save or PWRCNT register PCLCD = 0
0	1	OFF	OFF	Relax mode	
1	0	OFF	OFF	Retire mode	
1	1	—	—	Prohibition	

Table 4-33

When the power save function is used, PWRDWN1, 2 are set to "0." DISVGA is set to "0" to make the internal VGA effective. SIOCFR register and *LCDEN is set to "0" and LCD is selected as the display device.

To directly turn off the LCD power and the back light power by software, write "0" to PCVLCD and PCBL of PWRCNT register. In this case, similarly to the auto standby, PWRDWN1 signal is driven to high and the VGA controller goes into the mediate mode. When, therefore, it is required to turn off the LCD/back light power in the CRT mode, *LCDEN is driven to high. In this case, PCVLCD must be kept to "1."

When the power save function (auto power save) by the timer is used, PCVLCD and PCLB of PWRCNT register are kept to "1." "1" is written into ASLCD of ATSTBY register to make the timer effective, and the time to require for PWRTIM register power save is set.

PWRTIM register sets auto power save time. Setting is made in the range of 0 to 15 minutes in increment of 1 minute by PST3 – 0. The actual time, however, is shorter than the set value by less than 1 minute. When all of PST3 – 0 are "1," the set value is 14 – 15 minutes. In read/write enable mode, the set value is read. When interruption request signal (IRQ1) from 8042 or internal SIO interruption signal set to COM2 rises before reaching the set time, the set value is reloaded to the timer and counting is restarted from the beginning. When the Sharp Original Port, PWRCNT register, ATSTBY register or PWRTIM register is written, the timer is reloaded.

To use the standby function, write "1" into RSMEN of the RSMCNT register to enable this fucntion. To shift to the standby mode, there are following two cases:

(1) Ctrl + Alt + Pause is pressed and rising waveform is inputted from the 8052 keyboard controller to the RSMSW terminal.

(2) The keyboard or mouse is not operated for a certain period.

In the case of (1), high level signal is outputted from the NMI terminal at the rising edge of signal which is inputted from RSMSW terminal, and NMI is applied to the CPU. While in the case of (2), the timer in the resume controller keeps counting while there is no interruption request from 8042 or interruption request from internal SIO. When the set time is reached, NMI is generated. However, similarly to the sleep function, if the input from EXPND terminal is low, NMI output is prohibited and the resume function does not work. EXPND terminal input state can be read by EXPND of the EXSTAT register.

When using the resume function (auto resume) by the timer, write "1" into ASVCC of the ATSTBY register to make the timer effective, and set the time to power down of the RSMTIM register. The RSMTIM register sets the auto resume time. The setting can be made from 0 to 127 minutes by increment of 1 minute by ART6 – 0. The actual time, however, is shorter than the set value by less than 1 minute. When all of ART 6 – 0 are "1," time is set to 126 – 127 minutes. In read/write enable, the set value is read. In the same manner as the auto power save, when interruption request signal (IRQ1) from 8042 or interruption request signal from internal SIO rises, the set value is reloaded into the timer and the counting is started from the beginning. When the Sharp Original Port PWRCNT register, ATSTBY register, or RSMTIM register is written, the timer is reloaded.

In either case of (1) or (2), the process after generation of NMI is the same, and must be supported by software.

To make power down in the resume mode, the following procedures are required in the NMI process routine.

(1) Judge the NMI factor.

(2) Stand the flag which shows generation of the NMI which requests standby.

(3) Check this flag in the timer interruption (IRQ0) process routine, and judge if the unit may go into the standby mode. (During access of FD/HD, shift to the standby cannot be made.)

(4) Operate the PWRCNT register to cut off each block power. Control the HD controller to cut off HD spindle motor.

(5) Execute HLT command to go into the sleep mode.

To judge the NMI factor in (1), the NMIFCT register is read. When RSMNMI bit is "1," RSMSW input or NMI by resume timer is generated. Reset from the standby mode is made by pressing Ctrl + Alt + Pause keys. In this case also, the NMI is generated.

This unit is equipped with register group to reduce current consumption by turning off the printer/RS232C driver/receiver power. This function is called as the interface power off. This function enables to reduce current consumption of the interface IC when the printer and RS-232C are not used. The interface power off function works when there is no access to the printer or internal SIO for a certain period (auto interface power off), or when the internal I/O register is directly operated by software.

To directly operate the interface power off by software, write "0" into PCVIF of the PWRCNT register. In this case, the printer interface IC output becomes Hi-Z and the RS-232C line driver receiver goes into the standby mode, reducing the circuit current.

When the auto interface power off is used, PCVIF of the PWRCNT register is kept to "1," and "1" is written into ASVIF of the ATSTBY register to enable the timer. The timer is cleared when access is made to the internal printer and the internal SIO. The timer is cleared also when data are written into PWRCNT register of Sharp Original Port or into ATSTBY register. It takes 14 to 15 minutes until the power off fucntion works after the timer is cleared.

As interface power off, the internal modem power can be controlled. To turn off the power (VMDM) of internal modem, write "0" into PCVMD of the PWRCNT register. By this, signal is outputted from the VMDCNT terminal to turn off the modem power.

In the case of auto power off or auto interface off, the power is automatically turned off by the timer and the CPU can read states of the LCD power, the back light power, and the printer/RS-232C control by reading the RWRSTA register. The PWRSTA register is a read-only register and assigned to 08H of the Sharp Original Port. Except for PSVIF, PSLCD, and PSBL, the power control data set by the PWRCNT register are read. When "0," it is OFF, and when "1," it is ON.

4-3. Peripheral control LSI (LZ95H22)

4-3-1. Printer interface

The printer port has three ports inside the LZ95H22, and the flipflop and input/output buffer between the LZ95H22 and the printer connector.

Printer ports, port-1 [378H] [379H] [37AH] and port-2 [278H] [279H] [27AH] can be selected by the Sharp original port.

No print data and printer control signals will be issued when the CNT_D from the printer connector is other than a low state.

4-3-2. VGA interface

There are two write only register in the LZ95H22 besides the display chip. Those registers limit the address used by the VRAM.

Write 06H in 3CEH, then write the data in 3CFH, which are set in Table 4-34.

I/O address		Bit allocation
3CEH	Graphics address	06H
3CFH	Miscellaneous register	Bit 3, 2

bit3	bit2	Address used
0	0	A0000H~BFFFFH
0	1	A0000H~AFFFFH
1	0	B0000H~BFFFFH
1	1	B8000H~BFFFFH

Table 4-34

4-3-3. Power save

As signal VIFCNT from the SC9889 controls the buffer between the serial interface and the printer interface, it saves the power equaling to the buffer.

4-4. Keyboard

Main parts of the keyboard interface is managed by two devices of the 80C42 and the 80C52. The 80C52 scan the keyboard matrix and its data is sent to the 80C42 in a serial form. Since the signal on the keyboard matrix is analog, depression of a key is informed by interrogating the voltage. In order to allow the 80C52 to handle this signal, there is a need of a digital to analog conversion which is carried out by the keyboard interface chip (3JD2CA1A). Not only the 80C42 converts it to the form that the scanned data may be handled by the processor (ASCII/JIS), an interrupt is caused to the processor via the IRQ1 line. The processor reads the keyboard data from the 80C42 within the interrupt routine and stores in the key buffer.
The internal keyboard is standard with the machine, but it may use the external keyboard of the standard AT/AX specification with the portable FDD option attached. In this event, the signal line from the 80C52 must be prohibited by a high state of *INTKEY. This signal is allocated to 02H of the SOP index (SIOCFR register) and its bit definition is shown in Table 4-35.

SIOCFR register (Index 02H, R/W)

Bit	Signal name	Significance
0~2	FDD0~2	Reserved bit, read/write possible
3	*SIOEN	Internal SIO on/off setting
4	SIO1/*2	Internal SIO port allocation
5	*INTKEY	Internal key on/off setting
6	*LCDEN	Display device selection
7	—	Undefined

Table 4-35

There is no ten key keypad in the standard keyboard, an optional keypad may be connected to the main unit or expansion unit. This is allowed by taking out some of keyboard matrix signals to the keypad connector.

4-5. Display circuit

The PC-6220 has a 82C455 VGA display controller for both LCD and CRT display. In VGA (Video Graphics Array) mode, maximum resolution is 640 × 480, 256 colors out of 256k colors (in CRT), 16 gray scale for LCD. And also the backward compatibility (MDA,CGA,EGA HGC) is supported in this chip.

4-5-1. Overview of Display System

1) Display mode

The display mode of PC-6220 is not only compatible to VGA, but also EGA, CGA, MDA and HGC display adaptors.
In the cases of IBM VGA etc., some of CGA application softwares are not able to excuted properly though, with the model PC-6220, even those application softwares can be excuted successfully.

2) VGA mode (Video Graphics Array)

An analog type display will be used with the VGA mode and can be displayed 256 colors simultaneously out of 256 thousands colors. And it supports 480 lines in the horizontal resolution in addtion to current maximum resolution of 400 resolution.

3) EGA mode (Enhanced Graphics Adaptor)

A digital type display will be used with the EGA mode and can be displayed 16 colors simultaneously out of 64 colors. And it supports 350 lines in the horizontal resolution.
In the cases of VGA or EGA modes, the CG font will be given by the software when booting, the BIOS sets up the default of CG font.

4) CGA mode (Color Graphics Adaptor)

A digital type display will be used and it supports 200 lines in the horizontal resolution.

5) MDA mode (Monochrome Display Adaptor)

A monochorome digital display will be used, it only supports 720 × 350 dots resolution character mode. (in case of PC-6220, 640 × 350 dots resolution.)

6) HGC mode (Hercules Graphics Card)

A monochrome digital display is used with graphics card made by Hercules and has graphics function. The function of HGC itself is expanded version of MDA, and normally initiated at the same mode of MDA.
Since the graphics mode of HGC is 720 × 348 dots, the PC-6220 will only supports to CRT.

4-5-2. The relationship between each mode and display type

Mode / Display type	VGA	EGA	CGA	MDA	HGC	Connector
Analog Display for VGA	○	○	○	○	○	Analog
Enahanced Color Display	×	○	○	×	×	Digital
Color Display	×	×	○	×	×	Digital
Monochrome Display	×	×	×	○	○	Digital
LCD	○	○	○	○	△	—

○ ..... Support △ ..... Functions as MDA × ..... Not support

Table 4-36

In table 4-36 the display type and mode should be selected on the set-up menu, and effective when the system is booted. The selection of LCD and CRT can be switched by the slide switch located on the side of the main unit.

4-5-3. VGA mode control

The color display control of PC-6220 VGA mode.

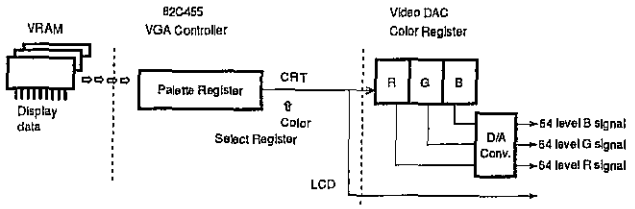


Fig. 4-10

Since the display to LCD of the PC-6220 is not through the Video DAC as shown in Fig. 4-10, the application software using Video DAC will only be effective to CRT.

4-5-4. Display toning for PC-6220

The PC-6220 is capable to display 16 toning and selects the tone by giving the each toning data to the palette register.
The following method is used for managing 16 kinds of tone for the PC-6220.

In case of 16 tones, the basic frame frequency is normally 15 times. ON and OFF action of 1-dot on the LCD is made at the cycle 0/15, 1/15, 2/15 ..... 15/15. However, because of the characteristic of the LCD, the display flickering is unavoidable at the cycle time of 1/15.
To reduce the flickering for PC-6220, the following measures are taken;

1) Increases frame frequency
2) Increases basic cycle time
3) Shifts the ON/OFF cycle of neighboring dots

Even the above measures are taken for PC-6220, there are still little flickering existed as follows;

1) Because of 16 toning, it is unavoidabel to have some part of flickering tone.
2) It is not possible to shift the ON/OFF cycle of neighboring dot in the tile pattern display mode, therefore, at this mode, little flickering are shown.
3) Low resolution mode like 320 dots in width, 2 × 2 dots are used to display 1 dot on the LCD, since 2 × 2 dots make ON/OFF action at the same time. Thus, the flickering is noticeable.

4-5-5. Compensation capability

The resolution of the PC-6220 LCD is 640 × 480 dots though, only 640 × 400 dots resolution is used for text mode. In this case, all the dots of LCD is not used by doing centering operation.
Also, PC-6220 is capable to handle a full screen of 640 × 480 dots at Expanded mode of LCD.

The above function is called "Compensation capability", and there are two types of compensations. One is text compensation, and the other is graphic compensation. Text compensation is displayed in Fig. 4-11, and graphic compensation is in Fig. 4-11.

[Text Compensation]

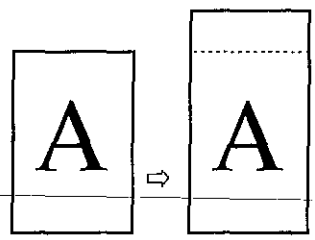


Fig. 4-11

At text mode, the 350 or 400 lines horizontal resolution is compensated by enlarging the most upper line of the character font.

However, since most CG fonts used in Europe countries, use the upper line is used also as character data. Therefore, if this method is applied to those fonts, the compensated character is changed to non-existed wrong character. The PC-6220 does not use this method actually.

[Graphic Compensation]

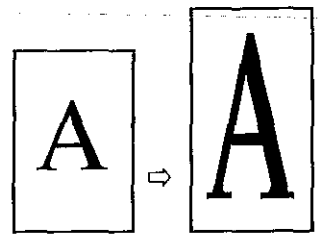


Fig. 4-12

The horizontal resolution is enlarged by duplicatelyduplicately 1-line per several lines over on all the screen. In this case however, since the duplicated line not always sets in between two characters. If a duplicated line sits on a character, the characterlooks distored.

The graphic compensation function is originally used for gaphic mode though,also used for text mode for PC-6220.

4-5-6. Conventional CRT support (clock switching)

In VGA mode, analog CRT is used to present the beautiful color but in another mode CGA/MDA), digital (conventional) CRT is needed. In order to support these CRTs, clock pulses can be changed by the signal from 82C455 ($\overline{\text{ERMEN}}$ signal) Refer to Fig. 4-13.

When $\overline{\text{ERMEN}}$ signal is HIGH,
28.322 MHz (for VGA monitor)
25.175 MHz (for EGA monitor) are selected.

When $\overline{\text{ERMEN}}$ signal is LOW
16.257 MHz (for MDA monitor)
14.31818 MHz (for CGA monitor) are selected.

The $\overline{\text{ERMEN}}$ signal is set by the BIOS according to the CRT type assigned in the SETUP menu.

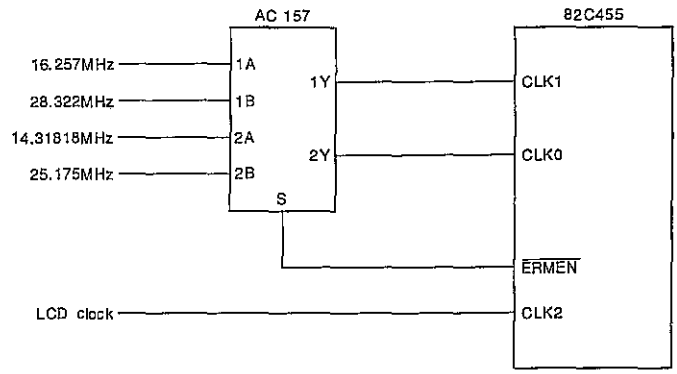


Fig. 4-13 clock switching

4-5-7. Address/Data multiplexer

The 82C455 uses several pins for address/data to reduce the number of the pins. So the address/data multiplexer is needed.
(Refer to Fig. 4-14)

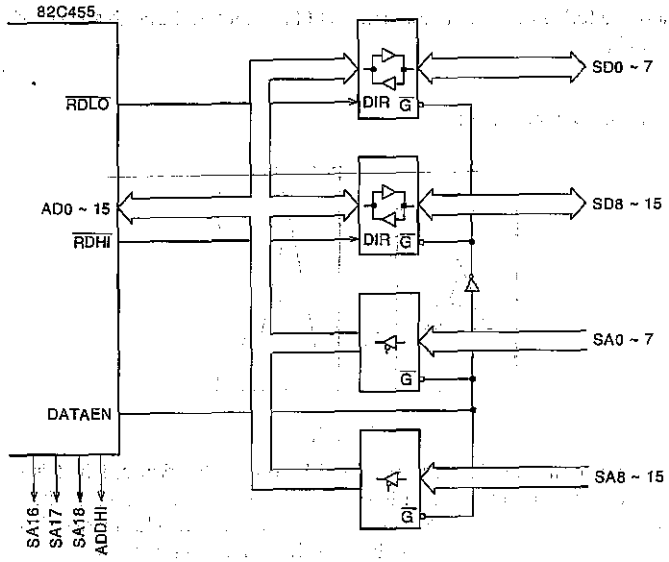


Fig. 4-14
Address/data multiplexer

4-6. Description of black/white liquid crystal backlight inverter (type: IV18106)

4-6-1. General

This PWB unit is employed to drive the LCD backlight (cold cathode ray tube) which will be directly installed to the plastic cabinet inside the display. Three connectors are used for the I/O and control signal interfacing.

NOTES:
1. This unit drives the entire backlight circuit with the power supply only, except that it is connected with an external VR and control lines.
2. Since it is an assembly unit, parts replacement and repair are not allowed. In case it has to be replaced with a new one, unfasten the connectors and remove screws.
3. Pay attention to a high tension voltage of 1000V on the secondary side when operating. For wires that are exposed over and below the transformer, these must be treated with care as it may result in wire breakage.
4. Since this unit is compact and low profile, the board height is low, width narrow, and long in the longitudinal direction, it would be liable to damage if subjected to twisting. So, never drop or twist it to avoid possible damage.

4-6-2.Electrical characteristics

(1) Maximum allowable ratings

Parameter	Symbol	Rating
Input voltage	Vin	16V
Input power	Pin	3.6W
Operating temperature	Ta	0~50°C
Storage temperature	Ts	-20~75°C
Operating humidity	RH	80% with maximum wet ball humidity at 35°C

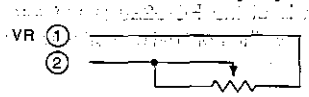
Table 4-37

(2) Electrical characteristics

Parameter	Symbol	Nominal	Note
Input voltage	Vin	DC12V	(9.0~16.0V)
Input current	Iin	0.24A	Lamp load Vin=12V, VR=0Ω
No-load release voltage	Vs	AC100Vrms	
Tube current	IL	5.0mA	
Oscillation frequency	f	65kHz	
Chipping frequency	fch	60kHz	

Table 4-38

The following circuit is used for intensity adjustment.



(3) Connector pin layout

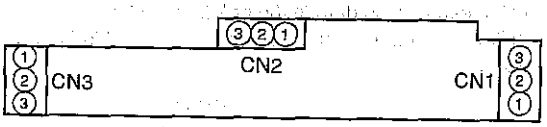


Fig. 4-15
PWB top view

(a) CN1 pin configuration

Pin No.	Signal name	Symbol
①	GND.	GND.
②	N.C	
③	OUT	OUT

(b) CN2 pin configuration

Pin No.	Signal name	Symbol
①	+B supply	+B
②	N.C	
③	GND.	GND.

(c) CN3 pin configuration

Pin No.	Signal name	Symbol
①	Intensity control VR	VR
②	GND.	GND.
③	Control	CONT

4-6-3. Circuit diagram

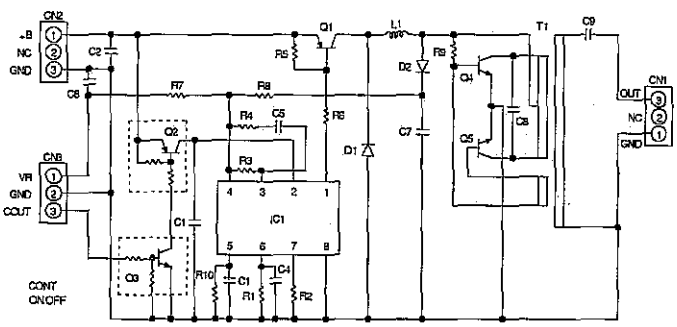


Fig. 4-16

CHAPTER 5. HDD

5-1-1. Introduction

The Hard disk drive (HDD) is a 2.5 inch ruggedized high performance disk drive optimized for an IBM PC-AT or XT compatible laptop or portable computer. The HDD contains an on-board controller with selectable interface that requires a simplified adapter board for interfacing to an AT or XT compatible bus.

5-1-2. Overview

This Manual describes the key features, specifications, characteristics, functional description and hardware and software considerations required to utilize the HDD in both the AT and XT interface modes.

5-1-3. Features

- Unique ramp loading mechanism for loading and unloading the disk heads during power-downs and periods of inactivity.
- User invoked low power modes and power-downs for power sensitive applications.
- High performance rotary voice coil actuator with embedded servo system.
- On-board controller for direct connection to a 50-pin interface.
- Microprocessor-controlled diagnostic routines that are automatically performed at power-up.
- Internal air filtration and dessicant system.
- Automatic error detection and correction.

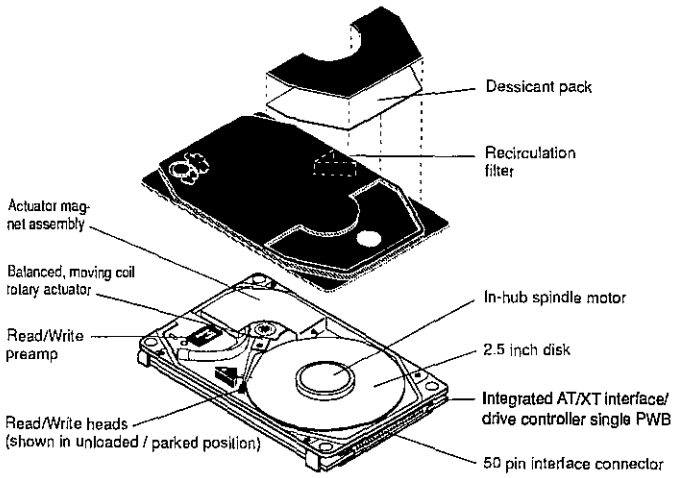


Fig. 5-1 HDD unit

5-1-4. Functional Description

The HDD contains all the necessary mechanical and electronic components to interpret control signals, properly position the recording heads, read and write data, and maintain a contaminant free environment for the disks and recording heads.

5-1-4-1. Read/Write and Control Electronic

The HDD has an integrated circuit attached to the flexible circuit connected to the actuator and read/write heads to provide one of two head selections, read preamplification, and write drive circuitry.

The microprocessor controlled circuit board provides the remaining electronic functions including:

- Read/Write Circuitry
- Rotary Actuator Control
- Interface Control
- Power Management
- Spin Speed Control
- Automatic Head Unloading

5-1-4-2. Drive Mechanism

The HDD has a spin speed of 3,307 RPM. The spin speed of the brushless DC direct drive spindle motor is maintained by using the motor in a synchronous mode.

Energy stored in the spindle motor is used to unload the read/write heads upon drive powerdown.

5-1-4-3. Head Positioner Mechanism

The two read/write heads of the HDD are directly attached to the actuator body which also supports the moving coil. The read/write heads are unloaded when the drive is spun down. This dynamically ramp loaded mechanism insures that the disk heads never come in contact with the disk media.

5-1-4-4. Read/Write Heads and Disks

Data is recorded on a 65mm diameter disk through two 3370 type heads.

5-1-4-5. Air Filtration System

The HDD HDA breathes through a high efficiency ambient filter. A high flow recirculative filter maintains a clean environment of better than class 100 for the head and disk enclosure.

5-1-4-6. Error Correction

The HDD performs internal error correction through the use of a polynomial capable of correcting one error burst with a maximum of 11 bits per 512 byte block.

5-1-4-7. Customer Options

The host interface on the HDD can be set to run on either an AT or XT compatible system. The polarity of Pin 44 on the interface will determine XT or AT operation (+ AT, – XT).

In AT mode, the HDD can operate as a single drive or in a dual drive (master/slave) configuration. The jumper trace E1 is shorted from the factory indicating a single drive or the master. In a dual drive configuration, the E1 trace must be cut to indicate the second drive or slave. The trace is shown in the following drawing.

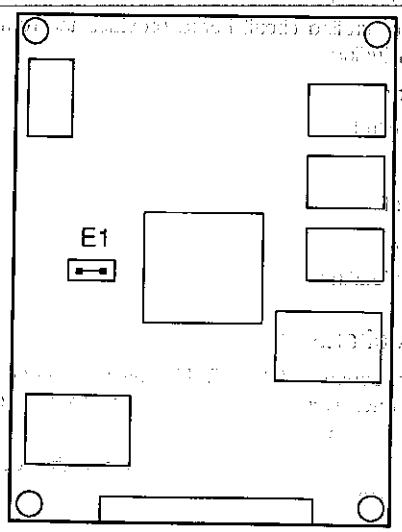


Fig. 5-2

The XT mode does not support dual dive master/slave configurations. The E1 jumper trace should not be cut.

5-1-4-8. Diagnostic Routines

Upon power up the microprocessor circuitry of the HDD performs diagnostics. If an error is detected the drive will not come ready.

5-1-4-9. Spin-Up/Down Operations

When power is applied to the drive, it will perform its diagnostics and come ready. To conserve power, it will accept commands, but will not spin up until it receives a command requiring a disk access (such as a Read, Write, Seek, Recal, etc.).

When spinning up for the first time after application of power, it will spin up and do a servo calibration which requires a total time of 4 seconds. Subsequent spin up from power down modes do not require calibration and will be completed within 2 seconds.

When the drive is in the process of spinning down, there is no minimum stop time required before another command can be issued and accepted. It takes 250ms (max) for the heads to become securely parked on the ramp after a spin down condition is generated.

5-1-4-10. Compatibility

The Hard disk drive powers up in the translate mode of 615 cylinders, 4 heads, 17 sectors. To utilize the Native mode of 615 cylinders, 2 heads, 34 sectors the BIOS must send the appropriate parameters during the Initialize Drive Parameters command (refer to the chapter concerning command descriptions).

5-2. Specifications Summary

5-2-1. Capacity

Formatted	21.4 MBytes

5-2-2. Configuration

Actuator Type	Rotary Moving Coil
Number of Disks	1
Data Surfaces	2
Data Heads	2
Servo System	Embedded
Tracks per Surface	615
Track Capacity	17,408 bytes
Bytes per Block	512
Blocks per Track	34
Blocks per Drive	41,820

5-2-3. Performance

Seek Times	
Track to Track	8ms
Average	23ms
Maximum	45ms
Average Latency	9.1ms
Rotation Speed	3,307 RPM
Controller Overhead	1ms
Data Transfer Rates	
To/From the Buffer-	
Burst (max)	5.50MB/sec
Sustained	4.25MB/sec
To/From the Media	1.25MB/sec
Start Time	2 sec (typical)
Stop Time	NA (refer to functional description)
Interleave	Programmable

5-2-4. Read/Write

Interface	AT or XT 50 pin
Recording Method	2 of 7 RLL Code
Track Density	1,350 TPI
Recording Density (ID)	38,452 BPI
Flux Density (ID)	25,634 FCI

5-2-5. Power Requirements

Typical Power Dissipation	
Spin Up	3.50 watts (peak)
Ready	1.10 watts (peak)
Seeks	1.25 watts
R/W	2.50 watts
Power Save Mode	0.70 watts
Standby Mode	0.05 watts

DC Input

+5 Volts±5% D.C., 1 amp max. Maximum ripple allowed is 2% with equivalent resistive load

5-2-6. Physical Characteristics

Outline Dimension	0.60"x2.75"x4.00" (15.2mmx69.9mmx101.6mm)
Weight	6.35 ounces (180 grams)

5-2-7. Environmental Characteristics

Temperature	
Operating	5°C to 55°C
Non-Operating	–40°C to 70°C
Thermal Gradient	20°C/hour max
Humidity	
Operating	10% to 90% non-condensing
Non-Operating	10% to 90% non-condensing
Max Wet Bulb	30°C
Altitude (relative to sea level)	
Operating	–1000 to 10,000 feet
Non-Operating (max.)	40,000 feet

5-2-8. Reliability and Maintenance

MTBF	20,000 POH
MTTR	5 minutes typical
Start/Stops	250,000
Preventive Maintenance	None
Component Design Life	5 years
Data Reliability	<1 non-recoverable error in 10^{12} bits read

5-2-9. Shock and Vibration

Shock	(1/2 sine pulse, 11 ms duration)
Non Operating	100G
Operating	5G
Vibration	(swept sine, 1 octave per minute, 10–400Hz)
Non Operating	5G peak to peak
Operating	1G peak to peak
	(without non-recoverable errors)

5-2-10. Magnetic Field

An externally induced magnetic flux density may not exceed 10 gauss as measured at the external drive surface.

5-2-11. Acoustic Noise

Sound pressure level at 1 meter –39 dBA.

5-2-12. Safety Standards

The Hard disk drive is designed to comply with relevant product safety standards such as:

UL 478 Electronic Data Processing Units and Systems

CSA C22.2 No. 154 Data Processing Equipment

VDE 0804 Regulations for Telecommunications Apparatuses including Information Processing Equipment

IEC 435 Safety Requirements for Data Processing Equipment

5-2-13. Mounting Configurations

The features which allow greater shock and vibration tolerance include the dynamically loaded heads, a fully balanced rotary actuator, and the low overall mass and weight of the drive and moving masses.

The drive may be mounted in any attitude. It can be mounted either from the side or the bottom using four M2X.4 screws as shown in Fig. 5-3.

Adequate ventilation must also be provided to the drive to ensure reliable operation over the specified operating temperature range.

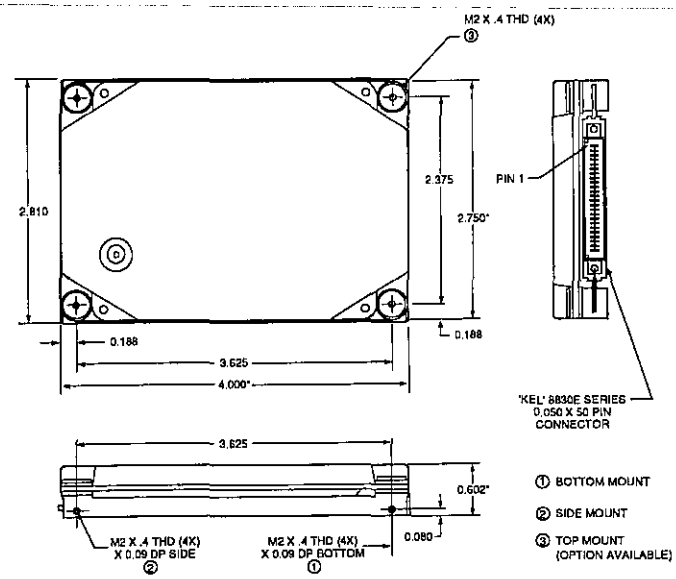


Fig. 5-3 Mounting Specifications/Dimensions

5-3-1. Signal description

The following table describes all of the pins on the 50 Pin Interface Connector (J1) in AT Mode. AT Mode is designated by pin 44.

I/O PIN	SIGNAL	I/O PIN	SIGNAL
01	–HOST RESET	02	GND
03	+HOST DATA 7	04	+HOST DATA 8
05	+HOST DATA 6	06	+HOST DATA 9
07	+HOST DATA 5	08	+HOST DATA 10
09	+HOST DATA 4	10	+HOST DATA 11
11	+HOST DATA 3	12	+HOST DATA 12
13	+HOST DATA 2	14	+HOST DATA 13
15	+HOST DATA 1	16	+HOST DATA 14
17	+HOST DATA 0	18	+HOST DATA 15
19	GND	20	KEY
21	Not Used	22	GND
23	–HOST LOW	24	GND
25	–HOST IOR	26	GND
27	Not Used	28	Not Connected
29	Not Used	30	GND
31	+HOST IRQ	32	–HOST IO16
33	+HOST ADDR1	34	–HOST PDIAG
35	+HOST ADDR0	36	+HOST ADDR2
37	–HOST CS0	38	–HOST CS1
39	–ACTIVE	40	GND
41	+5V Supply	42	+5V Supply
43	+5V Return	44	+AT/–XT
45	+5V Return	46	+5V Supply
47	+5V Return	48	+5V Supply
49	+5V Return	50	+5V Supply

SIGNAL NAME	DIR	PIN	DESCRIPTION
–HOST RESET	O	01	Reset signal from the Host system which is active low during power up and inactive thereafter.
GND	—	02	Ground between the drive and the Host.
+HOST DATA	I/O	03–18	16 bit bi-directional data bus between the Host and the drive. The lower 8 bits HD0 – HD7 are used for register & ECC byte access. All 16 bits are used for data transfers. There are tri-state lines with 24 ma drive capability.
GND	—	19	Ground between the drive and the Host.
KEY	—	20	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
Not Used	—	21	Not Used
GND	—	22	Ground between the drive and the Host.
–HOST IOW	O	23	Write strobe, the trailing edge of which clocks data from the Host data bus, HD0 through HD15, into a register or the Data register of the drive.
GND	—	24	Ground between the drive and the Host.
–HOST IOR	O	25	Read strobe, which when low enables data from a drive register onto the Host data bus, HD0 through HD15. The trailing edge of –HOST IOR latches data from the drive at the Host.
GND	—	26	Ground between the drive and the Host.
Not Used	—	27	Not used
Not Connected	—	28	Not connected
Not Used	—	29	Not used
GND	—	30	Ground between the drive and the Host.
+HOST IRQ	I	31	Interrupt to the Host system, enable only when the drive is selected, and the Host activates the -IEN bit in the Digital Output register. When the -IEN bit is inactive high, or the drive is not selected, this output in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by drive microcontroller. IRQ is reset to zero by a Host read of the Status register or a write to the Command register. This signal is a tri-state line with 24 ma drive capacity.
–HOST IO16	I	32	Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 20 ma drive capacity.
–HOST PDIAG	I	34	Passed diagnostic. Output by the drive if it is the slave drive. Input to the drive if it is the master drive. This low true signal indicates to a master that the slave has passed its internal diagnostic command.
+HOST A0,A1,A2	O	35,33, 36	Three bit binary coded address lines used to select the individual registers in the task file.
–HOST CS0	O	37	Chip select decoded from the Host address bus. Used to select low-order Host accessible registers.
–HOST CS1	O	38	Chip select decoded from the Host address bus. Used to access the three high order registers in the Task File.
–ACTIVE	I	39	Signal from the drive used to drive an active LED whenever the disk is being accessed. This signal is active low when the drive is busy and has a drive capability of 48 ma.
GND	—	40	Ground between the drive and the Host.
+AT/–XT		44	When connected to +5V or left open this signal will enable AT Mode.
+5V SUPPLY		41,42, 46,48, 50	+5V Volt drive supply
+5V RETURN		43,45, 47,49	+5V Volt P.S. ground

5-4-1. POWER COMMANDS

- At any given time the drive can be in one of three power modes:
  Active: The drive is either reading, writing, seeking, or is ready and idle on track awaiting the next command.
  Power Save: The drive is spinning, the heads are over the media but not necessarily on track. To recover typically requires 100 ms.
  Standby: The drive is spun down. Typically 2 seconds are required to recover from this mode.
- Commands are available to move between the modes as required to reduce power consumption.

Chapter 6. LCD (LM64N671)

6-1. Structure

Structure: The 640 x 480 full dot liquid display graphic display unit consists of an LCD panel, electronic component printed circuit board, and the film carrier LSI that electrically connected.

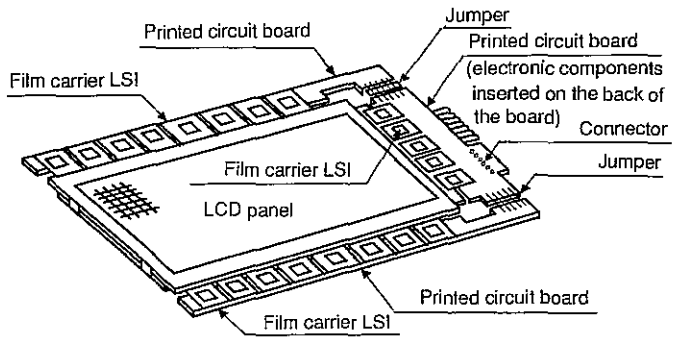


Fig. 6-1

6-2. BLOCK DIAGRAM

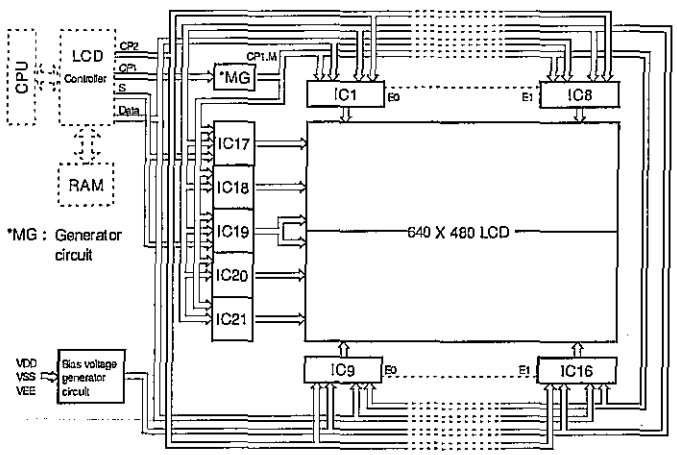


Fig. 6-2

6-3. Specification

Tbl. 6-1

Item	Characteristics	Unit
⁎1 Physical dimensions	244(W) x 195(H) x 7MAX(D)	mm
Effective display area	205(W) x 155(H)	mm
Display format	640(W) x 480(H) full dot	–
Dot size	0.28 x 0.28	mm
Dot space	0.03	mm
⁎2 Dot color	White ⁎3	–
⁎2 Background color	Black	–
Weight	About 240	g

⁎1: The physical dimensions of the unit excludes the LCD sealed portion.

⁎2: The color of the LCD panel may vary according to the environmental temperature due to the characteristic of the LCD panel.

⁎3: Data "H" → ON=white
Data "L" → OFF=black
When the RV line is open.
Negative logic is established when the RV line is connected to the VDD line.

6-4. Absolute maximum rating

(1) Absolute electrical maximum rating

Tbl. 6-2

Item	Symbol	Minimum	Maximum	Unit	Note
For logic circuit	$V_{DD} - V_{SS}$	0	6.0	V	Ta = 25°C
For liquid crystal drive circuit	$V_{DD} - V_{EE}$	0	33.0	V	Ta = 25°C
Input voltage	V_{IN}	0	V_{DD}	V	Ta = 25°C
For liquid crystal drive	$V_{DD} - V_O$	0	28.0	V	Ta = 25°C

(2) Environmental requirements

Tbl. 6-3

Item	Storage		Operating		Note
	Minimum	Maximum	Minimum	Maximum	
Temperature	–25°C	+60°C	0°C	+45°C	
Humidity	NOTE(1)		NOTE(1)		Free of moisture condensation

NOTE(1): Ta ≦ 40°C . . . 95%RH, max.
Ta > 40°C . . . Absolute humidity must be 59%RH with Ta=40°C.

6-4. Electrical characteristics

(1)

Tbl. 6-4

Ta = 25°C, V_{DD} = 5V ± 5%

Item	Symbol	Condition	Minimum	Maximum	Unit	Note
For logic circuit supply voltage	$V_{DD} - V_{SS}$		4.75	5.0	5.25	V
For liquid crystal drive circuit supply voltage	$V_{DD} - V_{EE}$		TBD	TBD	TBD	V
Liquid crystal drive voltage	$V_{DD} - V_O$	(NOTE)	18.0	21.2	25.7	V
Input voltage	V_{IN}	High level	0.8V_{DD}	–	V_{DD}	V
		Low level	0	–	0.2V_{DD}	V
Input leak current	I_{IL}	High level	–	–	25	µA
		Low level	–25	–	–	µA
For logic circuit supply current	I_{DD}	V_{DD}=5V, V_{DD}–V_O=F=75Hz 21.2V High frequency pattern	–	25	35	mA
For liquid crystal circuit supply current	I_{EE}		–	15	25	mA
Power consumption	Pd		–	600	900	mW

NOTE: The view angle (θ) of a maximum contrast may be obtained by changing the liquid crystal drive voltage (V_{DD}–V_0).
Maximum and minimum limits of the rating show the maximum and minimum voltages at the operating temperature range (0°C~45°C).
"Standard" shows the nominal voltage.

(2) Input capacity

Tbl. 6-5

Signal name	Input capacity
S	40pF TYP
CP1	250pF TYP
CP2	200pF TYP
UD0~UD3	200pF TYP
LD0~LD3	200pF TYP

(3) Interfacing signals

[1] Connector 1 (IL-Y-15P-S15L2-EF)

Pin No.*	Symbol	Function	Active signal level
1	S	Scan start	"H"
2	CP1	Input data latch	H→L
3	CP2	Data input lock	H→L
4	BLoff	Backlight control	Connected with the pin-2 of connector 2
5	V_{DD}	Logic circuit power supply (+5V)	–
6	V_{SS}	Ground potential	–
7	V_{EE}	Liquid crystal drive power supply (–)	–
8	DUO	Display data (upper half)	H(ON), L(OFF)
9	DU1	"	"
10	DU2	"	"
11	DU3	"	"
12	LD0	Display data (lower half)	H(ON), L(OFF)
13	LD1	"	"
14	LD2	"	"
15	LD3	"	"

Tbl. 6-6

[2] Connector 2 (IL-Y-5P-S15L2-EF)

Pin No.*	Symbol	Function	Active signal level
1	RV	Logic reverse control signal	Open or shorted with VDD
2	BLoff	Backlight control	Connected with the pin-4 of connector 1
3	V_{DD}	+5V	Must be connected with the contrast calibration circuit.
4	V_0	Liquid crystal drive voltage	
5	V_{EE}	Liquid crystal supply voltage (–)	

Tbl. 6-7

6-5. Driving method

1) Circuit configuration

Fig.6-2 shows the block diagram of the circuit configuration.

2) Display configuration

To obtain high contrast display by decreasing the duty, the area of 640 x 480 dots display is divided into two sectors, each sector (640 x 240 dots) is driven by 1/240 duty.

3) Input data and control signals

The LCD driver is 80-bit LSI that consists of latch circuit and LCD drive circuit.

A 4-bit parallel data is supplied to one line (640 dots) of both display sectors at a time, starting from the upper left corner of the display, via the shift register with the clock pulse CP2.

Upon receiving one line input data (640 dots), 640 signals are latched as parallel data at a high to low transition of the latch signal CP1 to supply dot drive signals corresponding to 640 electrodes of the LCD panel.

Since the scan start signal S sent to the scan signal drive circuit has been transferred to the first line of the scan electrode, the contents of the data signals are displayed on the first line of the display screen by a combination of the LCD scan electrode and the voltage added to signal electrode.

While the first line display data are being displayed, the second line data are received. Upon transferring the 640 dots data and latched at a high to low transition of CP1, the second line data are now displayed.

When data transfer is repeated down to the 240th line in this manner using the multiplex mode from the upper to lower lines, a single cycle of a full data display (1 frame) is completed, then again starts to accept the data from the first line. The scan start signal S is a horizontal electrode drive signals.

To avoid display flicker for this model, the operation with the frequency shown in the table next is recommended.

If a DC voltage was added to the LCD panel, a chemical reaction takes place in the liquid crystal of the LCD panel which may result in LCD fatigue. The driving waveform must be reversed in a certain cycle to avoid the generation of such a DC voltage. This is performed by the async M signal circuit which converts the driving waveform into AC signal M.

Source frequency	50	60	50/60
Operating frequency	50±1	60±1	72±1

(Unit: Hz)

On account of the characteristics of the CMOS driver LSI, the power consumption of the unit increases proportionate to the increase of the CP2 clock frequency. Therefore, to decrease the CP2 clock data transfer speed, the driver LSI incorporates the system to 4 bits transfer parallel data through 4 shift registers. Use of this LSI abates the power consumption of the unit.

For this circuit configuration, a 4-bit display data are supplied from data input lines of UD0~3 for the upper half and DL0~3 for the lower half.

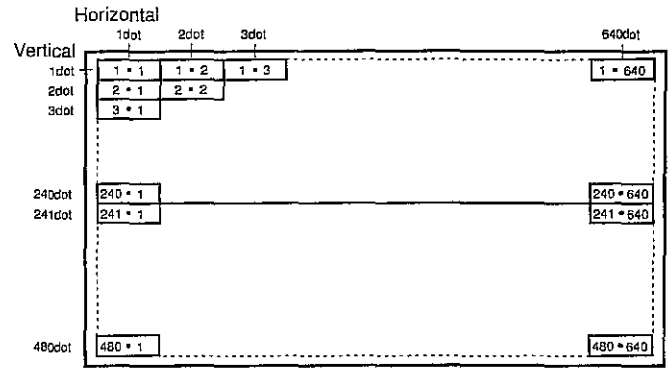
Aside from this, a data input bus line system is adopted for less power consumption. With this system, data inputs from LSI function only when appropriate data are sent.

The following shows the a full screen signal electrode data inputs and the driver LSI chip select functions.

First, when the driver LSI at the left is selected to send 80-dot data (20CP2), the right side driver close to it is selected. This action continues until the data have been sent to the driver LSI at the right. This process takes place at the same time with the signal electrode drive LSI for both screen sectors.

In this manner, data for both screen sectors are supplied through the 4-bit bus line one at a time.

Because this graphic display unit does not have the internal refresh RAM, it is necessary to supply the data and its timing pulse.



NOTE: 1·2 "1" represent the first vertical dot and "2" the second horizontal dot.

Fig. 6-5 Dot chart of Display Area

CHAPTER 7. POWER SUPPLY UNIT

7-1. Technical characteristics

1) Inputs

i) AC adaptor input

Rated voltage: 15.3V

Working voltage range: 14.24–16.5V

ii) Battery input

Rated voltage: 9.6v

Working voltage range: 8.0–12.8V

2) Outputs

i) Output

Circuit / name	5V Vcc	5V VBu1	–24V VLCD	*1 VBT
Rated load	2.12A	*2 0.1A	0.022A	2.7W

*1: VBT is an input voltage through circuit.

*2: VBul is battery backed up.
If Vcc is not, the load current is 0.01A.

ii) Recharge output

There are two modes of recharge; quick recharge and trickle recharge, which gets in action when the power is off to the personal computer.

Mode	Quick recharge	Trickle recharge
Charge current	0.78A	0.045A
Charge time	2 Hr	Continuous

7-2. Operational description

This DC/DC converter consists of two boards; one of which is the control PWB and the other is power supply PWB.

2-1) Input filter

Fig.7-1 shows the input filter.

It is a high pass type filter that consists of CL1, CL2, and C2. Noise on the input line, radio interference from within the converter, and conduction noise are suppressed in this circuitry.

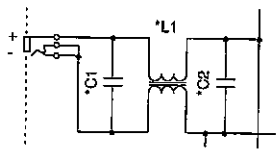


Fig. 7-1

2-2) 5V, VCC circuit

Fig.7-2 shows the 5V, VCC circuit.

8–16.5VDC supplied from the AC adaptor or the battery is dropped to 5V in TR4 to supply the regulated 5V. The transistor TR4 is switched at 110KHz using the control signal from IC1 of the control PWB to convert the DC input into high frequency square waveform, then rectified and smoothed by D2, L2, and C10.

To regulate the output voltage, a fluctuation in the supply line is detected and divided by means of the resistors R1, R2, and VR1 within the control PWB which is then sent to the comparator input in IC1 where the ON width of TR4 is controlled by the drive signal that error amplified by the error amp within IC1.

On and off of Vcc is controlled by CPU (IC5).

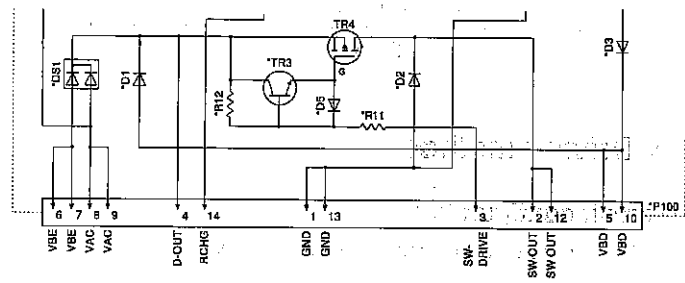


Fig. 7-2

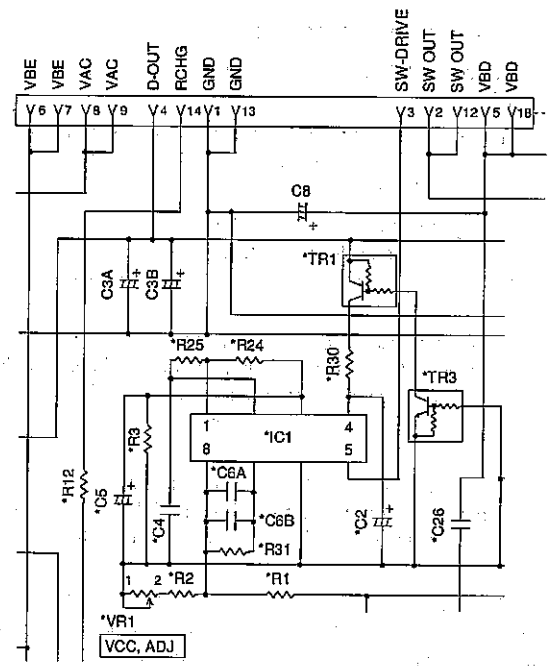


Fig. 7-3

2-3) 5V, VBu1 circuit

Fig.7-4 shows the 5V, VBu1 circuit.

For VBu1, the VCC output and the 3-pin regular IC3 outputs are OR-ed by the diode using DS1. If VCC was present, the VCC voltage is sent out straight. If not, output is obtained from IC3.

It has relationship of IC3 output < V_{CC}.

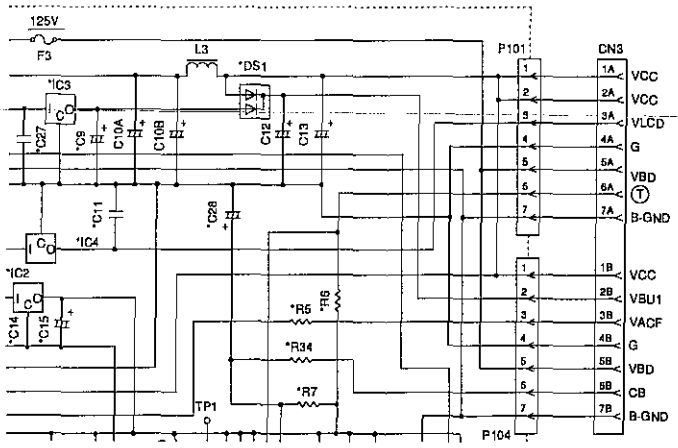


Fig. 7-4

2-4) –24V, VLCD circuit

Fig.7-5 shows the –24V, VLCD circuit.

Current flowing in the ON period of TR4 of the Vcc circuits charged in the primary circuit coil and released from the secondary circuit coil during the off period, to supply energy to the load.

A square waveform generated in the secondary side coil L2 is rectified and smoothed by D3 and C22 to obtain the DC current of about 40V. This then dropped to –24V by th 3-pin regulator IC4 to be used as the LCD power supply.

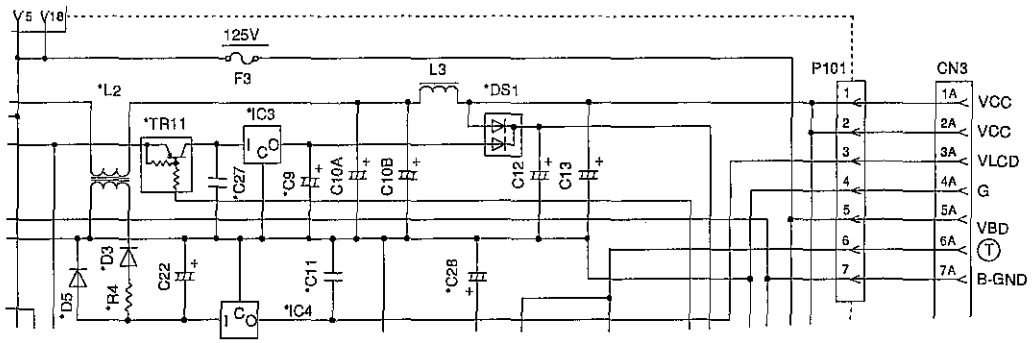


Fig. 7-5

2-5) VBT circuit

Fig.7-5 shows the VBT circuit.

VBT is an input through circuit from which derived the voltage same as the DC input. F1 is a short circuit protect fuse.

2-6) Recharge circuit

There are two types of the recharge circuits; the quick recharge circuit that operates when the switch S1 is off and the trickle recharge circuit which the current flows at all times during the time the AC adaptor is used.

i) Quick recharge circuit

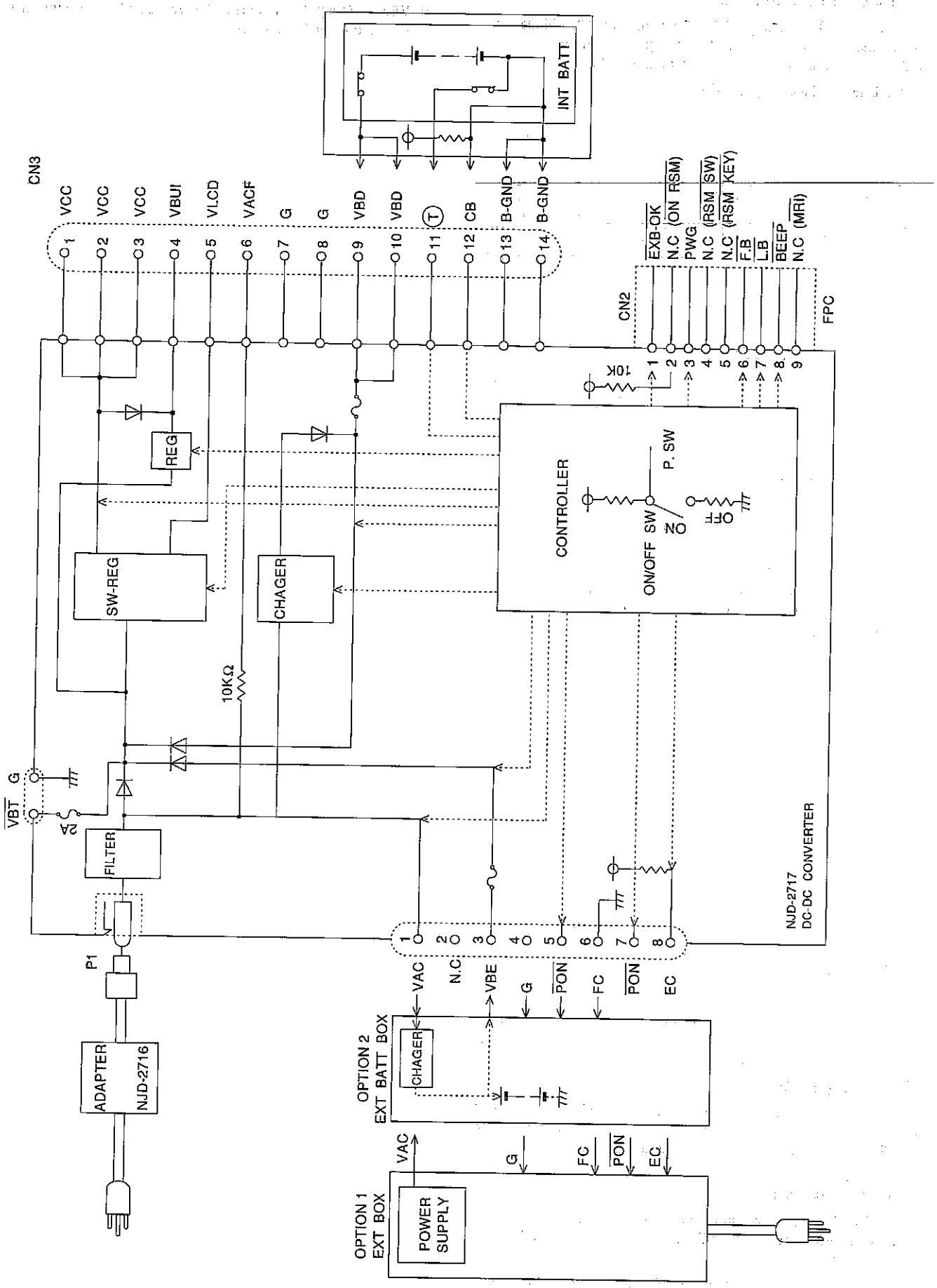
With the IC1 drive signal within the power supply PWB is switched at about 50KHz using TR1 which is then rectified and smoothed by D4, L1, and C3 to recharge the battery.

Recharge of the battery is entirely controlled by IC5 within the control PWB.

IC5 is a 4-bit microcomputer that not only controls battery recharge but handles signal transfer with the main unit.

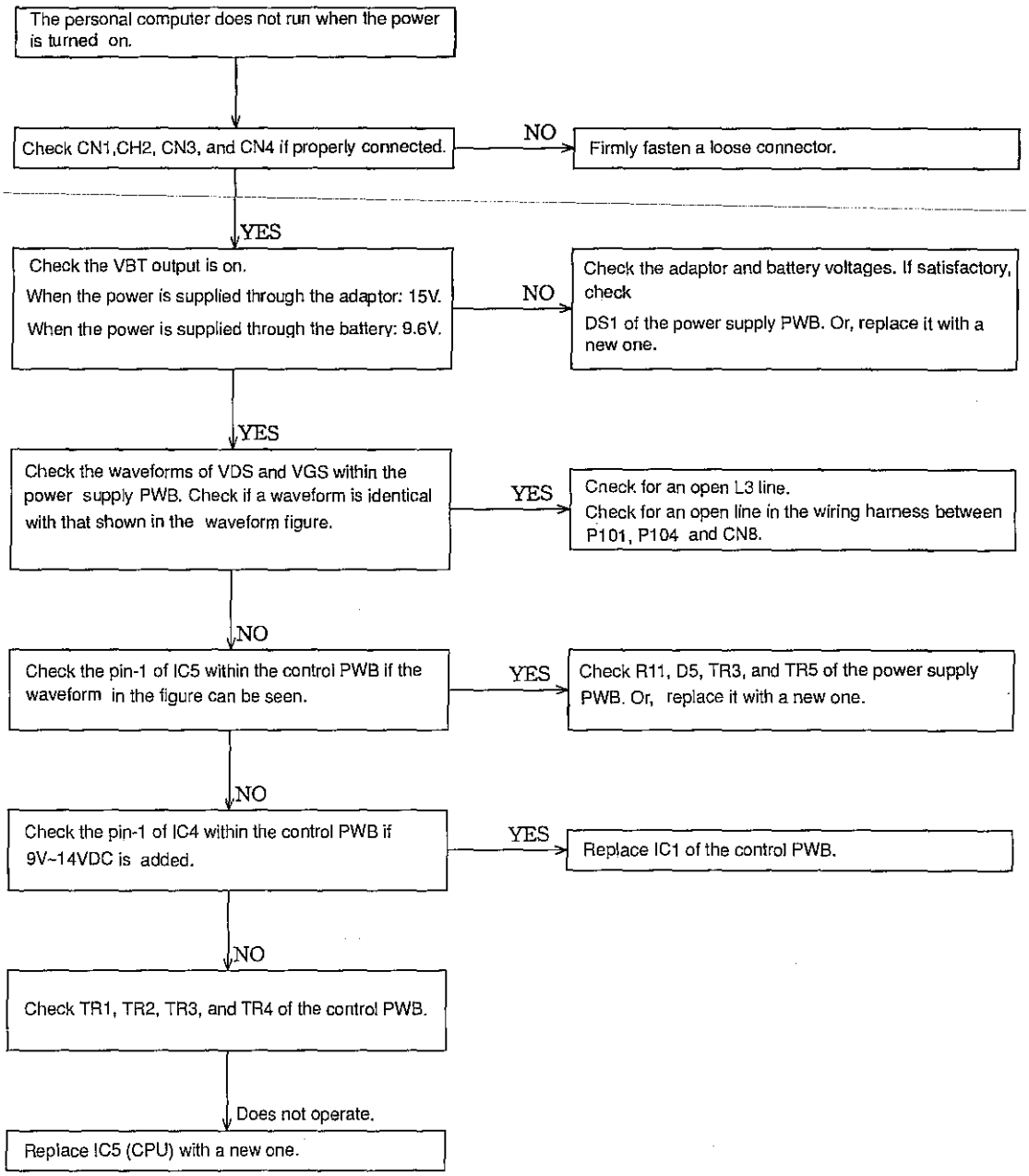
ii) When AC input is added to the AC adaptor, the current is kept supplied to the battery via R9.

2-7) Interface circuit and signals

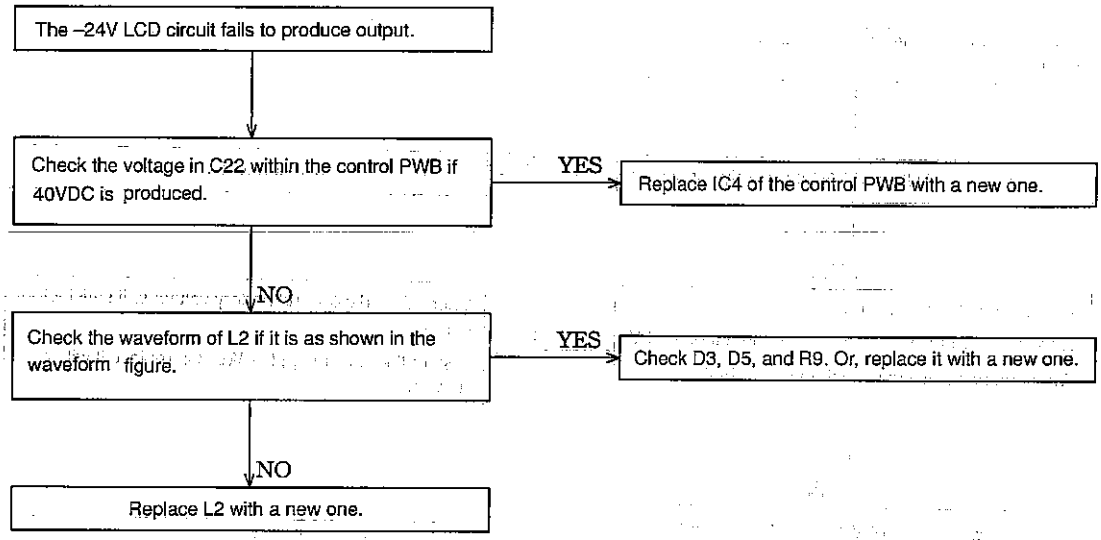


7-3. Troubleshooting

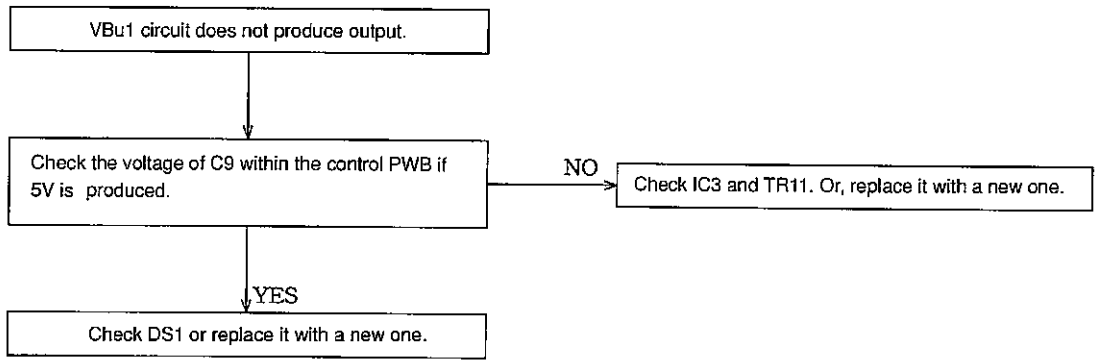
3-1)



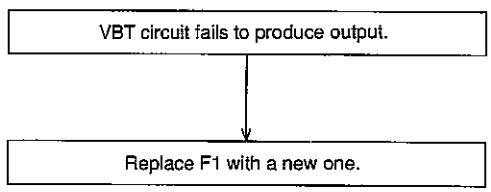
3-2)


The –24V LCD circuit fails to produce output.
Check the voltage in C22 within the control PWB if 40VDC is produced.
YES
Replace IC4 of the control PWB with a new one.
NO
Check the waveform of L2 if it is as shown in the waveform figure.
YES
Check D3, D5, and R9. Or, replace it with a new one.
NO
Replace L2 with a new one.

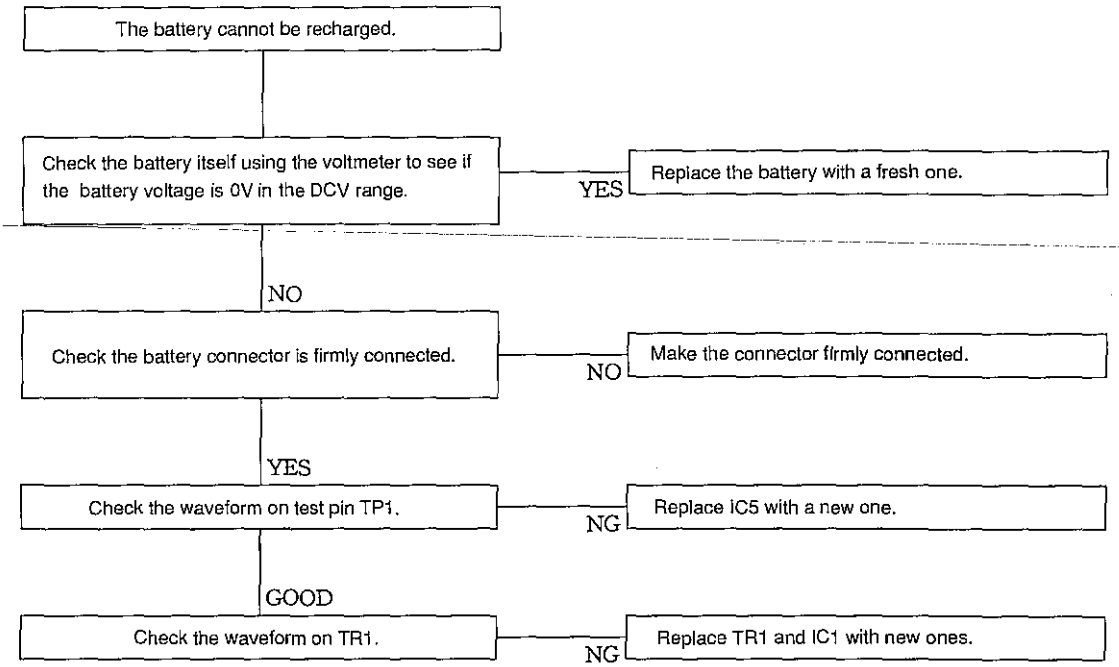
3-3)

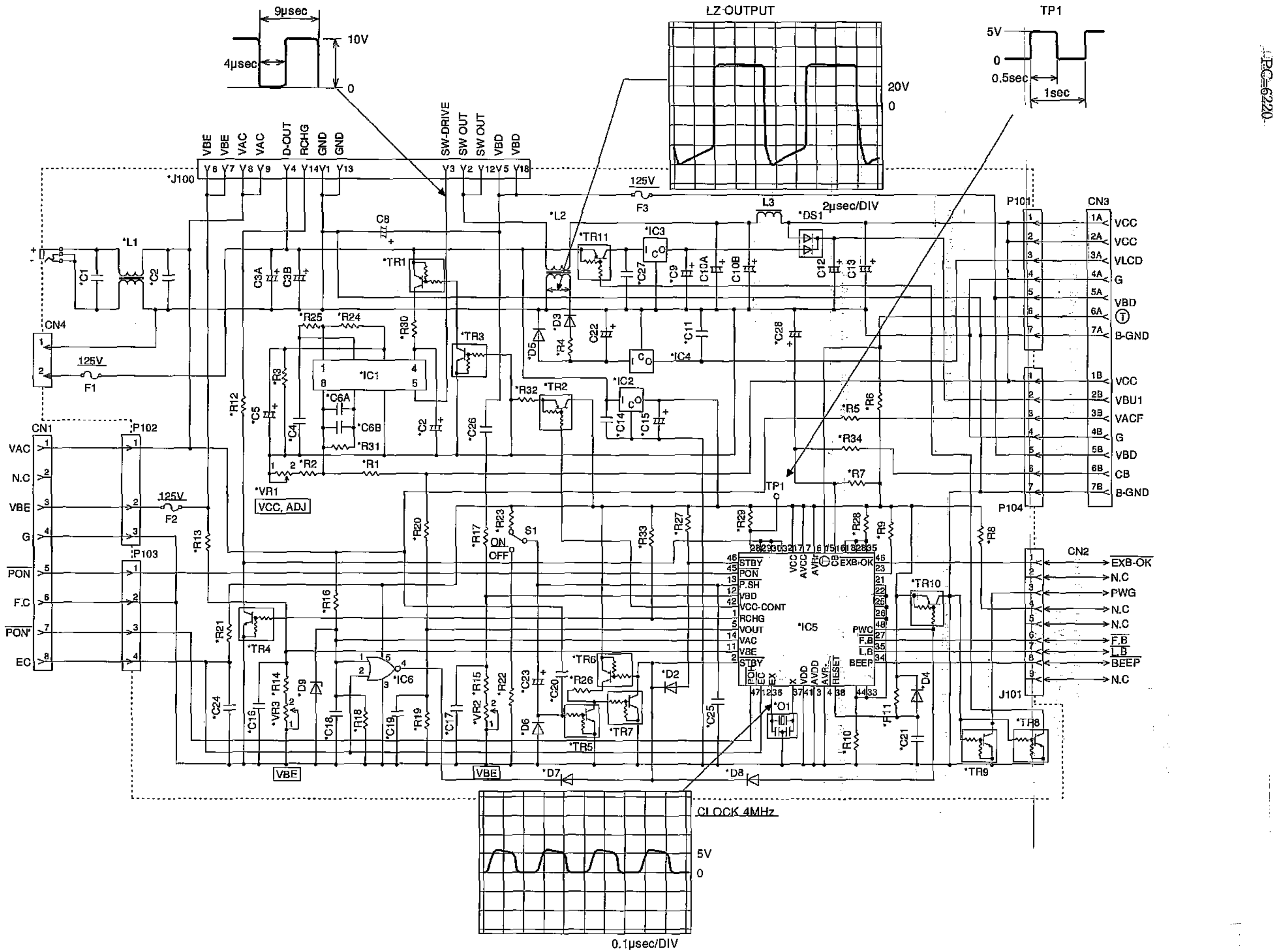

VBu1 circuit does not produce output.
Check the voltage of C9 within the control PWB if 5V is produced.
NO
Check IC3 and TR11. Or, replace it with a new one.
YES
Check DS1 or replace it with a new one.

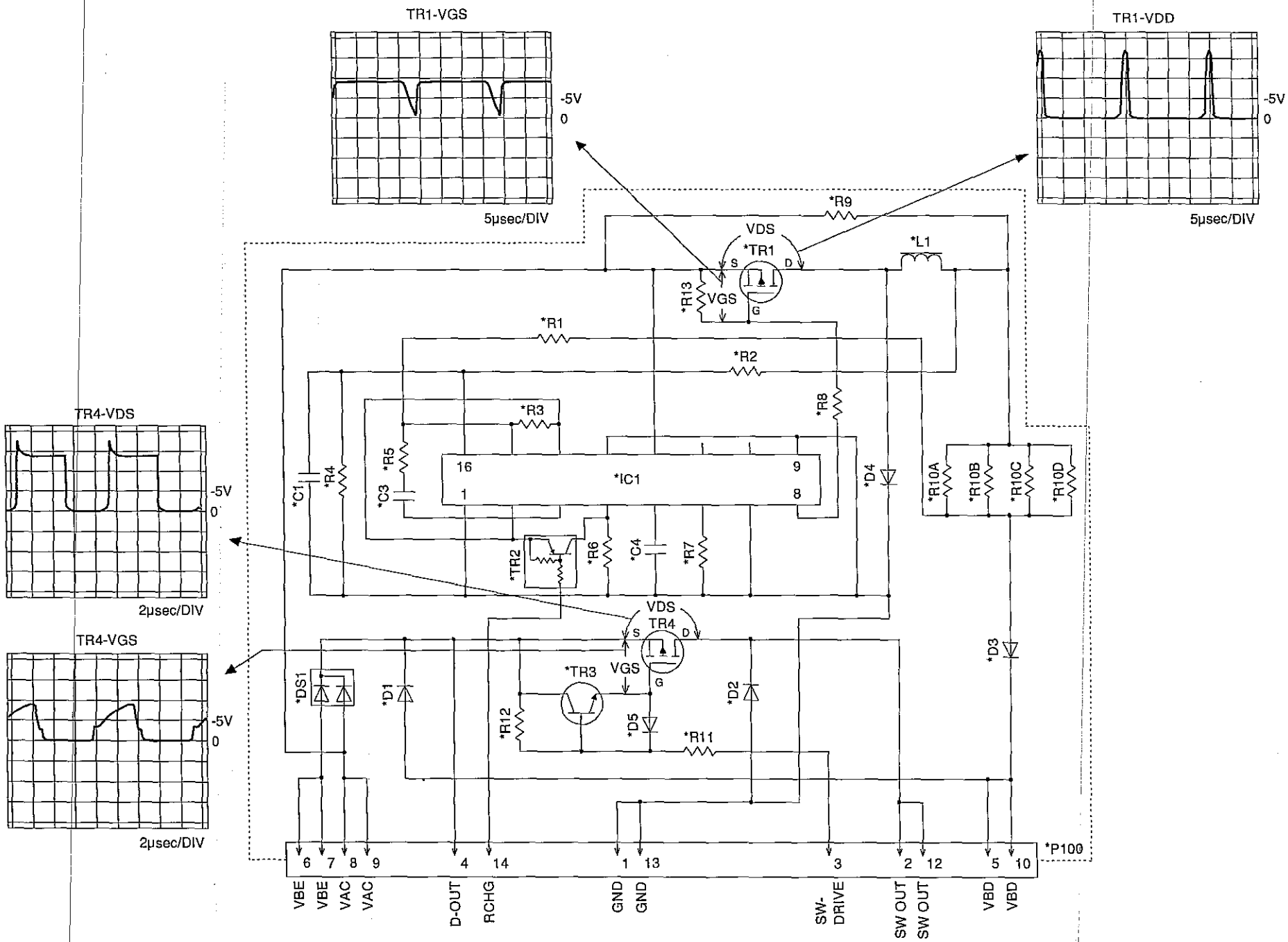
3-4)


VBT circuit fails to produce output.
Replace F1 with a new one.

3-5)


The battery cannot be recharged.
Check the battery itself using the voltmeter to see if the battery voltage is 0V in the DCV range.
YES
Replace the battery with a fresh one.
NO
Check the battery connector is firmly connected.
NO
Make the connector firmly connected.
YES
Check the waveform on test pin TP1.
NG
Replace IC5 with a new one.
GOOD
Check the waveform on TR1.
NG
Replace TR1 and IC1 with new ones.


9μsec
4μsec
10V
0
LZ OUTPUT
20V
0
2μsec/DIV
TP1
5V
0
0.5sec
1sec
VBE
VBE
VAC
VAC
D-OUT
RCHG
GND
GND
SW-DRIVE
SW OUT
SW OUT
VBD
VBD
*J100
125V
F3
L3
*DS1
*L2
*TR11
*IC3
P101
CN3
VCC
VCC
VLCD
G
VBD
B-GND
VCC
VBU1
VACF
G
VBD
CB
B-GND
P104
*L1
*C1
*C2
C8
*TR1
C3A
C3B
C27
*C9
C10A
C10B
C12
C13
CN4
125V
F1
*R25
*R24
*R30
*TR3
*IC1
*D5
*D3
*R4
C22
*C11
*IC4
*C28
*IC2
*C14
*C15
*R6
*R5
*R34
*R7
*C6A
*C6B
*R31
*C5
*R3
*R12
*C4
*C26
*R32
*TR2
CN1
VAC
N.C
VBE
G
PON
F.C
PON'
EC
P102
P103
125V
F2
*R2
*R1
*VR1
VCC, ADJ
TP1
*R13
*R20
*R17
*R23
ON
OFF
S1
*R33
*R27
*R29
*R28
*R9
*R8
CN2
EXB-OK
N.C
PWG
N.C
N.C
F.B
L.B
BEEP
N.C
J101
STBY
PON
P.SH
VBD
VCC-CONT
RCHG
VOUT
VAC
VBE
STBY
*IC5
EXB-OK
PWG
F.B
L.B
BEEP
VCC
AVCC
AVR+
CB
POH
EC
EX
X
VDD
AVDD
AVR-
RESET
*TR10
*R16
*R21
*TR4
*IC6
*C24
*C16
*R14
*VR3
*D9
*C18
*R18
*C19
*R19
*C17
*R15
*VR2
*R22
*C23
*C20
*R26
*TR6
*D2
*D6
*TR5
*TR7
*C25
*O1
*R10
*R11
*D4
*C21
*TR9
*TR8
VBE
VBE
*D7
*D8
CLOCK 4MHz
5V
0
0.1μsec/DIV


TR1-VGS
-5V
0
5µsec/DIV
TR1-VDD
-5V
0
5µsec/DIV
TR4-VDS
-5V
0
2µsec/DIV
TR4-VGS
-5V
0
2µsec/DIV
*R9
VDS
*TR1
S
D
G
VGS
*R13
*L1
*R1
*R2
*R3
*R8
*C1
*R4
*R5
*C3
16
1
*IC1
9
8
*D4
*R10A
*R10B
*R10C
*R10D
*TR2
*R6
*C4
*R7
VDS
TR4
S
D
G
VGS
*TR3
*D3
*DS1
*D1
*D2
*R12
*D5
*R11
*P100
6 7 8 9
4 14
1 13
3
2 12
5 10
VBE
VBE
VAC
VAC
D-OUT
RCHG
GND
GND
SW-DRIVE
SW OUT
SW OUT
VBD
VBD

CHAPTER 8. KEYBOARD (CE-621NK)

8-1. Input/output data

1) Start/stop, half-duplex transfer mode for the clock and data lines.

2) Transfer format

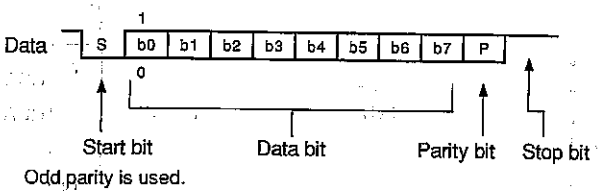


Fig. 8-1

3) Transmit rate

For both send and receive, it depends on the clock signal sent from the keyboard which will be 14300bps.

4) Output

The output (data, clock) is directly connected with the 80C52 controller.

8-2. Data send/receive control

Prior to sending and receiving of data on the keyboard, the clock and data lines are checked of their conditions.

Clock	Data	
1	1	Keyboard data ready to send
1	0	Keyboard data receive request
0	0 or 1	Send/receive disabled
0 ... Low		1 ... High

NOTE: After completion of the keyboard data, "1" is sent onto the clock and data signal lines.

1) Keyboard data output (KB→Host)

If there is data in the keyboard internal buffer with a high state of clock and data, these signals are driven in the timing shown separately to send the data. In case the clock signal is at a low (0) with "1" sent on the clock line, that is, the clock (0) is send by the host, the clock and data signals are fixed to "1" and the data output is interrupted.

2) Keyboard input (Host→KB)

If clock is at a high (1) and the data low (0), the host assumes that data is going to be sent to the keyboard, and the clock signal is driven in the timing separately shown and data are received in synchronization with it.

If a parity or framing error is involved, the RESEND command is issued from the keyboard and becomes ready for an input again.

8-3. Key code

A key code is sent to the FIFO buffer in the keyboard and the contents of FIFO are sent when it becomes ready to send after handshake. The SET 2 mode is established after the power was turned on. The key code can be selected by the SELECT SCAN command (F0, 00~03) and it is possible to select SET 1, SET 2, and SET3 for the output code. Except for special code keys shown in a separate listing, it produces a "MAKE" code and a "BREAK" code.

Set 1 mode

Make code ..... Value in the code table ..... 1 byte

Break code ..... Value in the code table + 80hex ..... 1 byte

Example: MAKE code = 20 hex produces BREAK code = A0) hex

Set 2, Set 3 mode

Make code ..... Value in the code table ..... 1 byte

1st Break code F0hex

2nd Break code ..... Value in the code table ..... 2 byte

Example: MAKE code = 20 hex produced BREAK code = F0, 20 hex

NOTE: If a key code that needs to be sent is occurred when the FIFO buffer is fully occupied, the OVERRUN code is provided after waiting until a vacancy is obtained in the buffer, then the key code is set. In this event, either MAKE/BREAK code may not be lacking.

8-4. Repeat operation

When the same key is kept depressed, it produces the key code repeatedly sent to the FIFO buffer. The following is established for the repeated key.

If the same key was kept depressed, that particular key code is repeated to issue and stored in the FIFO buffer. All keyboard keys are subject to this in the SET 1 and SET 2 modes, except for the SET 3 mode where the following keys are effective for repeat.

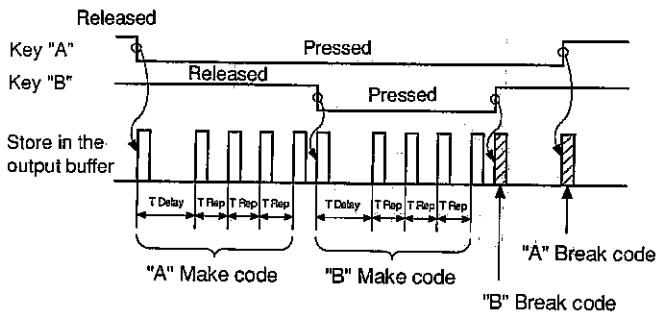


Fig. 8-2

Repeat takes place in the following sequence.

1. Wait for depression of a repeat (TYPEMATIC) key.
2. When a TYPEMATIC key is pressed, the MAKE code of that key is stored in the output buffer.
3. Step 2 is repeated until the MAKE code is accepted to the output buffer.
4. The key by which the MAKE code is produced is temporarily stored in the latest output buffer.

5. It waits for the time TDelay that programmed by the SET TYPEMATIC RATE/DELAY command. If a new key depression was made in this period, it returns to Step 2. If the key that stored the key code latest in the output buffer is released, it returns to Step 1 after storing the BREAK code of that key in the output buffer. If the other key than that stored the MAKE code latest in the output buffer is released, the BREAK code of that key is stored in the output buffer.
6. If the key that stored the MAKE code latest in the output buffer without a new key depression, the MAKE code that temporarily stored is sent to the output buffer.
7. It waits for the repeating time TRep that programmed by the SET TYPEMATIC RATE/DELAY command. If a new key is pushed in this period, it returns to Step 2. If the key that stored the MAKE code latest in the output buffer, the BREAK code of that key is stored in the output buffer and returns to Step 1. If a key other than stored the MAKE code latest in the output buffer is released, the BREAK code of that key is stored in the output buffer.
8. If the key that stored the MAKE code latest in the output buffer is released without a new key depression, it returns to Step 6.

8-5. Fn key

Operational description

The Fn key (key No.128) is the key employed to emulate the 24 key which was removed from the IBM AT 101/102 keyboard in regard to the US, GE, and UK keyboard. It is also used to generate the key code that expanded from the original 101/102 keyboard.

Key code shown next will be issued when the following key is pressed while depressing the Fn key or the Fn key is pressed while the following key is depressed.

Key combination (US keyboard)		Emulation key (AT101/102 keyboard key No.)	
Fn + 7/&	(Key No. 8)	7(Ten key for Number)	(91)
Fn + 8/*	(9)	8(Ten key for Number)	(96)
Fn + 9/(	(10)	9(Ten key for Number)	(101)
Fn + 0/)	(11)	*(Ten key)	(100)
Fn + \/|	(14)	Ins(Ten key for Cursor)	(99)
Fn + ←(BackSpace)	(15)	Del(Ten key for Cursor)	(104)
Fn + U	(23)	4(Ten key for Number)	(92)
Fn + I	(24)	5(Ten key for Number)	(97)
Fn + O	(25)	6(Ten key for Number)	(102)
Fn + P	(26)	-(Ten key)	(105)
Fn + J	(37)	1(Ten key for Number)	(93)
Fn + ;/:	(40)	+(Ten key)	(106)
Fn + ↵(Enter)	(43)	Enter(Ten key)	(108)
Fn + M	(52)	0(Ten key for Number)	(99)
Fn + ./>	(54)	.(Ten key for Number)	(104)
Fn + //?	(55)	/(Ten key)	(95)
Fn + ←	(79)	Home(Cursor key)	(80)
Fn + ↑	(83)	PageUp(Cursor key)	(85)
Fn + ↓	(84)	PageDown(Cursor key)	(86)
Fn + →	(89)	End(Cursor key)	(81)
Fn + Esc	(110)	Blank/5(Ten key for Cursor)	(97)
Fn + F1	(112)	F11	(122)
Fn + F2	(113)	F12	(123)
Fn + F3	(114)	←(Ten key for Cursor)	(92)
Fn + F4	(115)	→(Ten key for Cursor)	(102)
Fn + F5	(116)	↑(Ten key for Cursor)	(96)
Fn + F6	(117)	↓(Ten key for Cursor)	(98)
Fn + F7	(118)	PageUp(Ten key for Cursor)	(101)
Fn + F8	(119)	PageDown(Ten key for Cursor)	(103)
Fn + F9	(120)	Home(Ten key for Cursor)	(91)
Fn + F10	(121)	End(Ten key for Cursor)	(93)
Fn + Ins	(75)	Num Lock	(90)
Fn + Del	(76)	Scroll Lock	(125)
Fn + SysReq	(124)	Print Screen	(124)
Fn + Setup	(127)	Alternate Setup	(NEW)
Fn + Pause	(126)	Sleep	(NEW)

8-6. Typing timing

1) Normal typing timing

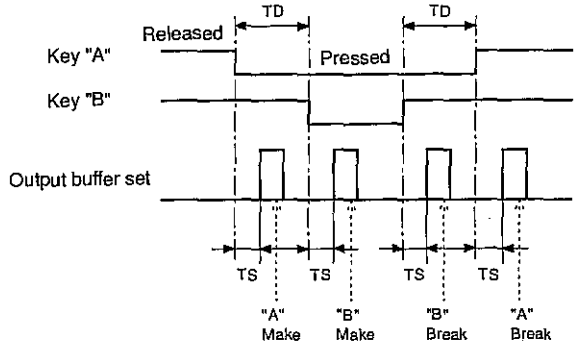


Fig. 8-3

Ts: 10–20msec (NOTE)

But, if it is shorter than the time required to prevent chattering by TD, the order of outputs "A" and "B" may be inverted depending on the sequence of sampling.

NOTE: For this period is required to prevent chattering and is the parameter that may vary according to keyboard mechanical characteristics. The parameter shown above is the one when the bounce convergence time.

Shown below is the expression to obtain Ts.

Min Ts = Maximum bounce convergence time

Max Ts = 2 x (maximum bounce convergence time)

2) Power on timing with a key depression or key code output timing at RESET command input

When power is turned on with a key depressed or the key code of the key pushed after sending the BAT completion code (AAH) is sent after the RESET command has been processed.

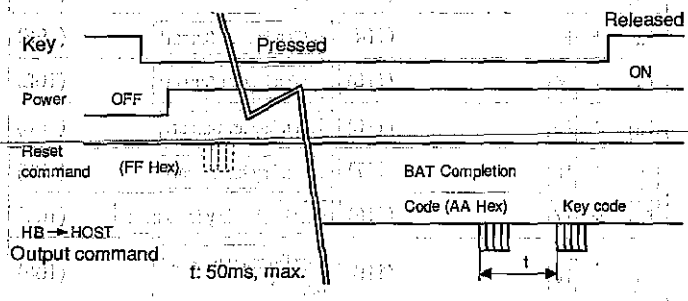


Fig. 8-4

8-7. Input/output commands

1) Input command (host→keyboard controller)

When a command given in the command list is inputted, the process takes place. The response signal to the host should be returned within 20msec, except for the response to the RESET command. If there is no such a command, the RESEND command is returned to the host.

2) Output command (keyboard controller→host)

The keyboard controller sends the command code to the host except the key scan code.

3) Newly employed command codes

DISABLE SLP command.....E2 hex
ENABLE SLP command.....E4 hex
RESET SLP command.....E0 hex
SET SLP command.....E1 hex

8-8. N-key rollover

The keyboard controller itself does the N-key rollover. A resistance method matrix is used for the key matrix, and the return data is sent to the controller via the rollover chip (VHi3JD2CA1A-1) made by Alps. Because of this, a complete N-key rollover may not be attained owing to the limit to the key numbers, it has been so made as to secure the 10 key rollover. Adoption of the N-rollover chip would not generate the overrun code caused by multiple key depression.

8-9. Multiple key depression including the emulation key

(1) In case a normal key is pressed while the emulation key is being pressed and that the normal key is released first.

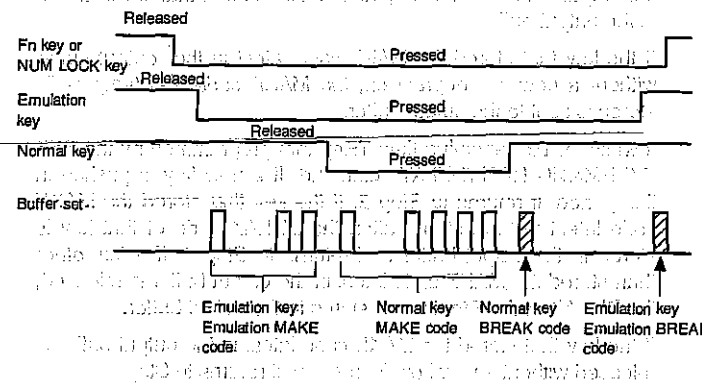


Fig. 8-5

(2) When the normal key is pressed while the emulation key is being pressed and that the emulation is released first.

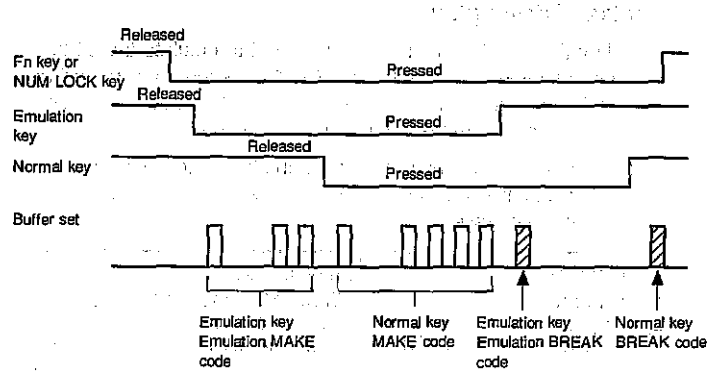


Fig. 8-6

(3) When the normal key is released while the emulation key is being depressed and that the Fn key, emulation key, and normal key are released in this order.

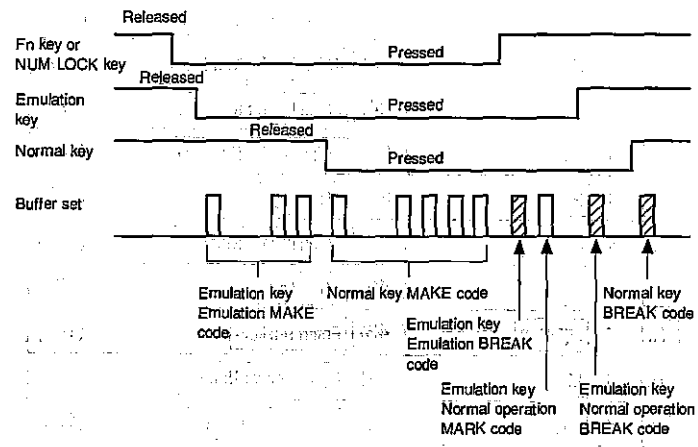


Fig. 8-7

(4) When the normal key is pressed while the emulation key is being pressed and that the Fn key, normal key, and emulation key are released in this order.

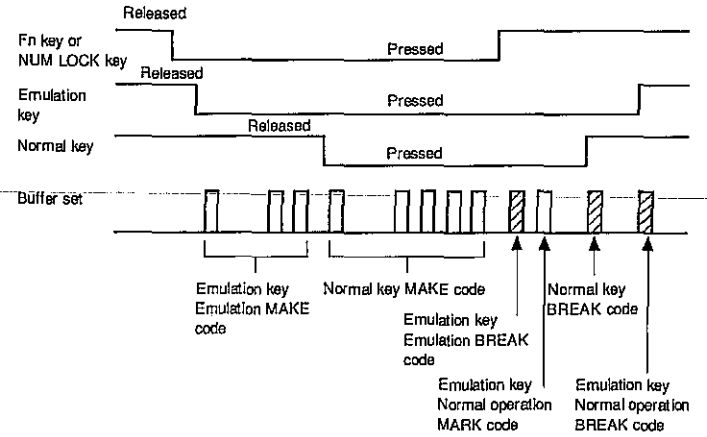


Fig. 8-8

(5) When the normal key is pressed with the shift key while the emulation key is being pressed and that the normal key, shift key, and emulation key are released in this order.

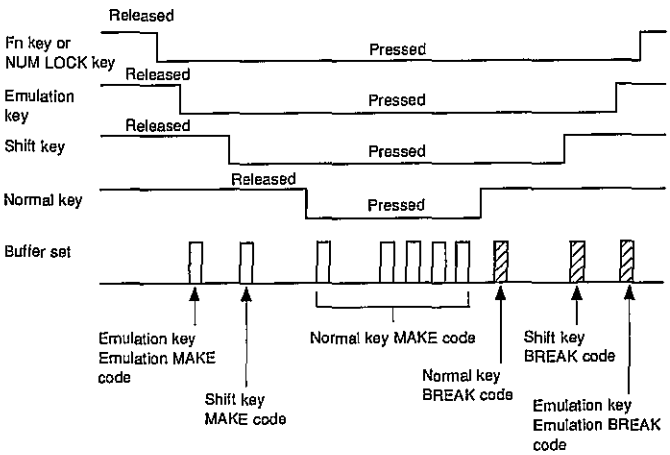


Fig. 8-9

(6) When the normal key is pressed with the shift key while the emulation key is being pressed and that the emulation key, normal key, shift key, and Fn key are released in this order.

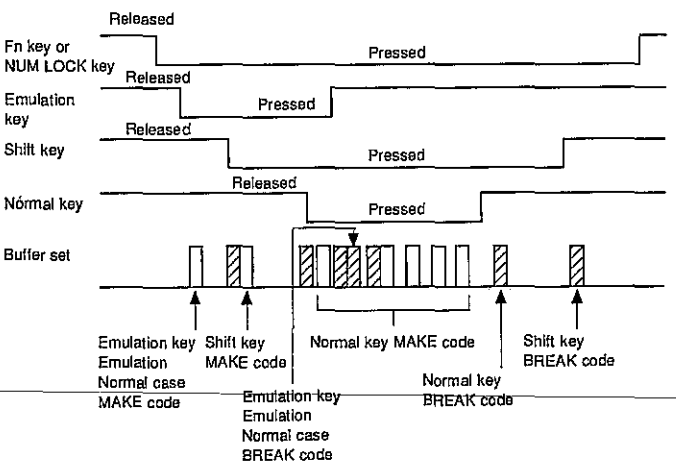


Fig. 8-10

(7) When the normal key is pressed with the shift key while the emulation key is being pressed and that the normal key, emulation key, and shift key are released in this order.

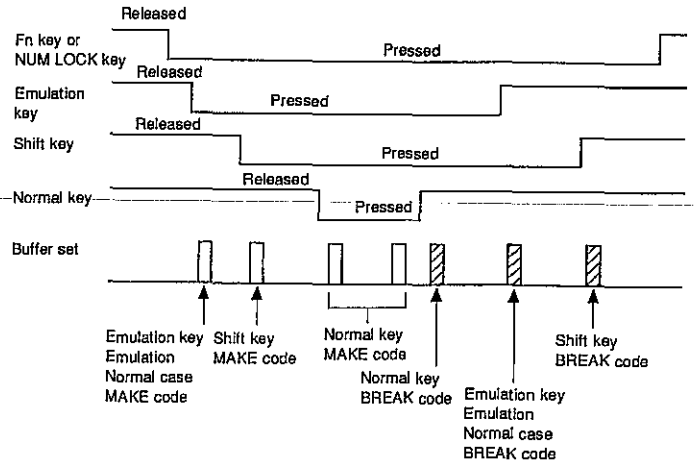


Fig. 8-11

8-10. Resistor membrane method

(1) Configuration

The resistor membrane N-key rollover circuit consists of:

① a membrane switch that has the resistor matrix (printed),

② scan circuit that convert the unselected row to ground level, and,

③ comparator that recognizes the receive signal level.

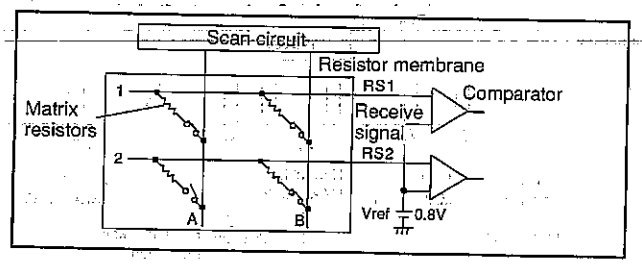


Fig.2 Resistor membraine N-key configuration

(2) Operation

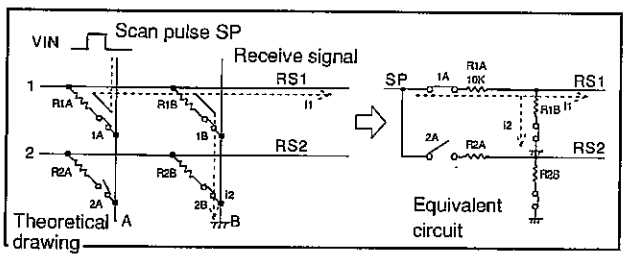


Fig.3 Theoretical drawing

(2)-1 Removal of phantom key by line separation

- Each key switch constitutes a serial matrix resistors RA1~R2B.
- Using those resistors, the not selected by the scan pulse is set to ground level.
- This way, line is isolated in terms of circuits (see Fig.3 Equivalent circuit).
- So, there would be no phantom key generated caused by line to line interference as seen in the conventional configuration.

(2)-2 Receive signal level recognition

- With this method, there would be no generation of phantom key caused by line to line interference.
- But, if there was a rollover operation in the same line of the matrix, the scan pulse peak value VIN is divided by the matrix resistors R1A and R1B to decrease the receive level.
- So, the comparator KM1 (KM2) is used to recognize the level.
- So, if assumed that occurrence of comparator threshold value Vref as many as the maximum rows of the matrix rows, the N-key rollover can be attained by setting it to the minimum receive level.

CHAPTER 9. EXPLANATION OF LSI SIGNAL

9-1. 80C287 80-Bit HMOS NUMERIC PROCESSOR EXTENSION (80C287)

- **High Performance 80-Bit Internal Architecture**
- **Implements Proposed IEEE Floating Point Standard 754**
- **Expands iAPX 286/10 Datatypes to Include 32-, 64-, 80-Bit Floating Point, 32-, 64-Bit Integers and 18-Digit BCD Operands**
- **Object Code Compatible with 8087**
- **Built-In Exception Handling**
- **Operates in Both Real and Protected Mode iAPX 286 Systems**
- **8x80-Bit Individually Addressable, Numeric Register Stack**
- **Protected Mode Operation Completely Conforms to the iAPX 286 Memory Management and Protection Mechanisms**
- **Directly Extends iAPX 286/10 Instruction Set to Trigonometric, Logarithmic, Exponential and Arithmetic Instructions for All Datatypes**
- **Compatible with 80386 CPU**
- **Available in EXPRESS—Standard Temperature Range**
- **Available in 40 pin-Cerdip package (see Packaging Spec: Order #231369)**

The Intel® 80C287 is a high performance numerics processor extension that extends the iAPX 286/10 architecture with floating point, extended integer and BCD data types. The iAPX 186/20 computing system (802C86 with 802C87) fully conforms to the proposed IEEE Floating Point Standard. Using a numerics oriented architecture, the 80C287 adds over fifty mnemonics to the iAPX 286/20 instruction set, making the iAPX 286/20 a complete solution for high performance numeric processing. The 80287 is implemented in N-channel, depletion load, silicon gate technology (HMOS) and packaged in a 40-pin cerdip package. The iAPX 286/20 is object code compatible with the iAPX 86/20 and iAPX 88/20.

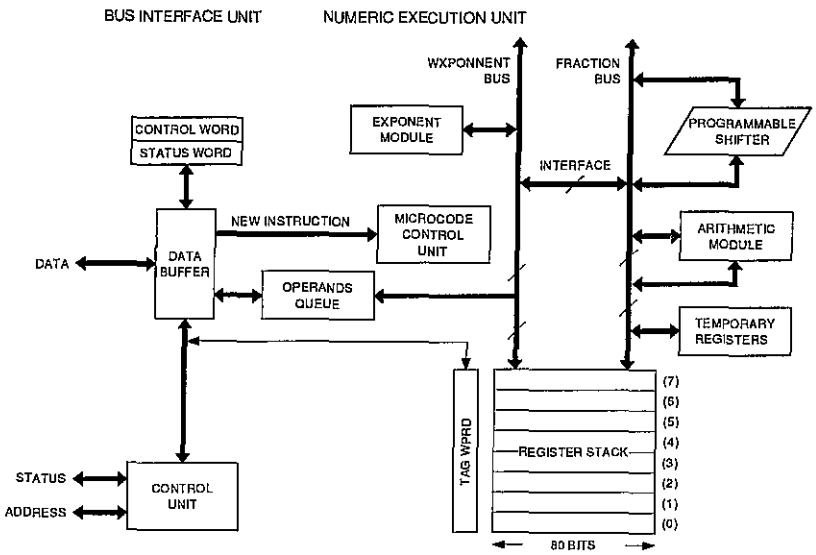
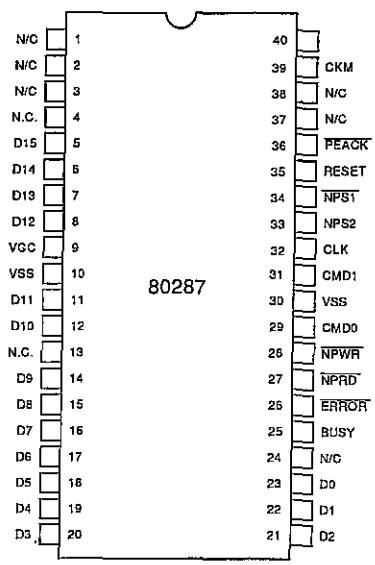


Fig. 9-1. 80C287 block diagram



NOTE:
NC PINS MUST NOT BE CONNECTED.

Fig. 9-2. 80C287 pin configuration

Table 9-1. 80C287 pin description

Symbol	Type	Name and Function
CLK	I	Clock input: this clock provides the basic timing for internal 80C287 operations. Special MOS level inputs are required. The 82284 or 8284A CLK outputs are compatible to this input.
CKM	I	Clock Mode signal: indicates whether CLK input is to be divided by 3 or used directly. A HIGH input will cause CLK to be used directly. this input may be connected to Vcc or Vss as appropriate. this input must be either HIGH or LOW 20 CLK cycles before RESET goes LOW.
RESET	I	System Reset: causes the 80C287 to immediately terminate its present activity and enter a dormant state. RESET is required to be HIGH for more than 480287 CLK cycles. For proper initialization the HIGH-low transition must occur no sooner than 50 µs after Vcc and CLK meet their D.C. and A.C. specifications.
D15-D0	I/O	Data: 16-bit bidirectional data bus. Inputs to these pins may be applied asynchronous to the 80287 clock.
$\overline{\text{BUSY}}$	O	Busy status: asserted by the 80287 to indicate that it is currently executing a command.
$\overline{\text{ERROR}}$	O	Error status: reflects the ES bit of the status word. This signal indicates that an unmasked error condition exists.
PEREQ	O	Processor Extension Data Channel operand transfer request: a HIGH on this output indicates that the 80C287 is ready to transfer data. PEREQ will be disabled upon assertion of $\overline{\text{PEACK}}$ or upon actual data transfer, whichever occurs first, if no more transfers are required.
$\overline{\text{PEACK}}$	I	Processor Extension Data Channel operand transfer ACKnowledge: acknowledges that the request signal (PEREQ) has been recognized. Will cause the request (PEREQ) to be withdrawn in case there are no more transfers required. $\overline{\text{PEACK}}$ may be asynchronous to the 80287 clock.
$\overline{\text{NPRD}}$	I	Numeric Processor Read: Enables transfer of data from the 80287. This input may be asynchronous to The 80C287 clock.
$\overline{\text{NPWR}}$	I	Numeric Processor Write: Enables transfer of data to the 80C287. This input may be asynchronous to the 80C287 clock.
$\overline{\text{NPS1}}$, NPS2	I	Numeric Processor Selects: indicate the CPU is performing an ESCAPE instruction. Concurrent assertion of these signals (i.e., $\overline{\text{NPS1}}$ is LOW and NPS2 is HIGH) enables the 80C287 to perform floating point instructions. No data transfers involving the 80C287 will occur unless the device is selected via these lines. these inputs may be asynchronous to the 80C287 clock.
CMD1, CMD0	I	Command lines: these, along with select inputs, allow the CPU to direct the operation of the 80C287. These inputs may be asynchronous to the 80C287 clock.

9-2. SC9889

9-2-1. General

This LSI incorporates two 82C59A interrupt controllers, 82C54 timer, 82C50 UART, and CMOS RAM, with a random gate to control the system operation and pseudo-SRAM control based on the AT/AX architecture.

Features

- AT/AX compatible machine system controller
- Internal peripheral controller
  - 82C59A interrupt controller x 2
  - 82C54 timer x 1
  - 82C50 UART x 1
- Internal 2KB CMOS RAM
- AT/AX compatibility
  - 80C286 interface
    - Clock control
    - Ready control
    - Reset control
    - Command generator
    - Data control
    - Hold control
  - 80C287 interface
  - Interrupt control by the 82C59A (internal = 3, external = 14)
  - System timer, refresh request, and speaker tone generation by 82C54
  - RS-232C interface by 82C50
  - Modem control
  - RTC interface
  - Including 2KB CMOS RAM
  - Pseudo-SRAM control (conventional memory, extended memory, EMS memory)
  - Port-B control
- Special functions
  - Sleep function
  - Power save function
  - Resume function (not used for the PC-6220)
  - Interface power off
- 184-pin QFP

9-2-2. Block diagram

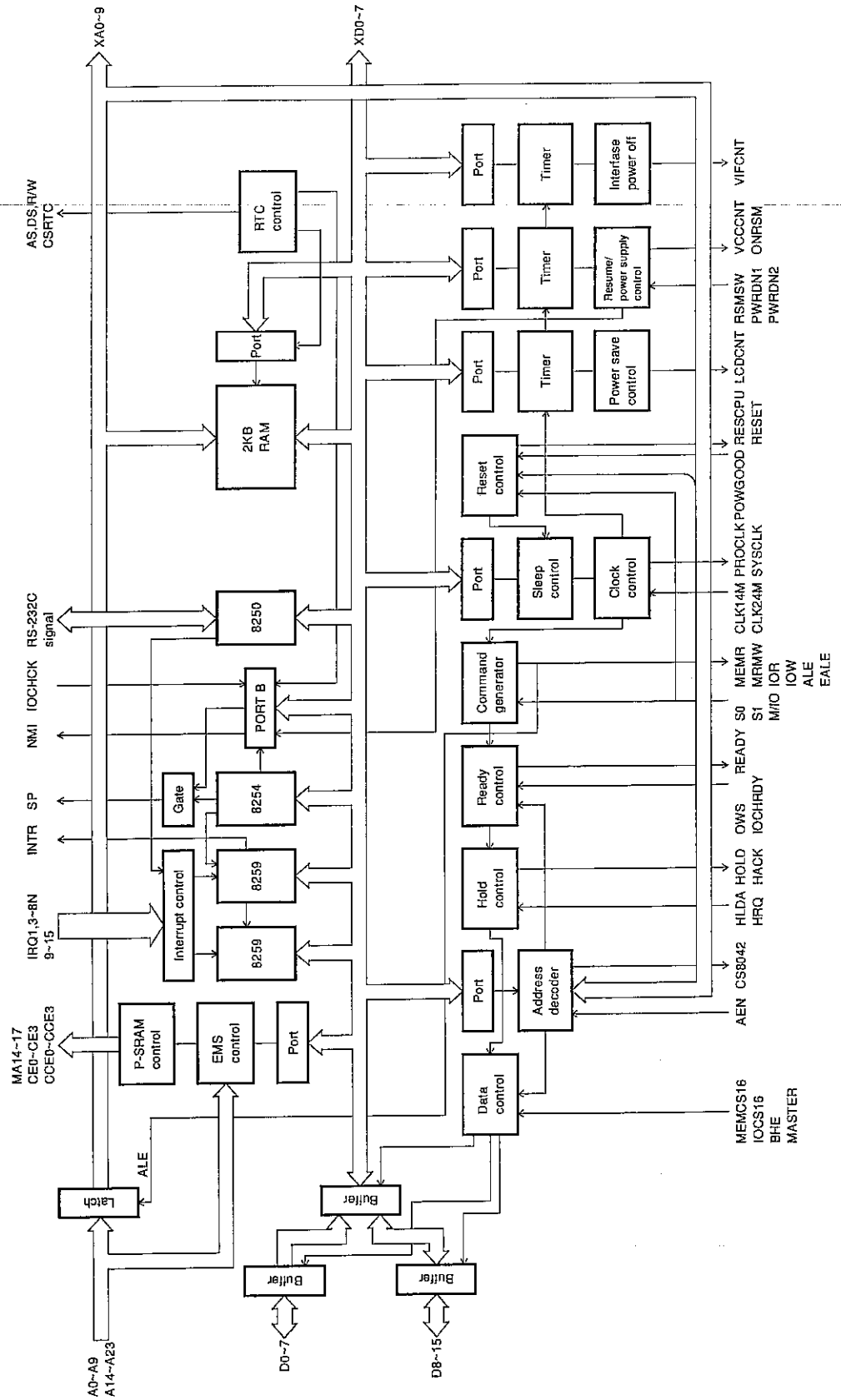


Fig. 9-3

9-2-3. Signal description

Signal name	IN/OUT	Function
CLK14M	IN	A 14.31818MHz clock input used for the CPU clock and also used for the timer clock after dividing it to 1/12.
CLK24M	IN	A 23.9616MHz clock input used for the CPU clock and also used for the 82C50A UART clock after dividing it to 1/13.
SYSCLK	OUT	I/O slot strobe signal. A 1/2 CLK14M or 1/4 CLK24M is delivered.
PRCLK	OUT	CPU clock. A CLK14M or CLK24M input or 1/2 CLK24M is delivered with the clock selection.
S1-0	IN	Bus cycle status signal input from the CPU.
MI0	OUT	Memory and I/O select from the CPU.
ALE	OUT	Strobe to externally latch the CPU output address.
MEMR	IN/OUT	Memory read signal. During the memory read cycle and refresh cycle, a low state of strobe signal is issued, except when reading the memory signal on the local bus.
MEMW	IN/OUT	Memory write signal. Except for the memory write of the local bus, a low state of strobe signal is issued during the memory write cycle.
IOR	IN/OUT	I/O read signal. A low state of strobe is issued during the I/O read cycle.
IOW	IN/OUT	I/O write signal. A low state of strobe is issued during the I/O write cycle.
LMSEL	OUT	Indicates accessing of address below 1MB which is used to generate SMEMR or SMEMW in the external circuit.
EALE	OUT	Address latch signal used by the expansion unit employed to emulate a 6MHz bus cycle.
PWRGOOD	IN	Input from the power supply unit to indicate that the supply voltage is normal.
RESCPU	OUT	Reset signal issued when returning from the protect mode to the real mode, or when exiting from the shut down cycle. Connected only to the CPU.
BRESET	OUT	System reset signal.
READY	OUT	Signal used to inform the CPU the end of the cycle currently executed.
OWS	IN	Signal used to request the system to terminate the bus cycle currently executed by the device on the I/O slot.
IOCHRDY	IN	Signal used to request the system to extend the bus cycle currently executed by the device on the I/O slot.
HOLD	OUT	Signal used to request the CPU to hand down the bus.
HLDA	IN	Acknowledge to the CPU for its hold request.
HREQ	IN	Bus request signal from the DMAC.
HLDAK	OUT	Acknowledge request to the DMAC.
AEN	OUT	Signal used to indicate that it is a DMA cycle not by the master. A high on this line indicate the DMA cycle.
MA21-14	OUT	Pseudo-SRAM high address. For MA21-19, the address from the CPU is internally latched for output.
PCSL0 PCSH0 PCSL1 PCSH1	OUT	Pseudo-SRAM chip select. Four chip selects are used to access 16 bits of 2-bank pseudo-SRAM. Bank0 Bank1 Low byte PCSL0 PCSL1 High byte PCSH0 PCSH1
PSOE	OUT	Pseudo-SRAM output enable signal.
PSWE	OUT	Pseudo-SRAM write enable signal.
REFR	OUT	Pseudo-SRAM refresh signal.
CSBIOS	OUT	Display BIOS chip select signal.
NMI	OUT	Non-maskable interrupt signal to the CPU.
IOCHCKN	IN	Signal used to inform an error in I/O slot.
PCKN	IN	Parity check error signal.
INTR	OUT	Interrupt request signal to the CPU.
IRQ1 IRQ3-7 IRQ8N IRQ9-12 IRQ14-15	IN	Interrupt request signal from an external device.
LA23-0	IN/OUT	CPU side address signal.
SA9-0	IN/OUT	System side address signal.
BHE	IN/OUT	Data bus access signal, high side .
SBHE	IN/OUT	Latched data bus access signal, high side.
D7-0	IN/OUT	CPU side data bus, low side.
D15-8	IN/OUT	CPU/system side data bus, high side.
XD7-0	IN/OUT	System side data bus, low side.

Table 9-2 (a)

Signal name	IN/OUT	Function
RDI	IN	Receive data.
CII	IN	Calling tone detect signal.
CTSI	IN	Send enable signal.
DSRI	IN	Modem signal ready signal.
CDI	IN	Carrier detect signal.
SDI	OUT	Send data.
RTSI	OUT	Send request signal.
DTRI	OUT	Terminal ready signal.
SP	OUT	Speaker tone output signal.
RFRSHN	IN/OUT	Refresh timing signal to external bus.
BCNT1 BCNT2 BCNT3 BCNT4	OUT	External buffer control signal. Enable / Direction Data bus, low side: BCNT3 / BCNT4 Data bus, high side: BCNT1 / BCNT2
EXPND	IN	Connected with GND of the expansion unit when connected need to pull-up externally.
SELTM	IN	Signal used to inform selection of external gate array.
DACK2	IN	Signal used to inform transfer on DMA channel 2.
AS	OUT	Strobe signal for the RTC to latch address.
DS	OUT	Strobe output for RTC to read.
RW	OUT	Strobe output for RTC to write.
CSRTCN	OUT	RTC chip select signal. A low state of signal is issued to select RTC.
VIFCNT	OUT	Printer and RS-232C interface IC control signal.
VCCOFF	OUT	Shuts off the unwanted power supply during the resume.
LCDCNT	OUT	Controls the LCD power supply.
VMDCNT	OUT	Control the modem power supply.
BLCNT	OUT	Control the backlight power supply.
RSMSW	IN	Resume switch status input.
ONRSM	OUT	Signal used to inform the resume state.
MANOFF	IN	Indicates the main power supply status.
SHUT	IN	Top cabinet close alarm signal. A high state of signal is an input normally by the external pullup resistor. When the top cabinet is closed, the microswitch is closed to have a low level input signal.
BUSY	OUT	Signal used to indicate to the CPU that NDP is busy.
BUSYNDP	IN	Signal from the NDP to indicate the busy state.
ERRNDP	IN	Signal used to indicate occurrence of an error from NDP.
RSTNDP	OUT	Signal used to initialize NDP.
CSNDP	OUT	NDP select signal.
PWRDWN2-1	OUT	Signal used to select the VGA controller operating mode.
CSMDMN	OUT	Internal modem select signal.
MINT	IN	Interrupt request from the internal modem.
MORSTN	OUT	Internal modem reset signal.
MRI	IN	RI signal from the internal modem.
MEMCS16	IN/OUT	Indicates that the currently accessed memory is a 16-bit device.
IOCS16	IN	Indicates that the currently accessed I/O is a 16-bit device.
MASTER	IN	Indicates that the bus control is requested by an external master.
DMACLK	OUT	DMAC clock which is 1/2 of SYSCLK.
CLKSM	OUT	Key controller clock. 1/3 of CLK24M is supplied in 50% duty.
ADS	N.C.	Reserved. ADS signal input pin when the 80386SX is used.
MA23-22	N.C.	Reserved. Memory address high order 2 bits (corresponds to 4M RAM).
TEXT	IN	Test input. With a high state of this signal, the test mode is established.
VDD	----	Power supply.
GND	----	GND

Table 9-2 (b)

9-2-4. Function of block

4.1. Clock control

In this clock controller, the system clock supplied to the CPU, internal circuits, and I/O slot is derived from the clock input. Also, the input clock to the 82C54/82C50 serial controller and the minute-increment timer used by a special function is derived.

Two kinds of input clocks are supplied at all times; 14.31818MHZ and 23.9616MHz. 1.8432MHz (After dividing 23.9616MHz to 1/13) is supplied to the internal timer. The CPU clock can be changed to 3 kinds software-wise. The I/O address 022H and 023H are used for the selection of the CPU clock. 04H is written to the port 022H, then the data are write to the port 023H. When 023H is once accessed, 04H needs to be written to 022H again. See the table next for the bit definition of the port 023H.

Bit	Signal name	Significance
0, 1	RESERVED	Reserved.
2, 3	CKSEL1, 2	CPU clock selection
4–7	RESERVED	Reserved.

When reset, all are reset except for CLSEL2 is set to "1".

Shown next is the CPU clock and the system clock when CKSEL1 and 2 are set for the port 023H.

CKSEL2	CKSEL1	CPU clock	CPU operating frequency	System clock
0	0	11.980S MHz	5.9904 MHz	5.9904 MHz
0	1	14.31818 MHz	7.15909 MHz	7.15909 MHz
1	0	23.9616 MHz	11.9808 MHz	5.9904 MHz
1	1	Prohibitted		

4.2. Ready control

In the ready controller, waits during the CPU access is determined. Shown below is the number of waits when accessing device.

Device	Waits	
	5.9904MHz/ 7.15909MHz	11.9808MHz
Main memory, private memory	0	1
Extended memory, EMS memory	0	1
BIOS ROM	0	1
VRAM (8-bit)	4	7
VRAM (16-bit)	1	2
DOS ROM, 8 bits	4	11
DOS ROM, 16 bits	1	5
80287	0	0
VGA (8-bit)	4	7
System I/O (000H~0FFH)		
VGA (16-bit)	1	2
Internal I/O, 8-bit I/O	4	11
HDC, EMS register, 16-bit I/O	1	5
Interrupt acknowledge cycle	1	2

4.3. Reset control

The CPU and system reset signal is created from the signal PWRGOOD.

When the CPU went into the shut down cycle, the reset signal is issued to the CPU. The data bus is monitored when the reset CPU command is sent to the keyboard controller (80C42) and the reset signal is sent to the CPU without receiving the signal from the 8042.

4.4. Command generator

The command signal is created by receiving the 286 CPU status signal. Also, the signal ALE is issued.

For a device that requires the command recovery time in the I/O cycle, the command delay is automatically inserted.

Shown next is the CPU clocks for the command delay when accessing a device.

Device	Command delay/CPU clocks	
	5.9904MHz/ 7.15909MHz	11.9808MHz
Main memory, private memory	0	0
Extended memory, EMS memory	0	0
BIOS ROM	0	0
VRAM (8-bit)	0	0
VRAM (16-bit)	0	0
Dictionary ROM, 8 bits	0	3
Dictionary ROM, 16 bits	0	3
80C287	0	0
VGA (8-bit)	1	2
System I/O (000H~0FFH)		
VGA (16-bit)	1	2
Internal I/O, 8-bit I/O	1	5
HDC, EMS register, 16-bit I/O	1	5
Interrupt acknowledge cycle	0	0

4.5. Data control

The internal/external data bus buffer is controlled and 8 bits to 16 bits and 16 bits to 8 bits conversion is carried out.

4.6. Address decoder

Internal device port select signal is created from the address. Also, chip select signal is issued for some of external devices.

Since the address input is latched by ALE, it may not be needed to be fully established during the cycle and may use CPU local address cycle.

4.7. Hold control

DMA request and refresh request are arbitrated and a hold is applied to the CPU.

When going into the sleep mode, the hold state is established before stopping the CPU clock. After this, the hold request is cancelled. For the clock is at a halt, the CPU stays in the hold state. Therefore, DMA request or refresh request during the sleep mode can be performed without contention.

4.8. Special functions

(1) Sleep function
The CPU clock is suspended to supply when the HLT command is executed.

(2) Power save function
With this feature, the power supply to the LCD and backlight is turned off after a lapse of a certain time (auto power save feature). It is also possible to directly shut off the power supply to the LCD and backlight independently.

(3) Resume function (not used for the PC-6220)
With this feature, the memory contents are backed up when the power is turned off so that the previous state may be recovered when the power is turned on.

(4) Interface power off
With this feature, power consumption is abated when not required for the RS-232C interface IC and internal modem.

(1) and (3) functions mentioned above are not able to use when connecting the expansion unit.

4.8.1. Sleep function

The sleep function is completely supported by the hardware once the HLT command has been executed. When the HLT command is executed, the CPU sets S0 and S1 low and M/*IO and A1 high to inform the existence of the hold state to externals. As the sleep controller recognize it, the sleep mode will be established in the following sequence.

(1) Hold request is issued to the CPU. If the refresh request or DMA transfer request is issued at the same moment, it will be handled by the arbitrary circuit.

(2) After recognizing the halt acknowledge, the CPU clock is suspended to supply in synchronization with a high to low transition of the clock input to the controller in $2 cycle.

(3) The hold request is cancelled by the sleep. Since the CPU is at a hold state, the DMA transfer and refresh during the sleep continue to perform.

An interrupt request is issued including NMI, it exits from the sleep mode. When the interrupt occurred, the clock is resumed to supply to the CPU in synchronization with a high to low transition of the clock input to the controller and the CPU starts executing the command that follows HLT.

When the input to EXPND line is at a low, connection of an expansion is assumed and prohibits steps (1)–(3) so that the sleep function does not take place. The state of the EXPND line input can be known by scanning EXPND of the EXSTAT register. When EXPND is at "0", the expansion unit is in connection. The EXSTART register is a read only register which is allocated to 0DH of the Sharp original port. The table below shows its bit definition.

EXSTAT register

Bit	Signal name	Significance
0	EXPND	State of expansion unit connection
1–7	—	Undefined. Reads "0" at all times.

4.8.2. Power save function

The power save function automatically turns off the power supply to the LCD and backlight when there was no key operation met for a period of the given time. So, it has a timer within the power save controller which continues to count the time as long as there is no interrupt request from the 8042 key controller. When the prescribed time is reached, the signal is issued from the LCDCNT and BLCNT line to turn off the LCD and the backlight power. At the same time, the VGA controller goes into the relax mode.

The VGA controller operating mode can be directly set by the internal I/O register. PWRDWN1 and 2 of the VGACNT register are used to set the relax mode and retire mode. DISVGA of the VGACNT register is used to set active or inactive of the internal VGA, which is active "0". The VGACNT register is allocated to 0EH of the Sharp original port and its bit definition is shown next.

VGACNT register

Bit	Signal name	Significance
0	POLINV	Internal SIO input/output polarity inversion
1	DISVGA	Internal VGA on/off setting
2	PWRDWN1	VGA controller mode setting (relax mode)
3	PWRDWN2	VGA controller mode setting (retire mode)
4–7	RESERVED	Reserved. Possible to read/write.

When reset, all are reset to "0".

The table next shows the VGA controller operation mode set by PWRDWN1 and 2.

PWRDWN 2	PWRDWN 1	LCD power supply	BL power supply	VGA controller	Note
0	0	ON	ON	Normal mode	
0	0	ON	OFF	Normal mode	
0	0	OFF	OFF	Relax mode	PWRCNT register, PCBL=0
0	1	OFF	OFF	Relax mode	
1	0	OFF	OFF	Retire mode	
1	1	OFF	OFF	Pro-hibited.	

When the power save feature is used, both PWRDWN1 and 2 need to be set to "0". The DISVGA is set to "0" to set the internal VGA active, and *LCDEN of the SIOCFR register needs to be set to "0" to select the LCD as a display device.

To directly turn off the LCD or backlight power supply by means of software, "0" must be written to PCVLCD and PCBL of the PWRCNT register. The PWRCNT register is an 8-bit read/write register employed to control power supplies which is allocated to 06H of the Sharp original port, whose big definition is as shown next.

PWRCNT register

Bit	Signal name	Significance
0	PCVIF	Printer, RS-232C interface IC control.
1	PCVLCD	VGA controller and LCD power supply control
2	PCVCC	System power supply control (VCC)
3	PCBL	Backlight power supply control
4	PCVMD	Modem power supply control
5–7	RESERVED	Reserved. Read/write possible.

When reset, each bit of PCVIF, PCVCC, PCBL, and PCVMD is set "1" and others are reset.

When using the power save function (auto power save) by means of the timer, OCVLCD and PCBL of the PWRCNT register must be set to "1". Then write "1" to ASLCD of the ATSTBY register to put the timer effective, then set in the PWRTIM register the time the power save should function.

The ATSTBY register is an 8-bit read/write register with which programmed to put control functions in effect, which the timer becomes effective when set to "1". It is allocated to 07H of the Sharp original port whose bit definition is as given next.

ATSTBY register

Bit	Signal name	Significance
0	ASVIF	Auto interface power off on/off setting
1	ASLCD	Auto power save on/off setting
2	ASVCC	Auto resume on/off setting
3–7	RESERVED	Reserved. Read/write possible

All are reset to "0" when reset.

The PWRTIM register is used to program the time for auto power save that it may be set in increment of one minute in a range of 0 to 15 minutes. However, the actual time is shorter than the programmed time within a minute. When PST3~0 are all "1", the setting will be 14~15 minutes. It is possible to read/write and the set value is read. It is allocated to 09H of the Sharp original port whose bit definition is given next.

PWRTIM register

Bit	Signal name	Significance
0~3	PST0~3	Auto power save time setting
4~7	RESERVED	Reserved. Read/write possible.

When reset, PST3~0 are set to "1" and others are reset.

When IRQ1 which is the interrupt request from the 8024 goes high before the set time, the set value is reloaded in the timer and starts to count from the start all over again. The timer will be reloaded even if the PWRCNT register, ATSTBY register or PWRTIM register of the Sharp original port is written.

4.8.3. Resume function (not used for the PC-6220)

To use the resume function, it has to be enabled by writing "1" in RSMEN of the RSMCNT register. The RSMCNT register is an 8-bit read/write register which is allocated to 0BH of the Sharp original port whose bit definition is given next.

RSMCNT register

Bit	Signal name	Significance
0	RSMEN	Resume mode setting
1	CIEN	Reserved. Read/write possible.
2	MRIEN	Reserved. Read/write possible.
3~7	RESERVED	Reserved. Read/write possible.

When reset, all are reset to "0".

In the resume mode (RSMEN=1), there are two cases that moves to the power down state by shutting the power supply (V_{CC}) off with the memory backed up.

(1) Input of a low to high transition signal from the RSMS line.

(2) No key operation is done within the prescribed time.

In the case of (1), a high state of signal is issued from the NMI line at a low to high transition of the signal input from the RSMSW line to apply NMI to the CPU. On the other hand, in the case of (2), the resume controller internal timer continues to count while there is no interrupt request from the 8042. When the programmed time is reached, the NMI is caused. But similar as the sleep function, a low on the EXPND input prohibit the NMI and the resume function does not take place. The state of the EXPND input can be scanned on EXPND of the EXSTAT register.

When using the resume function by the timer (auto resume), the timer must be turned on after writing "1" to ASVCC of the ATSTBY register and the time that the power down is expected must be set in the RSMTIM register. It would be possible to program it in increments of one minute within a range of 0 to 127 minutes. actual time is shorter than the programmed time within a minute. When ART6~0 are all "1", the setting will be 126~127 minutes. It is possible to read/write and the set value is read. It is allocated to 0AH of the Sharp original port whose bit definition is given next.

PWRTIM register

Bit	Signal name	Significance
0~6	ART0~6	Auto resume mode setting
7	RESERVED	Reserved. Read/write possible.

When reset, ART6~0 are all set to "1" and the bit 7 is reset. Similar as the auto power save, an interrupt request from the 8042 (IRQ) turns high before the programmed time, the set value is loaded in the timer and the count starts all over again from the beginning. The timer will be reloaded when the PWRCONT register, ATSTBY register, or RSMTIM register of the Sharp original port is written.

In either case of (1) and (2), occurrence of NMI does the same process and requires software support. The following are required in the NMI routine in order to power down during the resume mode.

(1) Judges the NMI cause.

(2) All I/O registers of the device (VCC supply) installed to the system must be saved to the expanded CMOS RAM.

(3) If the VRAM contents may not be retained, it has to be saved in the pseudo-SRAM private area (256KB).

(4) All CPU registers at NMI occurrence must be saved to the stack and SS:SP must be written in the CMOS RAM.

(5) In order to shut down the system power supply, "0" must be written in PCVCC of the PWRCNT register.

To judge the cause of NMI at (1), RSMNMI of the NMIFCT register must be scanned. If "1", an NMI occurrence is indicated by the RSMSW input or the resume timer. The NMIFCT register is a read only register which is used to judge the NMI cause which is allocated to 0FH of the Sharp original port whose bit definition is shown next.

NMIFCT register

Bit	Signal name	Significance
0	RSMNMI	On state of the resume NMI request
1~7	—	Undefined. Reads "0" at all times.

To restore from the power down state in the resume mode, the system power must be turned on and PWRGOOD input must change from low to high. Because a reset is applied in this instance, the following process takes place in the initialization routine after the reset.

(1) Reset cause is judged.

(2) The contents of I/O registers saved in the CMOS RAM and are loaded to devices.

(3) The contents of the VRAM are loaded from the private area of the pseudo-SRAM (in case the contents of the VRAM may not be retained).

(4) SS:SP is read from the CMOS RAM and all CPU registers are restored from the stack.

To judge the reset cause in (1), RCR of the RSTFCT register is scanned. If "1", it indicates to turn off the VCC supply by software in order to power down in the resume mode. The RSTFCT register is a read only register used to judge the reset cause. When this register is scanned, each bit of RCR, RCCI, and RCMRI is reset to "0". It is allocated to 0CH of the Sharp original port whose bit definition is shown next.

RSTFCF register

Bit	Signal name	Significance
0	—	Undefined. Reads "0" at all times.
1	RCR	On state of the system power (VCC) off request
2	RCCI	State of the power on cause by the CI input of the internal SIO.
3	RCMRI	State of the power on cause by the RI input of the internal modem.
4~7	—	Undefined. Reads "0" at all times.

RCCI and RCMRI of the RSTFCT register is used to support the auto sensor from the internal SIO and the internal modem.

When the system power turns on, a reset is applied, and the CPU reads the RSTFCT register during the initialization routine. If RCCI or RCMRI is "1", it indicates that power on took place by the auto answer. Reading it again resets RCCI and RCMRI.

4.8.4. Interface power off

Withe the interface power off function, the power consumption of the interface IC may be held down when not using the printer or RS-232C. The time the interface power off feature functions is when the printer or the internal SIO was not accessed within the given time, or, the internal I/O register is directly accessed by means of software.

To directly turn off the interface power by software, "0" must be written to PCVIF of the PWRCNT register. When written, the printer interface IC output goes high impedance and the RS-232C line drive receiver goes into a standby mode to decrease the circuit current.

To use the auto interface power off feature, PVCIF of the PWRCNT register must be set to "1". then write "1" to ASVIF of the ATSTBY register to turn on the timer. The timer will be cleared when the internal printer and internal SIO is accessed. It may also be cleared by writing the PWRCNT register or ATSTBY register of the Sharp original port. The time power off feature comes active after the timer has cleared for 14 to 15 minutes.

It is also possible to control the power supply to the internal modem using the interface power off function. To shut off the power supply to the internal modem (VMDM), write "0" to PCVMD of the PWRCNT register. With this, the signal employed to shut off the modem power supply appears on the VMDCNT line.

4-8-5. Power status

Since the power is automatically shut down for the auto power save timer, and auto interface power off functions by means of the timer. The CPU will recognize the status of the LCD power, backlight power, and printer-RS-232C control by scanning the PWRSTAT register. The PWRSTAT register is a read only register which is allocated to 08H of the Sharp original port. Except for PSVIF, PSLCD, and PSBL, the power supply control data set to the PWRCNT register are read. "0" means off and "1" on. See the table next for the bit definition of the PRSTAT register.

PWRSTAT register

Bit	Signal name	Significance
0	PSVIF	State of printer and RS-232C interface IC control
1	PSLCD	State of LCD power supply (VLCD)
2	PSVCC	State of system power supply (VCC)
3	PSBL	State of backlight power supply (VBL)
4	PSVMD	State of modem power supply (VMDM)

4-9. Interrupt control

A pair of 82C59A interrupt controllers are internally contained in this chip for the interrupt control and supports 16 interrupt levels in conjunction with the cascade connection NMI. The NMI is port-B controlled.

As an 8-bit I/O device on the system bus (XD bus), a pair of 82C59A has address mapped to 020H–03FH on the master side and 0A0H–0BFH. In order to avoid contention with the CPU clock switch controlling I/O address 022H and 023H (refer to paragraph 4.1) for the 82C59A on the master side, the selection is not done when the bit of the latch address is "1".

The table below shows the 82C59A interrupt outputs.

Master	Slave	Function
IRQ0		Timer output channel 0
IRQ1		Keyboard (output buffer full)
IRQ2		Interrupt from the slave side controller
	IRQ8	Real time clock interrupt
	IRQ9	VGA controller or INT0AH (IRQ2)
	IRQ10	Reserved (expansion slot)
	IRQ11	Reserved (expansion slot)
	IRQ12	Reserved (expansion slot)
	IRQ13	Co-processor
	IRQ14	Hard disk controller
	IRQ15	Reserved (expansion slot)
IRQ3		Serial port 2 (COM2)
IRQ4		Serial port 1 (COM1)
IRQ5		Parallel port 2
IRQ6		Floppy disk controller
IRQ7		Parallel port 1

4.10. Timer

A single 82C54 interval timer is internally contained in this chip.

The 82C54 is mapped to the I/O address 040H–05FH as an 8-bit I/O device on the system bus (XD bus). Three independent 16-bit counter on channels 0–2 of the 82C54 can be defined as follows:

Channel 0	System timer
GATE0	Fixed ON
CLKIN0	1/12 14.31818MHz clock
CLKOUT0	82C59A IRQ0
Channel 1	Refresh request generator
GATE1	Fixed ON
CLKIN1	1/12 14.31818MHz clock
CLKOUT1	Refresh request cycle
Channel 2	Speaker tone generator
GATE2	Fixed ON
CLKIN2	1/12 14.31818MHz clock
CLKOUT2	Speaker drive

4.11. Serial interface

The 82C50 UART is internally contained in this chip as a serial interface and supports a single channel RS-232C interface using the external RS-232C driver as an internal SIO. This also used for the interface with the internal modem.

Two serial interfaces may be port allocated and set on or off, which the SIOCFR register is used for the RS-232C and the MDMCFR register for the internal modem. The SIOCFR register is a 7-bit read/write register which is allocated to 01H of the Sharp original port. The MDMCFR register is a 2-bit read/write register which is allocated to 03H of the Sharp original port.

The table next shows bit definition.

SIOCFR register

Bit	Signal name	Significance
0–2	FDD0–2	Reserved. Read/write possible.
3	S101/*2	Internal SIO port allocation
4	*SIOEN	Internal SIO on/off setting
5	*INTKEY	Reserved. Read/write possible.
6	*LCDEN	Display device selection
7	—	Undefined. Reads "0" at all times.

MDMCFR register

Bit	Signal name	Significance
0	OUTSEL	MORSTN output signal selection
1–3	—	Undefined. Reads "0" at all times.
4	*MDMEN	Internal modem on/off setting
5–7	—	Undefined. Reads "0" at all times.

When reset, *SIOEN of the SIO CFR register and *MDMEN of the MDMCFR register are set to "1" and all others are reset.

*SIOEN and SIO1/*2 of the SIOCFR register may be revised of their contents when written to "02" to the Sharp original port. The inverted bit 4 of the 02H port corresponds to SIO1/*2 and bit 5 to SIOEN.

The table below shows the ports that allocated by the setting of SIOCFR and MDMCFR registers vs. active input to IRQ3 and IRQ4 of the 82C59A.

*SIOEN	*MDMEN	SIO1/*2	Internal SIO	Internal modem	IRQ3 input	IRQ4 input
0	0	0	COM2	COM1	Internal SIO	Internal modem
0	0	1	COM1	COM2	Internal modem	Internal SIO
0	1	0	COM2	OFF	Internal SIO	External IRQ4
0	1	1	COM1	OFF	External IRQ3	Internal SIO
1	0	0	OFF	COM1	External IRQ3	Internal modem
1	0	1	OFF	COM2	Internal modem	External IRQ4
1	1	0	OFF	OFF	External IRQ3	External IRQ4
1	1	1	OFF	OFF	External IRQ3	External IRQ4

The RS-232C interface serial input/output and control signals can be inverted with POLINV of the VGACNT register. When POLINV is at "1", the polarity inverts. The VGACNT register is allocated to 0EH of the Sharp original port whose bit definition is as shown next.

VGACNT register

Bit	Signal name	Significance
0	POLINV	RS-232C input/output polarity inversion
1	DISVGA	Internal VGA on/off setting
2, 3	PWRDWN1, 2	VGA controller mode setting
4–7	RESERVED	Reserved. Read/write possible

When reset, all are reset to "0".

To reset the internal modem (that can be installed within the machine), the output from the MORSTN line is used. The 1-bit output of the MORSTN output port can be switched with the port select signal output using OUTSEL of the MDMCFR register. When OUTSEL is at "1", the bit 3 of the I/O address 202H port is issued. When "0", the decoded signal of the I/O address 202H is issued as a port select signal. The 202H port is a read/write internal I/O register whose bit definition is shown next.

202H port

Bit	Signal name	Significance
0–2	RESERVED	Reserved. Read/write possible
3	MORSTN	Internal modem reset signal
4	RESERVED	Reserved. Read/write possible
5–7	—	Undefined. Reads "0" at all times.

When reset, bits 0–4 are reset.

4.12. RTC and CMOS RAM

For this chip, RTC is controlled by AS, DS, R/W, and SCRTCN outputs. For setup expansion, a 2KB CMOS RAM is provided.

Among 11 bits address input of the 2KB CMOS RAM, the low 6 bits is connected to the I/O 070H port bits 0–5, and high 5 bits to the latch address bits 10–14. Which is to be selected, RTC or CMOS RAM, when the I/O 071H port is accessed is determined by the data in the I/O 70H bit 6. When "0", RTC is selected and "1" the CMOS RAM. See the figure below for the mapping of the RTC and the CMOS RAM.

4.13. Pseudo-SRAM control

This chip supports control of a maximum 4MB of the pseudo-SRAM. Memory has three address spaces of the system area, EMS control area, and private area. The EMS control area can further be divided into three subsections of conventional area, extended area, and EMS area according to the internal I/O register setting.

(1) System area
The area of 256KB is allocated to 000000H–03FFFFH as the conventional memory.

(2) EMS control area
Address can be allocated to three areas using the internal I/O register setting.
(a) Convectional area
An address space of 384KB can be allocated to 040000–09FFFFH as a conventional memory.
(b) Extended area
Address space can be allocated after 100000H as an extended memory.
(c) EMS area
To support the EMS version 4.0, 34 windows of 16KB increments can be mapped in 040000–09FFFH and 0C8000H–0EFFFH.

(3) Private area
Using the internal I/O register setting, 2 256KB of address space is allocated to 0E0000H–0EFFFFH (access by bank select), which is to be used to save the VRAM contents during the resume and used by the system. It is possible to eliminate the private area by the internal I/O register setting.

4.13.1. System area

Among 4MB memory area supported by the memory controller, a 256KB of address space 000000H–03FFFFH is allocated as a conventional memory, regardless of the internal I/O register setting.

4.13.2. EMS control area

The maximum 4MB area from which excluded the system area and the private area is allocated to the EMS control area, and mapped to the conventional area, extended area, and EMS area by the internal I/O register setting.

There are EMSCFR register, PSRAMCF register, and EMSSTAT register as the internal I/O register controlled, whose bit definition is shown next.

EMSCFR register

Bit	Signal name	Significance
0–2	SW0–2	EMS control register I/O address setting
3, 4	JP2, 3	Extended memory capacity setting (expansion)
5, 6	SW5, 6	Extended memory capacity setting
7	RESERVED	Reserved. Read/write possible

PSRAMCF register

Bit	Signal name	Significance
0	RESERVED	Reserved. Read/write possible
1	INTLV	Pseudo-SRAM interleave access enable
2	*PCS3EN	256KB standard RAM usage setting
3, 4	JP0, 1	Extended memory capacity setting
5	VPTMEM	Private memory access enable
6, 7	MAP0, 1	Private memory bank select

EMSSTAT register

Bit	Signal name	Significance
0–2	SW0–2	State of EMS control register I/O address allocation
3, 4	SW3, 4	Both SW3 and SW4 reads "1" at all times.
5, 6	SW5, 6	State of the extended memory capacity setting
7	EMSEN	EMS on/off setting

The EMSCFR and PSRAMCF registers are allocated to 04H and 05H of the Sharp original port, and reset to "0" when reset.

SW0–2, and SW5–6 of the EMSSTAT register are read only bits which the data written in the EMSCFR register is read. EMSEN is a read/write bit that turns to "0" when reset.

When operated with the CPU clock at 24MHz, INTLV of the PSRAMCF register, is a bit which enables the non-wait access for the conventional memory and private memory interleave mode when the bit is set to "1".

(a) Conventional area

To allocate the memory space 040000H–09FFFFH to a conventional memory, EMSEN of the EMSSTAT register must be set to "0" to disable the EMS.

(b) Extended area

By setting SW5~6, JP2~3, of the EMSCFR register and JP0~1, and *PCS3EN of the PSRAMCF register, the memory space after 100000H can be allocated to the extended memory in a manner as shown next.

SW6	SW5	JP3	JP2	JP1	JP0	*PCS3EN	Extended memory
0	0	*	*	*	*	*	OMB
0	1	*	*	*	*	*	64KB (100000H~10FFFFH)
1	0	0	0	0	0	1	OMB
1	0	0	0	0	0	0	256 KB (100000H~13FFFFH)
1	0	0	0	0	1	1	1MB (100000H~1FFFFH)
1	0	0	0	0	1	0	1.25MB (100000H~23FFFFH)
1	0	0	0	1	0	1	2MB (100000H~2FFFFFH)
1	0	0	0	1	0	0	2.25MB (100000H~33FFFFH)
1	0	0	0	1	1	1	3MB (100000H~3FFFFFH)
1	0	0	0	1	1	0	3.25MB (100000H~43FFFFH)
1	0	0	1	*	*	1	3MB (100000H~3FFFFFH)
1	0	0	1	*	*	0	3.25MB (100000H~43FFFFH)
1	0	1	0	*	*	1	3MB (100000H~3FFFFFH)
1	0	1	0	*	*	0	3.25MB (100000H~43FFFFH)
1	0	1	1	*	*	1	3MB (100000H~3FFFFFH)
1	0	1	1	*	*	0	3.25MB (100000H~43FFFFH)
1	1	*	*	*	*	*	512KB (100000H~17FFFFH)

* : don't care

*PCS3EN is the bit employed to specify the usage of the 256KB area within the standard RAM which may be used as a private area when "1" and as an EMS control area when "0".

(c) EMS area

To turn on the EMS, EMSEN of the EMSSTAT register must be set to "1". To support the EMS version 4.0, the EMSADR register and the EMSDAT register are provided as internal registers, whose bit definition is shown next.

EMSADR register

Bit	Signal name	Significance
0~7	EMSADR0~7	EMS mapping register address

EMSDAT register

Bit	Signal name	Significance
0~7	EMSDAT0~7	EMS mapping register data
8~14	—	Undefined. Reads "0" at all times.
15	EMSPEN	EMS page enable bit

The EMS control register for the EMSADR register, EMSDAT register, including the EMSSTAT register, is I/O address allocated by SW0~2 of the EMSSTAT register, which are set as shown in the table.

SW2	SW1	SW0	EMSSTAT	EMSADR	EMSDATL	EMSDATH
0	0	0	208H	209H	20AH	20BH
0	0	1	218H	219H	21AH	21BH
0	1	0	248H	249H	24AH	24BH
0	1	1	258H	259H	25AH	25BH
1	0	0	268H	269H	26AH	26BH
1	0	1	2A8H	2A9H	2AAH	2ABH
1	1	0	2B8H	2B9H	2BAH	2BBH
1	1	1	2E8H	2E9H	2EAH	2EBH

When reset, SW0~2 are reset to "0".

The EMSADR register is a 8-bit read/write register which is employed to point the 34 EMS mappings using EMSADR2~7. EMSADR2~7 is automatically incremented when the high side of the EMSDAT register is accessed. "0" is always read from EMSDAR0~1 and write is ignored.

The following shows the address setup range for the EMSADR register

40H, 44H, 48H, 4CH, 50H, 54H, 58H, 5CH, 60H, 64H, 68H, 6CH, 70H, 74H, 78H, 7CH, 80H, 84H, 88H, 8CH, 90H, 94H, 98H, 9CH, C8H, CCH, D0H, D4H, D8H, DCH, E0H, E4H, E8H, ECH,

The EMSDAT register is a 16-bit read/write register and there are 34 sections. The EMS mapping data is set in EMSDAT0~7 of the EMSDAT register and determines the page that mapped to the window of address space of 040000H~09FFFFH and 0C8000~0EFFFFH. Window can be set on or off for EMSPEN; sets on when "1" an. EMSDAT8~14 are read "0" at all times and write is ignored.

When the EMSADR register is out of the setup address range, EMSDAT0~15 is read "0" and write is ignored.

The EMS control area equals to the memory controller supported all memory but the system area and the private area, of which capacity is a maximum 3.75MB when the private memory is not used (*PCS3EN=0).

The following shows the mapping of the EMS control area.

"C" represents conventional memory mapping, "X" extended memory mapping, and "P" expanded memory mapping. "nnnnnnH" is dependents to the extended area setting, "mmmmmmH" to the actually installed memory capacity.

The actually installed memory capacity may be set to "nnnnnnH" when mapping the conventional memory. For an example, the extended area for the 4MB memory, it should be set to 3.25MB and "nnnnnnH" is 3DFFFFH (in case *PCS3EN=0).

When mapping the EMS memory, the capacity under the actual memory capacity should be set to "nnnnnnH". For the 4MB of actually installed memory, the EMS area should be set to 0–3.25MB. If 0MB was set, all are mapped as the EMS memory.

4.13.3. Private area

It may be possible with the internal I/O register setting to reserve a 256KB private area out of the memory controller supported 4MB memory.

To reserve the private area, set *PCS3EN of the PSRAMCF register to "1" and set 256KB of the internal standard RAM as the private memory. Set EMSEN of the EMSSTAT register to "0" and PVTMEM of the PSRAMCF register to "1", which is then mapped to the address space of 0E0000H~0EFFFFH.

To access the 256KB private memory, four banks must be selected using MAP0~1 of the PSRAMCF register.

4.14. Port-B

The port-B consists of a logic gate which is used for NMI occurrence control, speaker output control, and refresh detection by the parity and I/O channel checks.

4.15. Sharp original port

To access the Sharp original port, I/O addresses 07CH and 07DH are used. First, set the pointer to 07CH port and read and write the pointer specified port with 07DH. Unless the pointer is set with 07CH, it may not permit to access the Sharp original port of 07DH. Once 07DH has accessed, it needs to set the pointer again.

See the table below for the Sharp original port used by this chip.

Pointer address	Register name	R/W
01H	SIOCFR (SIO Configuration Register)	R/W
02H	PRICNT (Peripheral Control Register)	W/O
03H	MDMCFR (Modem Configuration Register)	R/W
04H	EMSCFR (EMS Configuration Register)	R/W
05H	PSRAMCF (PSRAM Configuration Register)	R/W
06H	PWRCNT (Power Control Register)	R/W
07H	ATSTBY (Auto Stand-by Control Register)	R/W
08H	PWRSTAT (Power Status Register)	R/O
09H	PWRTIM (Power Save Timer Register)	R/W
0AH	RSMTIM (Auto Resume timer Register)	R/W
0BH	RSMCNT (Resume Control Register)	R/W
0CH	RSTFCT (Reset Factor Register)	R/O
0DH	EXSTAT (Expansion Unit Status Register)	R/O
0EH	VGACNT (VGA Control Register)	R/W
0FH	NMIFCT (MNI Factor Register)	R/O

Chips port map (Si)

[1] Access method

① Write the pointer address in the I/O address 22H.

② Read or write the data in the I/O address 23H.
After the 23H has accessed, it may not permit to access the pointer again unless the pointer is set again.

9-3. MC146818 (Real time clock)

Advance Information

REAL-TIME CLOCK PLUS RAM (RTC)

The MC146818 Real-Time Clock plus RAM is a peripheral device which includes the unique MOTEL concept for use with various microprocessors, microcomputers, and larger computers. This part combines three unique features: a complete time-of-day clock with alarm and one hundred year calender, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The MC146818 uses high-speed CMOS technology to interface with 1 MHz processor buses, while consuming very little power.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part (in an otherwise NMOS/TTL system) including all the common battery backed-up functions such as RAM, time, and calender. Secondly, the MC146818 may be used with a CMOS microprocessor to relieve the software of the timekeeping workload and to extend the available RAM of an MPU such as the MC146805E2.

- Low-Power, High-Speed, High-Density CMOS
- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day
- Counts Days of the Week, Date, Month, and Year
- 3 V to 6 V Operation
- Time Base Input Options: 4.194304 MHz, 1.048576 MHz, or 32.768 kHz
- Time Base Oscillator for Parallel Resonant Crystals
- 40 to 200 µW Typical Operating Power at Low Frequency Time Base
- 4.0 to 20 mW Typical Operating Power at High Frequency Time Base
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24-Hour Clock with AM and PM in 12-Hour Mode
- Daylight Savings Time Option
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Microprocessor Bus Compatible
- MOTEL Circuit for Bus Universality
- Multiplexed Bus for Pin Efficiency
- Interfaced with Software as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit Indicates Data Integrity
- Bus Compatible Interrupt Signals ($\overline{IRQ}$)
- Three Interrupts are Separately Software Maskable and Testable
  Time-of-Day Alarm, Once-per-Second to Once-per-Day
  Periodic Rates from 30.5 µs to 500 ms
  End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Clock Output May Be Used as Microprocessor Clock Input At Time Base Frequency ÷ 1 or ÷ 4
- 24-Pin Dual-In-Line Package
- Chip Carrier Also Available

PIN ASSIGNMENT

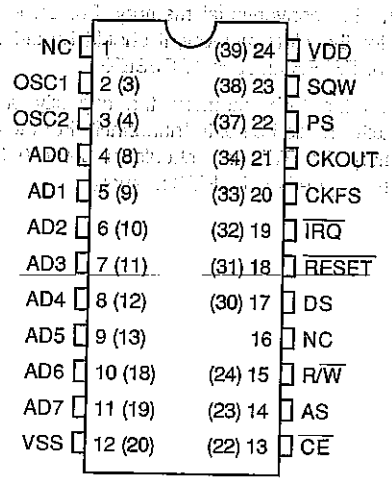


Fig. 9-4

Pin numbers in parentheses represent equivalent Z suffix chip carrier pins. Pins that have not been designated for the chip carrier are not connected.

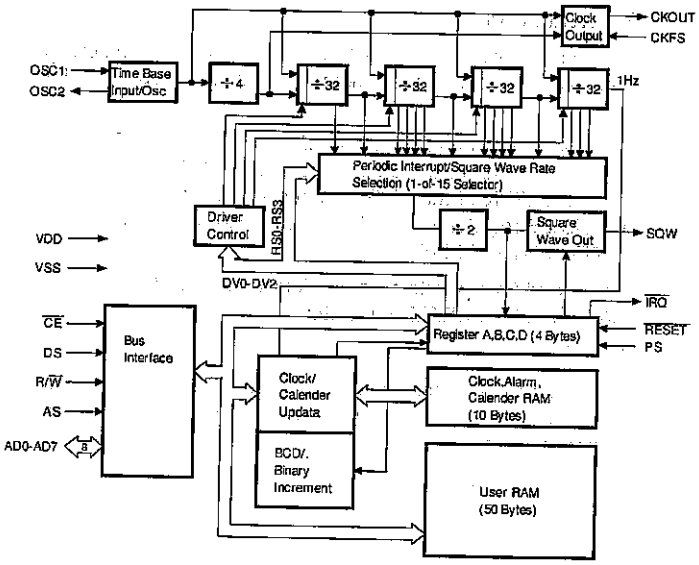
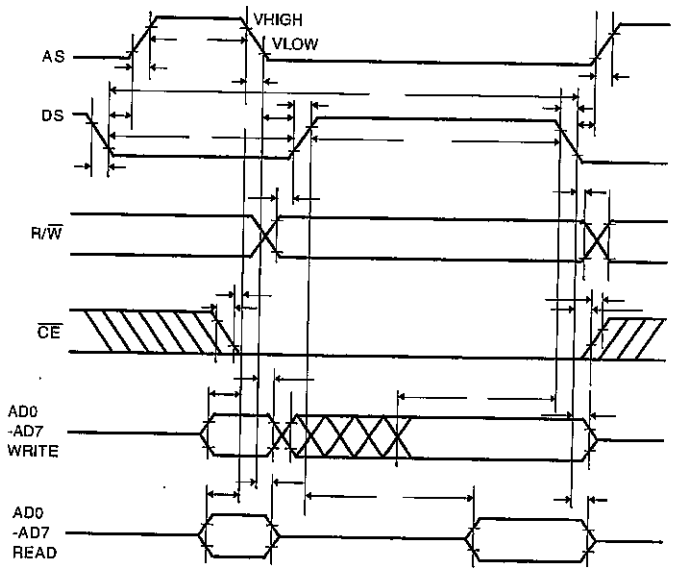


Fig.9-5 Block diagram



NOTE VHIGH=VDD-20V VLOW=0.8V for VDD=5.0V±10%

Fig. 9-6
MC146818 bus timing

SIGNAL DESCRIPTIONS

The block diagram in Figure 1, shows the pin connection with the major internal functions of the MC146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

V_{DD}, V_{SS}

DC power is provided to the part on these two pins, V_{DD} being the more positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC1, OSC2—TIME BASE, INPUTS

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC1. The internal time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant.

AT cut crystal at 4.194304 MHz or 1.048576 MHz frequencies.

CKOUT—CLOCK OUT, OUTPUT

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 9-3.

CKFS—CLOCK OUT FREQUENCY SELECT, INPUT

When the CKFS pin is tied to V_{DD} it causes CKOUT to be the same frequency as the time base at the OSC1 pin. When CKFS is tied to V_{SS}, CKOUT is the OSC1 time-base frequency divided by four. Table 2 summarizes the effect of CKFS.

Time Base (OSC1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304 MHz	High	4.194304 MHz
4.194304 MHz	Low	1.048576 MHz
1.048576 MHz	High	1.048576 MHz
1.048576 MHz	Low	262.144 kHz
32.768 kHz	High	32.768 kHz
32.768 kHz	Low	8.192 kHz

Table 9-3. Clock output frequencies

SQW—SQUARE WAVE, OUTPUT

The SQW pin can output a signal from one of the 15 taps provided by the 22 internal-divider stages. The frequency of the SQW may be altered by programming Register A. The SQW signal may be turned on and off using the SQWE bit in Register B.

AD0–AD7—MULTIPLEXED BIDIRECTIONAL ADDRESS/DATA BUS

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the MC146818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the MC146818 latches the address from AD0 to AD5. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle, the MC146818 outputs eight bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to the high-impedance state) when DS falls in the Motorola case of MOTEL or $\overline{RD}$ rises in the other case.

AS—MULTIPLEXED ADDRESS STROBE, INPUT

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the MC146818. The automatic MOTEL circuit in the MC146818. The automatic MOTEL circuit in the MC146818 also latches the state of the DS pin with the falling edge of AS or ALE.

DS—DATA STROBE OR READ, INPUT

The DS pin has two interpretations via the MOTEL circuit. When emanating from a Motorola type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and ø2 (ø2 clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second MOTEL interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from the competitor type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of DS is also the same as an output-enable signal on a typical memory.

The MOTEL circuit, within the MC146818, latches the state of the DS pin on the falling edge of AS/ALE. When the Motorola mode of MOTEL is desired DS must be low during AS/ALE, which is the case with the Motorola multiplexed bus processors. To ensure the competitor mode of MOTEL, the DS pin must remain high during the time AS/ALE is high.

R/$\overline{W}$—READ/WRITE, INPUT

The MOTEL circuit treats the R/$\overline{W}$ pin in one of two ways. When a Motorola type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, whereas a write cycle is a low on R/$\overline{W}$ during DS.

The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from competitor type processors. The MOTEL circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMs.

$\overline{CE}$—CHIP ENABLE, INPUT

The chip-enable ($\overline{CE}$) signal must be asserted (low) for a bus cycle in which the MC146818 is to be accessed. $\overline{CE}$ is not latched and must be stable during DS and AS (Motorola case of MOTEL) and during $\overline{RD}$ and $\overline{WR}$ (in the other MOTEL case). Bus cycles which take place without asserting $\overline{CE}$ case no actions to take place within the MC146818. When $\overline{CE}$ is high, the multiplexed bus output is in a high impedance state.

When $\overline{CE}$ is high, all address, data, DS, and R/W inputs from the processor are disconnected within the MC146818. This permits the MC146818 to be isolated from a powered-down processor. When $\overline{CE}$ is held high, an unpowered device cannot receive power through the input pins from the real-time clock power source. Battery power consumption can thus be reduced by using a pullup resistor or active clamp on $\overline{CE}$ when the main power is off. When $\overline{CE}$ is not used, it should be grounded.

$\overline{IRQ}$—INTERRUPT REQUEST, OUTPUT

The $\overline{IRQ}$ pin is an active low output of the MC146818 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance estate. Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor.

$\overline{RESET}$—RESET, INPUT

The $\overline{RESET}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{RESET}$ pin must be held low for the specified time, t_{RLH}, in order to allow the power supply to stabilize.

When $\overline{RESET}$ is low the following occurs:

a) Periodic Interrupt Enable (PIE) bit is cleared to zero.

b) Alarm Interrupt Enable (AIE) bit is cleared to zero.

c) Update ended Interrupt Enable (UIE) bit is cleared to zero.

d) Update ended Interrupt Flag (UF) bit is cleared to zero.

e) Interrupt Request status Flag (IRQF) bit is cleared to zero.

f) Periodic Interrupt Flag (PF) bit is cleared to zero.

g) The part is not accessible.

9-4. 82C455 VGA FLAT PANEL/CRT CONTROLLER DATA SHEET

- VGA-Compatible flat panel controller optimized for laptop computer applications.
- Supports CRT, LCD, Plasma and Electro-Luminescent displays of varying resolutions.
- Single chip implementation tightly couples to the CHIPS/250 and CHIPS/280 and interfaces with 8 and 16 bit PC bus and MCA (an interface compatible with the MicroChannel™).
- Up to 40 MHz dot clock speed for graphics and text modes.
- Can utilize an external palette DAC with up to 16 million colors.
- Provides intelligent backward compatibility to the EGA, CGA, Hercules™, and MDA on Flat Panel displays.

The 82C455 Graphics Controller provides a complete solution for implementing a Video Graphics Array-compatible controller. The 82C455 is supplied in a 144-pin PFP package. It can be used in 8 and 16-bit PC bus and in 16-bit MCA bus environments.

Display Types Supported

CGA, EGA, MDA, Multifrequency, IBM PS/2™ and other monitors can be used. The choice of flat panel displays includes EL, plasma, as well as single panel/single drive, dual panel/single drive and dual panel/double drive LCDs. Both gray scale and monochrome panels are supported; a proprietary frame rate control algorithm provides gray scale capability on monochrome panels.

CHIPS/250 and CHIPS/280 Interface

The 82C455 interfaces directly to the CHIPS/250 and CHIPS/280, providing a simple, cost-effective solution for PS/2 compatible systems, When used with one of these CHIPSets®, the 82C455 can execute FAST memory cycles at a speed greater than that normally available on the MCA bus.

Backward Compatibility

The 82C455 is compatible with IBM's EGA, CGA and MDA, in addition to offering a Hercules monochrome-graphics-compatible mode. On-chip compensation registers permit software designed for low resolution displays to utilize the entire screen area on a flat panel with higher resolution.

Hardware Support for Context Switching

Multitasking and windowing environments can be implemented easily since all internal registers of the 82C455 can be read and written.

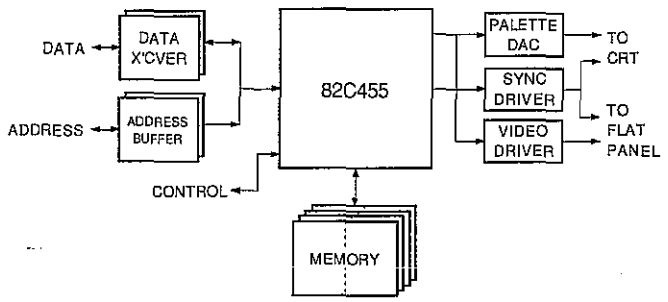


Fig. 9-7 82C455 System Implementation

82C455 Functional Description

The 82C455 offers a complete solution for implementing a VGA/MCGA/EGA/CGA/MDA/Hercules-compatible display system. By integrating all necessary logic the device ensures that total chip count for a VGA-compatible solution can be as low as 14 chips (includes 82C455, display memory, buffers and drivers).

Any one of a variety of CRT monitors or flat panel displays can be driven. Internal compensation registers ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software. The 256 Kbytes of display memory size is comprised of 8 64K*4 DRAMs. Display memory refresh is controlled by the 82C455; it is transparent to the CPU.

For support of multitasking environments and context switching, the entire state of the 82C455 (internal registers and latches) is readable and writeable. This feature is 100% compatible to IBM's VGA.

The 82C455 directly interfaces to 8-bit PC and PC/XT, 16-bit PC/AT and 8 or 16-bit MCA buses. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations and generation of the necessary control signals.

The 82C455 contains 16 color palette registers. It also interfaces directly to an external Inmos G171 (or compatible) color palette and D/A converter. Like the VGA, it is capable of display resolutions of 640*480 with 16 on-screen colors (internal palette) and 320*200 with 256 on-screen colors from an external palette of 256 thousand (or 16 million) colors. The 82C455 can also be programmed for higher resolutions up to 800*600 in 16 colors.

The 82C455 integrates four different modules as follows:

Graphics Controller

The Graphics Controller interfaces the 8 or 16-bit CPU data bus to the 32-bit data bus used by the four planes (Maps) of display memory. It also latches and supplies to the Attribute Controller display memory data for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and an attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller also performs any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Sequencer

The Sequencer generates all CPU and display memory timing signals. It controls CPU access of display memory by inserting cycles dedicated to CPU access and contains mask registers which can prevent writes of individual display memory planes.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and graphic modes the 4-bit pixel data acts as an index into a set of internal palette registers which generate a 6-bit stream. Two additional bits of color data are added if 256-color mode is enabled. Text blink, underline and cursor are also the responsibility of the Attribute Controller.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

Pin Description Table

Flatpack Pin No.	Name	Type	Active	Description
63	AD0	I/O	Both	SYSTEM ADDRESS and DATA Bits 0-15. These bits are used to address display memory and the I/O mapped 82C455 internal registers. They also transfer data between the CPU bus and display memory and 82C455 registers. Addresses must be valid when output signal DATAEN is low and data must be held until\VGACMD (COMMAND) is low. Addresses are latched internally.
62	AD1	I/O	Both	
61	AD2	I/O	Both	
60	AD3	I/O	Both	
59	AD4	I/O	Both	
58	AD5	I/O	Both	
57	AD6	I/O	Both	
56	AD7	I/O	Both	
53	AD8	I/O	Both	
52	AD9	I/O	Both	
51	AD10	I/O	Both	
50	AD11	I/O	Both	
49	AD12	I/O	Both	
48	AD13	I/O	Both	
47	AD14	I/O	Both	
46	AD15	I/O	Both	
44	A16	I	Both	SYSTEM ADDRESS Bits 16-18 and AUXILIARY DATA Bits 0-2. These bits transfer a high-order address when DATAEN is low. The auxiliary data bits on pins A16, A17, and A18 respectively are read into Bits 0-2, respectively, of the DIP Switch register when that register is accessed by the CPU. The address bits are latched internally and are ignored for I/O cycles.
43	A17	I	Both	
42	A18	I	Both	
72	\BHE	I	Low	BYTE HIGH ENABLE and AUXILIARY DATA Bit. \BHE low indicates that the high order byte at the current word address is being accessed. If active, \BHE must be valid when DATAEN is low. The pin is also an auxiliary data input which is read into Bit 3 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This data bit is latched internally on the falling edge of \VGACMD (\IOR).
41	ADDHI	I	High	ADDRESS HI and AUXILIARY DATA Bit. This high order memory address enable input is generated external to the 82C455 by decoding system addresses A19-A23. As an address, it must be valid when DATAEN is low, is latched internally and specifies that the current memory address is valid for the 82C455. This pin is an auxiliary data bit read into Bit 4 of the DIP Switch register when the DIP Switch register is accessed by the CPU. This input pin is ignored during I/O cycles.
67	DATAEN	O	High	DATA ENABLE. The DATAEN output controls external multiplexing of the system address/data bus. DATAEN low selects address and DATAEN high selects data. In an MCA interface, DATAEN is low when \VGACMD is high and DATAEN is high when \VGACMD is low. In a PC or PC/AT bus interface DATAEN is low when all \MEMR, \MEMW, \IOR, and \IOW are high. DATAEN is high when any one of \MEMR, \MEMW, \IOR or \IOW is low.
65	\RDLO	O	Low	READ LO. this output controls the direction of the external data transceivers on the low order byte (Bits 0-7) of the address/data bus. It is low when data is read from the 82C455 and high when data is written to 82C455. DATAEN can be used to enable the external transceiver.
64	\RDHI	O	Low	READ HI. This output operates in a fashion identically to the \RDLO output except that it controls direction for the high order byte (Bits 8-15) of the address/data bus. RDHI is low when data is read from 82C455 and high when data is written to 82C455.
71	M/IO (AEN)	I	Both	MEMORY/IO or ADDRESS ENABLE and AUXILIARY DATA input. In MCA interfaces, the M/IO input pin selects either a memory or an I/O transfer. M/IO high selects a memory cycle and low selects an I/O cycle. When defined as M/IO, it must be valid when the DATAEN input is low. In PC-Bus interfaces, this input is renamed AEN. When low, it indicates a valid I/O address when DATAEN is low. The M/IO (AEN) signal is latched internally. In both MCA and PC-Bus environments this pin serves as an auxiliary data bit input. It is read into Bit 5 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
69	\S0 (\MEMW)	I	Low	S0 or MEMORY WRITE. \S0 is the memory and I/O write input from the MCA bus. In PC-Bus interface applications, this input is named \MEMW. It must be low for CPU writes to display memory.
70	\S1 (\MEMR)	I	Low	S1 or MEMORY READ. \S1 is the memory and I/O read input from the MCA bus. In PC-Bus interface applications, this input is named \MEMR. It must be low to permit the CPU to read display memory.
79	\VGASETUP (\IOW)	I	Low	VGA SETUP or I/O WRITE. In an MCA environment this active low \VGASETUP input allows configuration registers at I/O Addresses 100-104h to be accessed. All other memory and I/O functions are disabled. In PC-BUS interface applications, this input is named \IOW. It must be low to permit the CPU to write to an 82C455 I/O register.
68	\VGACMD (\IOR)	I	Low	VGA COMMAND or I/O READ. In an MCA environment this active low \VGACMD indicates a command bus cycle. \VGACMD must not be asserted during system memory refresh cycles. In a PC-Bus environment this input is named \IOR. It must be low to permit the CPU to read an I/O register.

Table 9-4 (a)

Flatpack Pin No.	Name	Type	Active	Description
80	VGAENAB (\REFRESH)	I	High/Low	VGA ENABLE or REFRESH and AUXILIARY DATA. In an MCA environment this active high VGAENAB input signal enables memory and I/O accesses. In the PC-Bus interface, REFRESH high indicates a valid memory cycle. This pin also serves as an auxiliary data bit input which is read into Bit 6 of the DIP Switch register whenever the DIP Switch register is accessed by the CPU.
78	\VGAREQ (\IOSC16)	O	Low	VGA REQUEST or I/O SELECT 16. In an MCA environment this output indicates that a FAST memory cycle can be executed (this feature can be disabled through a register). In a PC-Bus environment this active low \IOCS16 signal indicates a valid 16 bit I/O cycle.
74	VGARDY	O	Low	VGA READY. when low this output indicates that the current CPU read/write cycle must be extended with wait states.
77	\VGADS16 (\MEN16)	O	Low	VGA ADDRESS SELECT 16 or MEMORY ENABLE 16. In an MCA environment this active low \VGADS16 output indicates that a 16-bit memory or I/O transfer cycle is occurring. In a PC-Bus environment this active low \MEN16 signal indicates a 16-bit memory cycle transfer is enabled. This signal should be used in external logic to decode the high order address and generate \MEMCS16 for the PC-AT bus.
75	\VGAACK (\WR46E8)	O	Low	VGA ACKNOWLEDGE or WRITE 46E8h. In an MCA environment this active low \VGAACK output indicates a valid CPU access (memory and I/O) to the 82C455. In a PC-Bus environment this active low \WR46E8 signal indicates a valid I/O write to address 46E8h.
113	VGAINT	O	Either	VGA INTERRUPT. This pin is asserted whenever the vertical sync signal goes active. This pin can be configured to be active high (EGA) or active low (VGA) through the Emulation Mode register (XR14).
114	RESET	I	High	RESET. An active high input which resets the 82C455.
38	TEST	I	High	TEST. This input is used for factory testing only. It should be tied low.
40 111	PWRDN2 PWRDN1	I I	Both Both	POWER DOWN 2, 1. The POWER DOWN input pins select the Normal, Relax, and Retire modes of operation as follows: PWRDN2 PWRDN1 OPERATION 0 0 Normal Operation 0 1 Relax Mode 1 0 Retire Mode 1 1 Illegal
105 104 103	CLK0 CLK1 CLK2	I I I	Both Both Both	CLQCK 2-0. Video Clock inputs. One of these dot clock inputs is selected by the Miscellaneous Output Register.
101	MCLK	I	Both	MASTER CLOCK. This clock input is used to sequence internal 16-bit I/O cycles.
108	SENSE	I	Both	SENSE. The state of this input pin can be read in Input Status Register 0, Bit 4.
100	\PALRD	O	Low	PALETTE READ. This output is active low during an I/O read to an address in the range 3C6-3C9h and is connected to the Read input of an external Inmos G171 Palette/DAC.
99	\PALWR	O	Low	PALETTE WRITE. This output is active low during an I/O write to an address in the range 3C6-3C9h and is connected to the Write input of an external Inmos G171 Palette/DAC.
142 3 7 12 16 24 28 33	M0D0 M0D1 M0D2 M0D3 M0D4 M0D5 M0D6 M0D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 0 DATA. Display memory data bus for Plane 0 (Map 0).
144 5 10 14 22 26 31 35	M1D0 M1D1 M1D2 M1D3 M1D4 M1D5 M1D6 M1D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 1 DATA. Display memory data bus for Plane 1 (Map 1).
115 118 120 122 124 128 130 132	M2D0 M2D1 M2D2 M2D3 M2D4 M2D5 M2D6 M2D7	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	MEMORY 2 DATA. Display memory data bus for Plane 2 (Map 2).

Table 9-4 (b)

Flatpack Pin No.	Name	Type	Active	Description
116	M3D0	I/O	Both	MEMORY 3 DATA. Display memory data bus for Plane 3 (Map 3).
119	M3D1	I/O	Both	
121	M3D2	I/O	Both	
123	M3D3	I/O	Both	
125	M3D4	I/O	Both	
129	M3D5	I/O	Both	
131	M3D6	I/O	Both	
133	M3D7	I/O	Both	
143	AA0	O	Both	ADDRESS PLANES 0, 1. Display memory address bus for DRAM planes 0 and 1.
4	AA1	O	Both	
8	AA2	O	Both	
13	AA3	O	Both	
21	AA4	O	Both	
25	AA5	O	Both	
29	AA6	O	Both	
34	AA7	O	Both	
141	BA0	O	Both	ADDRESS PLANES 2, 3. Display memory address bus for DRAM Planes 2 and 3.
2	BA1	O	Both	
6	BA2	O	Both	
11	BA3	O	Both	
15	BA4	O	Both	
23	BA5	O	Both	
27	BA6	O	Both	
32	BA7	O	Both	
20	\RAS	O	Low	ROW ADDRESS STROBE. Row address strobe for all DRAM memory banks.
134	\CAS0	O	Low	COLUMN ADDRESS STROBE 0. Active low column address strobe for Memory Plane 0.
135	\CAS1	O	Low	COLUMN ADDRESS STROBE 1. Active low column address strobe for Memory Plane 1.
136	\CAS2	O	Low	COLUMN ADDRESS STROBE 2. Active low column address strobe for Memory Plane 2.
137	\CAS3	O	Low	COLUMN ADDRESS STROBE 3. Active low column address strobe for Memory Plane 3.
139	\WE	O	Low	WRITE ENABLE. Active low write enable signal for all display memory banks/planes.
97	HSYNC	O	Both	HORIZONTAL SYNC OUTPUT. HSYNC is active high if the horizontal polarity bit (Bit 6 of the Miscellaneous Output register; I/O address 3C2) is low. It is active low if the horizontal polarity bit is high.
98	VSYNC	O	Both	VERTICAL SYNC OUTPUT. VSYNC is active high if the vertical polarity bit (Bit 7 of the Miscellaneous Output register; I/O address 3C2) is low. It is active low if the vertical polarity bit is high.
96	BLANK	O	Both	BLANK is a programmable output for blanking the CRT or Flat Panel. Its polarity is programmable. It can be redefined as the Display Enable signal.
85	VIDEO0	O	Both	VIDEO 0-7. Eight video outputs to drive a color or monochrome display devices.
86	VIDEO1	O	Both	Color values for digital CRT interface are assigned as follows:
87	VIDEO2	O	Both	Video0 B Blue
88	VIDEO3	O	Both	Video1 G Green
89	VIDEO4	O	Both	Video2 R Red
93	VIDEO5	O	Both	Video3 BS/V Secondary Blue/Monochrome
94	VIDEO6	O	Both	Video4 GS/I Secondary Green/Intensity
95	VIDEO7	O	Both	Video5 RS Secondary Red
				Video6 User Defined
				Video7 User Defined
92	SHIFTCLK	O	High	SHIFT CLOCK. Output pixel clock to which video output data is synchronized.
83	WGTCLK	O	High	WEIGHT CONTROL CLOCK. Gray scale reference clock for Panels with Pulse Width Modulation support.
17	ACDCLK	O	High	LCD CLOCK. A 50% duty cycle square-wave with programmable period. Used to back bias LCD panels.
140	\ERMEN	O	Low	EARLY MEMORY INDICATOR. This output indicates whether display memory is being accessed by the CPU or by the 82C455 to refresh the display. A high indicates display device access and a low is CPU access. This signal can be redefined as a general purpose output.
112	\TRAP	O	Low	TRAP. This active low output indicates a TRAP condition requiring special CPU assistance. It can be redefined as a general purpose output pin.
82	PTMC	I	Both	PTMC. this input selects the type of CPU interface. PTMC low selects an MCA interface and high selects a PC-Bus interface. This input must always be valid.

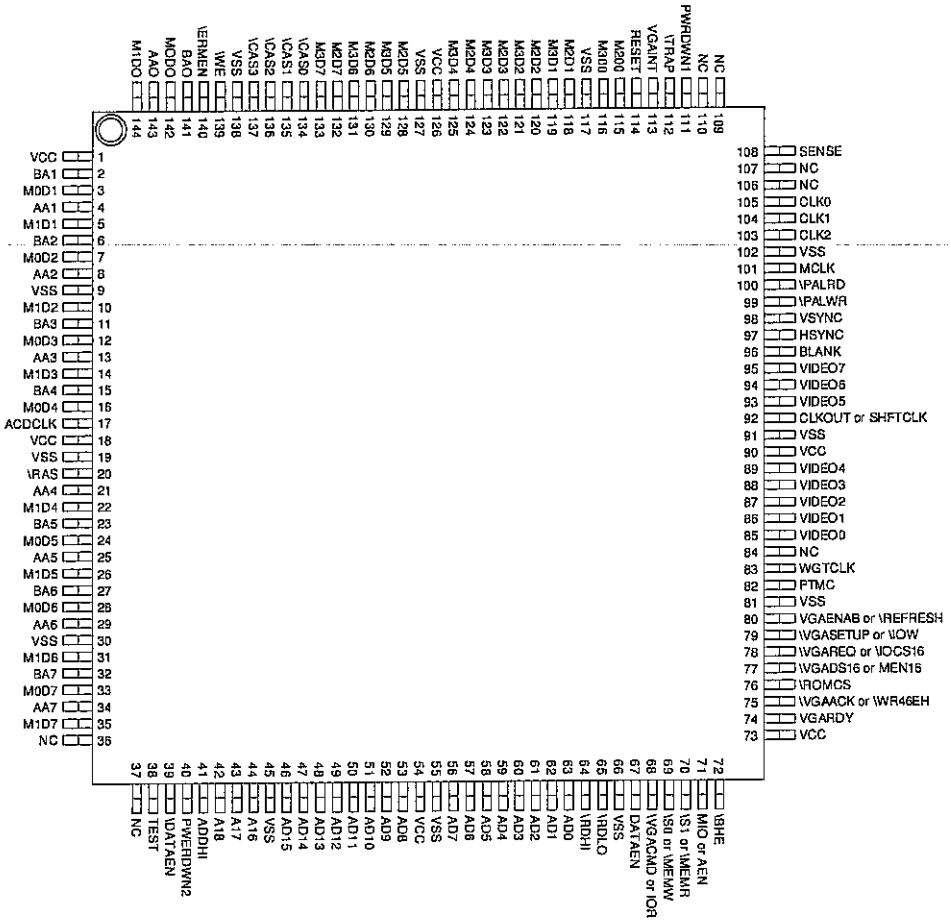


Fig. 9-9 Top view

9-5. μPD80C42 Universal peripheral interface

Features

- Instruction cycle: 1.25μs/12MHz
- Program memory (ROM): 2K x 8 bits
- Data memory (RAM): 128 x 8 bits
- I/O port: 2 x 8 bits
- Async slave master interface
  Two data registers (DBBIN,, DBBOUT)
  8-BIT STATUS
- Internal timer/counter: 8 bits
- A pair of working registers
- 8-level stack
- Internal clock oscillation circuit
- Interrupt function
- DMA function
- Expandable I/O port
- Single step operation

Block diagram

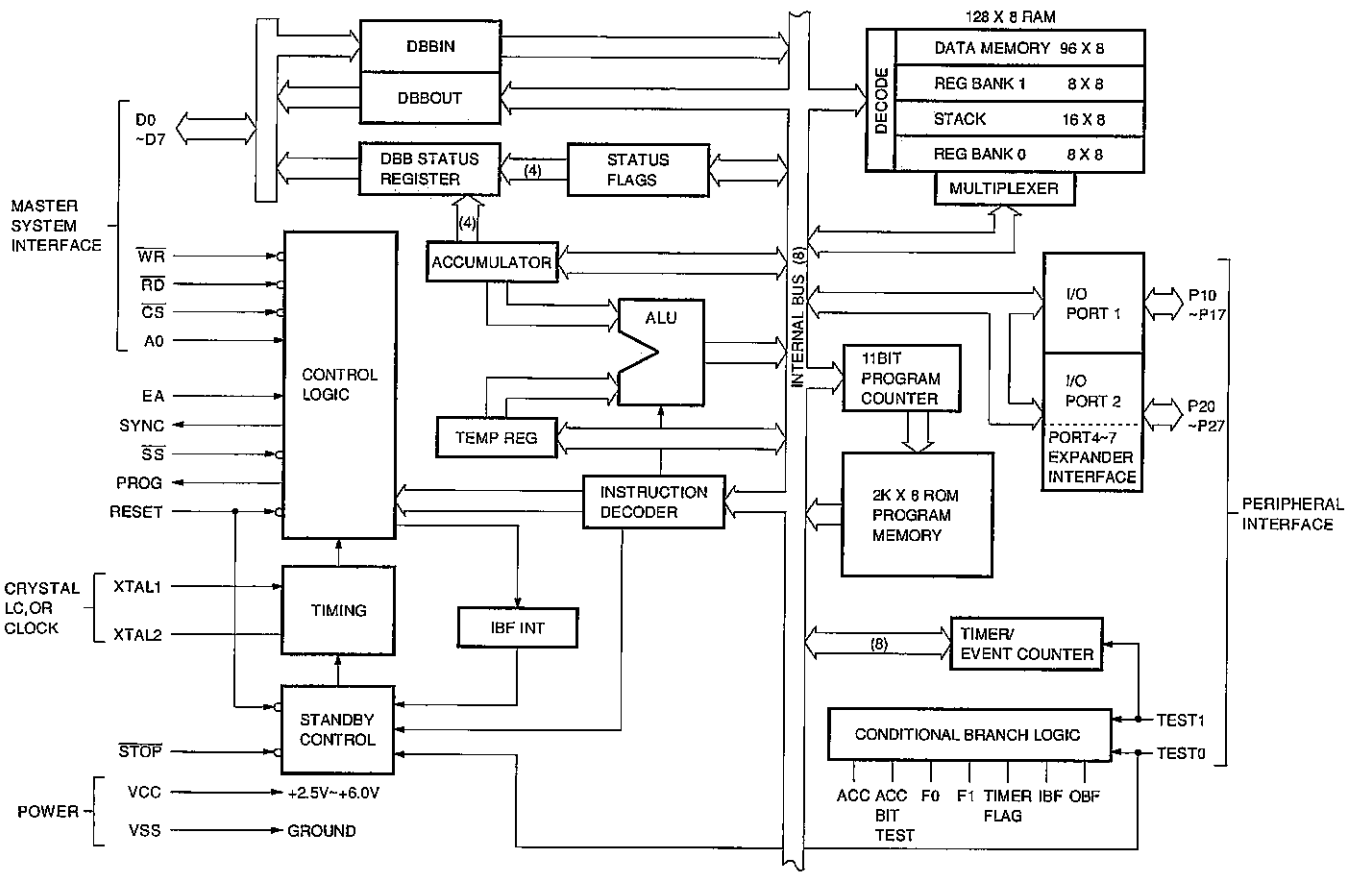


Fig. 9-9

9-6. TC51128AFL-80 CMOS PSEUDO-STATIC RAM (131,072 WORDS X 8 BITS)

General

The TC518128AFL is a single 5V operated 131,072 words x 8 bits pseudo-static RAM. It realized a large capacity, high speed, and low power dissipation by a combination of single transistor type dynamic memory cell and peripheral CMOS static circuit. With the TC518128AFL, auto refresh and self-refresh can easily be achieved with -RFSH input, and, similar as an async static RAM, the R/W input is accepted at a low to high transition of R/W, which enhances easier interface with microcomputer.

The TC518128AFL is pin compatible with 1MB static RAM (JEDEC standard) and a package of 0.3" wide, 32-pin SOP mini-flat static package is used.

Refresh can be done by selecting 512 address (A0~A8) within 8ms.

Features

t_{CEA}	Access time	80ns
t_{OEA}	$\overline{OE}$ access time	35ns
t_{RC}	Cycle time	130ns
P_D	Operating power dissipation	385mW
Self-refresh current		1mA/220μA

- Large capacity:, 131,072 words x 8 bits
- High speed, low power dissipation
- Single 5V supply: 5V±10%
- Auto refresh possible by the internal counter
- Self-refresh possible by the internal counter
- All input/output are TTL compatible
- 512 refresh cycle/8ms
- Adoption of the auto refresh power down function
- Pin compatible with 1M static RAM (JEDEC standard)
- 32-pin mini-flat package

Pin configuration

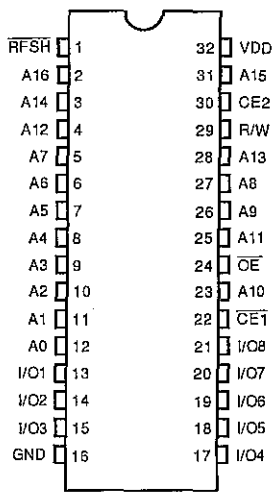


Fig. 9-10

Pin name

A0~A16	Address input
R/W	Read/write input
$\overline{OE}$	Output enable input
$\overline{RFSH}$	Refresh input
$\overline{CE1}$, CE2	Chip enable input
I/01~I/08	Data input/output
V_{DD}	Power supply
GND	GND

Block diagram

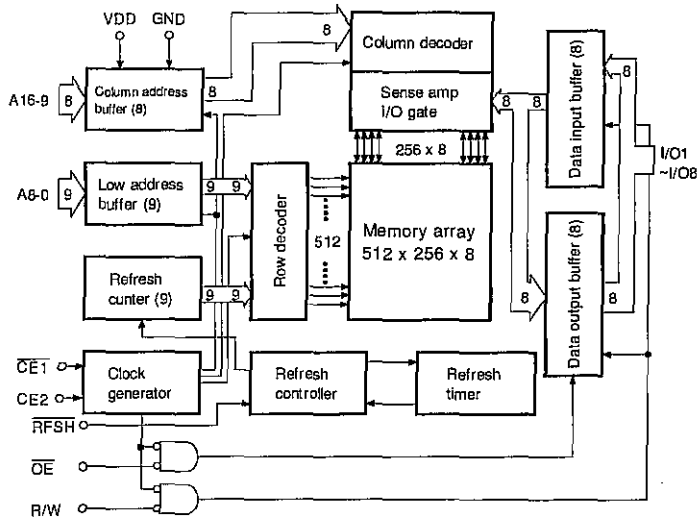


Fig. 9-11

9-7. M5M27C102FP ONE TIME PROM FOR BIOS

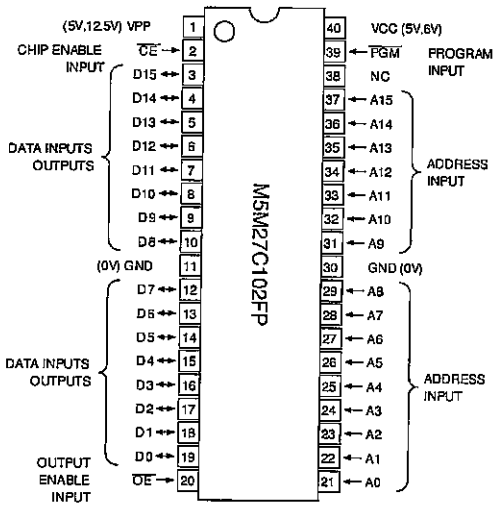
DESCRIPTION

The M5M27C102FP is high-speed 1048576-bit one time programmable read only memories. They are suitable for microprocessor programming applilications where rapid turn-around is required. The M5M27C102FP are fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and are available in 40 pin (DIP, SOP, VSOP) or 44 pin (PLCC) plastic packages.

FEATURES

- 65536 word x 16 bit organization
- Package SOP (525 mil) M5M27C102FP
- Access time .....200ns (max.)
- Programming voltage: 12.5V
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (Icc): Active..... 50mA (max.)
  Stand by ..... 1mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Word programming algorithm
- Page programming algorithm

PIN CONFIGURATION (TOP VIEW)



Outline 40P2M (SOP : FP)

Fig. 9-12

9-8. SC9871 DMAC

9-8-1. DMAC general description

The DMAC function is stored in the SC9871.

Two 8237 DMACs are contained in this controller which supports 7 DMA channels. The DMA controller-1 operates as a slave to carry out the DMA transfer for CH0~3 in byte increment. The DMA controller-2 operates as a master to carry out the DMA transfer for CH4~7 in 16-bit increment. CH4 is used for the cascade connection. The rate transferred at a time is 64KB for CH0~3 and 128KB for CH4~7. The transfer area is 16MB whose high order area is set to the page register within the superintegration.

Channel allocation

CH0 : I/O slot
CH1 : I/O slot
CH2 : Floppy disk + I/O slot
CH3 : I/O slot
CH4 : For cascade connection
CH5 : I/O slot
CH6 : I/O slot
CH7 : I/O slot

I/O address

Described next is I/O address.

00H : CH0 base, current address
01H : CH0 base, current address
02H : CH1 base, current address
03H : CH1 base, current address
04H : CH2 base, current address
05H : CH2 base, current address
06H : CH3 base, current address
07H : CH3 base, current address
08H : DMAC 1 command, status register
09H : DMAC 1 request register
0AH : DMAC 1 single mask register
0BH : DMAC 1 mode register
0CH : DMAC 1 clear byte point register
0DH : DMAC 1 master clear
0EH : DMAC 1 clear mask register
0FH : DMAC 1 all mask register
C0H : CH4 base current address
C2H : CH4 base current address
C4H : CH5 base current address
C6H : CH5 base current address
C8H : CH6 base current address
CAH : CH6 base current address
CCH : CH7 base current address
CEH : CH7 base current address
D0H : DMAC 2 command, status register
D2H : DMAC 2 request register
D4H : DMAC 2 single mask register
D6H : DMAC 2 mode register
D8H : DMAC 2 clear byte point register
DAH : DMAC 2 master clear

DCH: DMAC 2 clear mask register

DEH: DMAC 2 all mask register

DMAC 1 address and count must be set in increment of a byte. The address of DMAC 2 is possible for DMA due to a 16-bit word environment and a half of the actual address is used to set.

Page register

87H : DMAC CH0 page address

83H : DMAC CH1 page address

81H : DMAC CH2 page address

82H : DMAC CH3 page address

8BH : DMAC CH5 page address

89H : DMAC CH6 page address

8AH : DMAC CH7 page address

8FH : High address during DRAM refresh

80H : MFG port

84, 85, 86, 88, 8C, and 8EH are reserved.

In the page register is set the DMA address A23~16. But, for the DMAC 2, the LSB of the page register is insignificant because the DMAC is an output for A16.

DREQ/DACK signal are connected to the I/O slots, but, the internal FDC is connected for the channel 2 of the slave when the bit 3 of the 3F3H/372H port is at "1".

9-8-2. DMAC block diagram (SC9871)

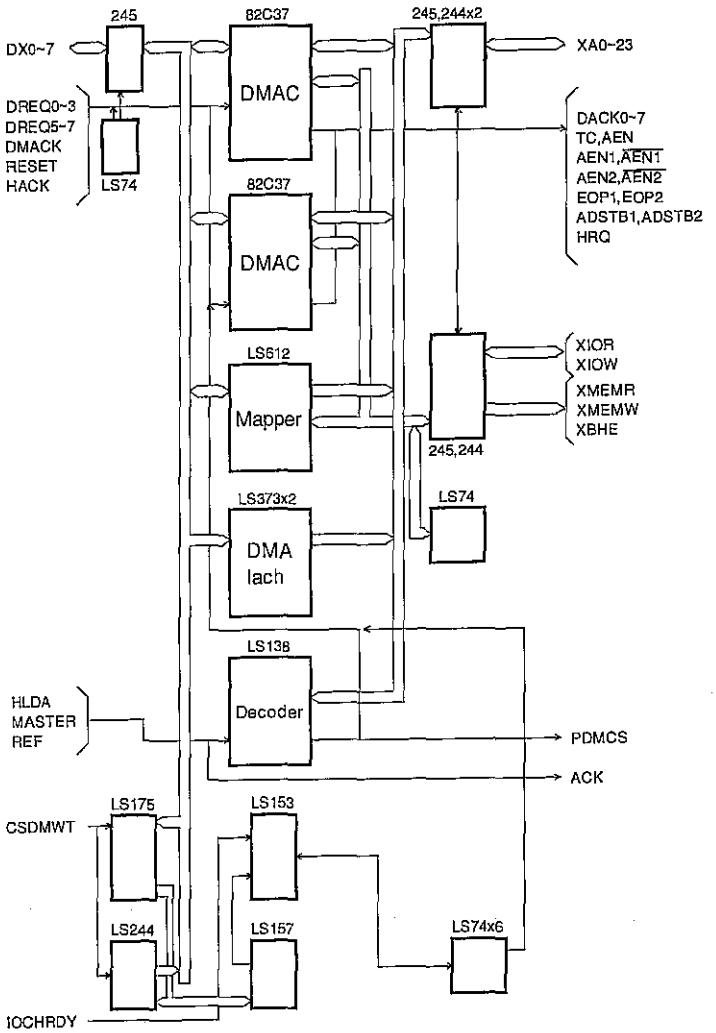


Fig. 9-13

9-8-3. Configuration register

Can be accessed when the register number is set in the configuration register 22H and the set value is outputted to the address 23H.

- 22H: Register number (write only)
- 23H: Value to be set in the register (read/write possible).

There are some registers provided, but explanation will be given here for the register number 01H which is DMAC related.

Register number 01H (read/write port)

7							0
X	X	16W1	16W0	8W1	8W0	X	X

Default .... ALL "0"

The register to which set the DMA wait control.

Table

Set value		DMAC 2 waits
16W1	16W0	
0	0	1 wait
0	1	2 waits
1	0	3 waits
1	1	4 waits

Set value		DMAC 1 waits
8W1	8W0	
0	0	1 wait
0	1	2 waits
1	0	3 waits
1	1	4 waits

DMAC 2 is for 16-bit transfer (master DMAC)

DMAC 1 is for 8-bit transfer (slave DMAC)

9-8-4. SC9871 DMAC signal descriptions

PIN No.	NAME	I/O	Function
1~5	TXA0~5		Not used.
6~7 9~15 17 18~24 26~32	XA0~1 XA2~8 XA9 XA10~16 XA17~23	B B B O O	System address bus
33~36	DACK0~3	O	Response to 8-bit transfer request for DREQ0~3.
37	DACK4	O	Not used.
38~40	DACK5~7	O	Response to 16-bit transfer request for DREQ5~7.
42	AEN	O	Not used.
43	AEN1	O	Not used.
44	AEN2	O	Not used.
45	AEN1B	O	Address enable
46	AEN2B	O	Not used.
47	ADSTB1	O	Not used.
48	ADSTB2	O	Not used.
49	EOP1	O	Not used.
50	EOP2	O	Not used.
51	TC	O	DMA complete signal
52	HRQ	O	Hold request, to system gate array
53	HRQ	O	Not used.
54	ACK	O	Not used.
55	TEST	I	Fixed LOW
56	GATERDY	O	Not used.
58	XIOR	B	I/O read
59	XIOW	B	I/O write
60	TXIOR		Not used.
61	TXIOW		Not used.
62	XBHE	O	Byte high enable
63 65~71	XD0 XD1~7	B B	System data bus
73~80	TXD0~7		Not used.
81	XMEMR	O	System bus memory read MEMRC
82	XMEMW	O	System bus memory write MEMWC
83	TEST CK	I	Fixed LOW
84	TSTNORT	I	Fixed HIGH
85	IOCHRDY	I	AT bus IOCHRDY signal
86	CSDMWT	I	Indicates the configuration register access inside the DMAC that indicates the 23H is accessed following to 22H 01.
87	REF	I	Indicates the refresh cycle.
88	MASTER	I	AT bus master signal input. Indicates that the AT bus has became the bus master.
89	RESET	I	Reset
91~94	DREQ0~3	I	8-bit DMA request signal
95~97	DREQ5~7	I	16-bit DMA request signal
98	DMACLK	I	4MHz DMA clock
99	HACK	I	Hold acknowledge
100	HLDA	I	CPU HLDA signal that indicates that the CPU released the bus.

9-9. LZ95H22

9-9-1. General

The DOS_ROM, VGA, and printer interface are contained in a single chip for the PC-6220.

(1) DOS-ROM interface
Supports the same features as the ROM board.

(2) VGA interface
Creates the memory and I/O chip select signals.

(3) Printer interface
Supports the parallel port functions of the IBM serial/parallel board. Ports 1 and 2 are set by the Sharp original port.

(4) 8042 hard disk interface select signal generation

(5) Others
Drive select signal generation
Key board select signal generation
CRT display select signal generation
Drive access LED internal/external key selection

9-9-2. I/O address

The following I/O ports exist in the gate array.

① Sharp original port

② DOS-ROM interface port

③ Printer interface port

④ Hard disk interface, 8042 decoder

⑤ FDD control signal port

See the table next for the relationship between address and port

AEN	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	HEX	
1	X	X	X	X	X	X	X	X	X	X	XXX	Not selected
0	0	0	0	1	1	1	1	1	0	0	7C	Sharp port pointer (WO)
0	0	0	0	1	1	1	1	1	0	1	7D	Sharp port data (R/W)
0	0	1	#	#	#	#	1	0	0	0	1#8	DOSROM port pointer (WO)
0	0	1	#	#	#	#	1	0	0	1	1#9	DOSROM port data (R/W)
0	0	1	#	#	#	#	1	0	1	0	1#A	DOSROM port reserved (R/W)
0	0	1	#	#	#	#	1	0	1	1	1#B	DOSROM port ID (R/W)
0	1	$	0	1	1	1	1	0	0	0	$78	Printer port data (R/W)
0	1	$	0	1	1	1	1	0	0	1	$79	Printer port status (RO)
0	1	$	0	1	1	1	1	0	1	0	$7A	Printer port control (R/W)
0	1	1	1	1	0	0	1	1	1	0	3CE	VGA port
0	1	1	1	1	0	0	1	1	1	1	3CF	VGA port
0	0	0	0	1	1	0	0	X	0	0	60, 64	-CS8042 signal output
0	0	1	%	1	1	1	0	X	X	X	1F0~7	-HDCS0 signal output
0	1	1	%	1	1	1	0	1	1	X	3F6,7	-HDCS1 signal output
0	1	1	1	1	1	1	0	0	1	0	3F2	FDD select signal output

#: Set by the Sharp original port 12H.

$: Set by the Sharp original port 02H.

%: Set by the Sharp original port 02H.

X: Don't care

9-9-3. Sharp original port

① Access method
After setting the register number in the pointer port of 7CH, make access through 7DH. For the pointer of 7CH is cleared after the data port of 7DH is accessed, the register number needs to be set to the pointer port of 7CH again in order to access the data port of 7DH once more.

② Register 01H [W/O]
Read port is within SI.

BIT	7	6	5	4	3	2	1	0	
	*								Not Used
		*							-LCD, CRT
			*						-INTKEY
				*					SIO SEL (Not used in this GA)
					*				SIO EN
						*			FDD SEL 2 (Not used in this GA)
							*		FDD SEL 1 (Not used in this GA)
								*	FDD SEL 0 (Not used in this GA)

-LCD, CRT 0: LCD MODE 1: CRT MODE

-INTKEY 0: INTERNAL KEYBOARD ENABLE
1: INTERNAL KEYBOARD DISABLE (IF EXTERNAL KEYBOARD INSTALLED)

SIO EN 0: INTERNAL SIO ENABLE 1: INTERNAL SIO ISABLE
SIO_EN can also be changed by the register 2.

② Register 02H [R/W] Write port is within SI.

BIT	7	6	5	4	3	2	1	0	
	*								HD EN
		*							HD SEL
			*						SIO EN
				*					SIO SEL (Not used in this GA) @
					*				PRT EN
						*			PRT SEL
							*		IMS EN (Not used in this GA) @
								*	IMS SEL(Not used in this GA) @

HD EN 0: HD port enable 1: HD port disable

HD SEL 0: Primary setting 1: Secondary setting

PRT EN 0: Printer port enable 1: Printer port disable

PRT SEL 0: Port 1 setting (378H~37AH) 1: Port 2 setting (278H~27AH)

SIO EN 0: Internal SIO enable 1: Internal SIO disable See register 1.

NOTE @: A bit exists in the register.

③ Register 0EH [W/O] Read port is within SI.

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					PRINTER BUSY CONTROL
					*	*			PWRDWN2, PWRDWN1 (Not used in this GA)
							*		VGA_EN

VGA_EN 0: Internal VGA enable 1: Internal VGA disable

Printer busy control 0: Normal, busy in the status port indicates the state of the line.
1: Forced to the busy state by the strobe and cancelled by -ACK.

④ Register 12H [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Reserved.
					*	*	*	*	ID2SW3~0

ID2SW3~0: The value "X" is set for the port address 1X8~BH.

⑤ The register 11~1FH is kept for software address.

9-9-4. DOSROM port

① Access method

After the register number is set to the pointer port of 1X8H, access is made through 1X9H.
Existence of the DOSROM port is recognized by the 1XBH port.
The value "X" is set by the Sharp original port (pointer 12).

② Register group

Pointer register (1X8H)	Data register (1X9H)
00h	Memory data read/write
01h	Chip select register
02h	Memory mapper register
03h	Address register 1
04h	Address register 2
05h	Address register 3

Control register: 1XAH

ID register: 1XBH

③ Explanation of register

∘ Pointer register: 1X8H

BIT	7	6	5	4	3	2	1	0	
						*	*	*	Data register pointer
				*	*				Reserved.
		*							Test bit
	*								Reset

Data register pointer: The register to be accessed through the data register 1X9H.

Test bit: For counter clear, normally set to "0".

Reset: 1: Same function as the hardware reset. The 1X9H related register keeps the reset state.
0: During normal operation

Reserved: Normally set to "0".

NOTE: Since the pointer set is kept until written next, it needs no setting when the same register is to be read or written next.

∘ ROM data read: Pointer 00H [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Memory data

ROM data port when accessing the I/O.

Write is valid only when the RAM is installed.

∘ Chip select register: Pointer 01H

BIT	7	6	5	4	3	2	1	0	
						*	*	*	Chip select
	*			*	*				Reserved.
			*						Reserved @.
		*							Address auto increment

- Chip select
  010: DOSROM1 (enabled only for 8-bit access)
  011: DOSROM2 (enabled only for 8-bit access)
  100: Reserved
  101: Reserved
  110: Reserved
  111: Reserved

- Address auto increment
  0: The contents of the address register are not incremented when the I/O is accessed.
  1: The contents of the address register are incremented when the I/O is accessed.

NOTE: Set to 00H when reset.

NOTE @: A bit exists in the register.

∘ Memory map register: Pointer 02H

BIT	7	6	5	4	3	2	1	0	
			*	*	*	*	*	*	Memory base address
		*							8/16 access
	*								Memory access enabled

Within the 1MB system address space, the base address is set for a 64KB window at a boundary of 16KB.

Setting is possible 010000~111100.

With the software,
101100 B0000~BFFFF (Disabled depending on the display mode)
110100 D0000~DFFFF
110101 D4000~E3FFF
110110 DS000~E7FFF
110111 DC000~EBFFF
111000 E0000~EFFFF 6 kinds of setting enabled

Disabled addresses are:
00XXXX 00000~3FFFF
C0000~CFFFF (disabled)
1111XX F0000~FFFFF

8/16 access
Selection is made whether the 64KB space set operate as an 8-bit memory or 16-bit memory.
0: Only 8-bit access is enabled.
1: 16-bit access is enabled.

Memory access enable/disable 0: Disable 1: Enable

NOTE: Set to 38H when reset and CPU is reset (test cycle detection of FEH to I/O 64H)

∘ Address pointer 1: Pointer 03H

BIT	7	6	5	4	3	2	1	0	
				*	*	*	*	*	Expansion address
	*	*	*						Reserved.

Expansion address, EA20~EA16: Specified which 64KB sector of a 2MB memory card is to be mapped to a window.

Reserved. Set to "0" when writing, and "0" when reading

NOTE: Set to 00H when reset.

∘ Address register 2: Pointer 04H

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Memory address, AD15~AD08

Memory card address AD15~AD08 when accessing the ROM.

NOTE: Set to 00H when reset.

∘ Address register 3: Pointer 05H

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Memory address

Memory card address AD07~AD00 when accessing the DOSROM. The address registers 2 and 3 are auto incremented according to the setting when accessing I/O. (Subsequent address is turned to 0H when the contents of the address registers 2 and 3 are 0FFFFH and carry is not reflected to the address register 1. In the test mode, count increments at every digit.

NOTE: Set to 00H when reset.

° Control register" 1XAH [R/W]

BIT	7	6	5	4	3	2	1	0	
	*								Serial in (not used)
		*	*	*	*				Reserved.
						*			IDMEME
							*		IDMEME
								*	Serial out (not used)

RESCPUE 0: Reset CPU monitor enable
The 1X9 and 1XA registers within this gate array are reset when FEH is written in the address 64H.
1: Reset CPU monitor disable
The 1X9 and 1XA registers within this gate array are not reset when FEH is written in the address 64H.

IDMEME 0: Memory access enabled when ID changed.
1: Memory access disabled when ID changed.

Others Reserved.

NOTE: Set to 00H when reset.

° ID register: 1XBH

BIT	7	6	5	4	3	2	1	0	
	1	1	0	0	1	1	0	1	LSI code
	0	0	0	0	0	0	1	0	Board ID

LSI code and ID code are read alternately. The LSI code is read immediately after reset.

LSI code: CDH
Board code: 02H

Any board to be developed next will be allocated with 03H through 0FH.
When the board ID is written in the ID register, the board is enabled. If disabled, read/write to any register is not enabled.

* Recognition method

02H → ID register
ID register read x 2 OCDH&02h → Yes → interface exists

9-9-5. Printer port

The printer port consists of three internal ports and external input/output. The board address can be selected using the Sharp port bit PRT_EN and PRT_SEL, as shown in the table below.

PRT_EN	PRT_SEL	I/O address	Port name
1	X	Not selected	
0	0	37xH	Printer port 1
0	1	27xH	Printer port 2

° Print data (I/O address, 378H/278H) [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*	*	Printer output data

° Printer status (I/O address, 379H/279H) [R/W]

BIT	7	6	5	4	3	2	1	0	
	*								-BUSY
		*							-ACK
			*						PE
				*					SELCT
					*				-ERROR
						*	x	x	

-BUSY: Printer busy signal 0: Busy

-ACK: Printer acknowledge signal 0: Acknowledge

PE: Paper empty signal 1: Paper empty

SELF: Printer select signal. Selection of the printer is informed to the gate array. 1: Printer selected

-ERR: Printer error 0: Printer error.

A printer error is informed to the gate array.

x: Don't care.

° Printer control (I/O address, 37AH/27AH) [R/W]

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Don't care
				*					ENIR
					*				SEL
						*			-INIT
							*		AUTFDX
								*	STROBE

ENIR: Printer port interrupt enable 1: Interrupt enabled with -ACK.

SEL: Printer select 1: Printer selected

-INIT: Printer initialization 0: Initialization (50$s/min)

ATFD: Auto feed 1: Linefeed with a CR code (CR/LF)

STB: Printer data strobe signal

Don't care: Not affected (during write) 0: (During read)

9-6-6. Hard disk selection

Generates the AT bus interface hard disk drive select signal.

HD_EN	HD_SEL	-HDCS0	-HDCS1
1	X	Not active	Not active
0	0	Active through 1FO~1F7	Active through 3F6~3F7
0	1	Active through 170~177	Active through 376~377

9-9-7. FDD selection (I/O address: 3F2H) [WO]

BIT	7	6	5	4	3	2	1	0	
	*								DRIVE D MOTOR ENABLE (Not used)
		*							DRIVE C MOTOR ENABLE (Not used)
			*						DRIVE B MOTOR ENABLE
				*					DRIVE A MOTOR ENABLE
					*				ENABLE IRQ & DMA (Not used)
						*			FDC RESET (Not used)
							*	*	DRIVE SELECT (Not used)

When the FDD is selected, (BIT 5, BIT 4) = (1, 0), (0, 1), (1, 1).
To turn on the floppy disk access lamp, set FDSELF to "1".

NOTE: Set to 00H when reset.

9-9-8. VGA port (I/O address: 3CEH, ECFH) [W/O]

Working range of the display memory is set.

① Access method
Write the pointer 06H in the register of 3CEH to put the 3CFH port active.

② Register group
3CEH Graphic address
3CFH Miscellaneous register

③ Explanation of register

Graphics address 3CEH [W/O]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					NOT USED
					*	*	*	*	INDEX TO GRAPHICS CONTROLLER DATA REGISTERS

Index: 0110: 3CFH is enabled to write.
Other: 0110: 3CFH is disabled to write.

(Reference): Because this gate array consists of a 1-bit register, no signal is assumed for other than 06H.

Miscellaneous register 3CFH [W/O]

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					NOT USED
					*				MEMORY MAP 1
						*			MEMORY MAP 0
							*		CHAIN ODD EVEN PLANES (Not used in this GA)
								*	GRAPHICS/TEXT MODE (Not used in this GA)

VRAM address is specified by the memory map.

MAP 1	MAP 0	Address used
0	0	A0000H~BFFFFH
0	1	A0000H~AFFFFH
1	0	B0000H~BFFFFH
1	1	B8000H~BFFFFH

NOTE: Set to 00H when reset.

9-9-9. Signal descriptions

① The signal name preceded with a "-" represents active low signal.

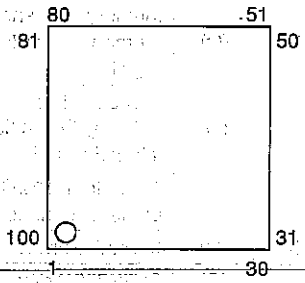
② The column next to the signal name indicates: (I) for input, (O) for output, (I/O) for input/output.

Signal name	I/O	Explanation
-LMSEL	(I)	When all addresses A20~A23 are at 0, this signal turns low and cannot be latched by ALE when the CPU accesses. Used for the memory decode enable signal.
A19~A1	(I)	Memory address 19~1. Not ALE latched when the CPU accesses. Incorporates a pullup resistor.
XA0	(I)	Memory address 0. Latched by ALE when the CPU accesses. Incorporates a pullup resistor.
AEN	(I)	Address enable signal that goes high during the DMA access. With a "0" state of the signal, it is used for the enable signal of the I/O decode circuit.
ALE	(I)	Address latch enable signal during the CPU access. Fixed high other than when the CPU access.
XD7~XD0	(I/O)	CPU side data bus (low side).
MEMR	(I)	Memory read command. Output for any space of 16MB.
-MEMW	(I)	Memory write command, Output for any space of 16MB.
-IOR	(I)	I/O read command.
-IOW	(I)	I/O write command.
RESET	(I)	System reset command. Schmidt input.
-SELTM	(O)	I/0 select signal for within the gate array. Turns active when accessing the printer I/O, RAM I/O, hard disk I/O, floppy disk I/O, -SELMD, -SELEXIO.
-SELMD	(I)	Select return signal from the modem connector. In the case of a device other than the modem, the select signal needs to be added to this line. Incorporates a pullup resistor.
-SELEXIO	(I)	Select return signal from an expansion unit. When using the XD0~7 bus by the expansion unit, the select signal must be an input to this line. Incorporates a pullup resistor. If the signal is active when the internal printer port is selected, it treated invalid as the expansion unit side port takes preference by the internal printer logic.
-MEMCS16	(O)	16-bit memory access request signal. Turns active when accessing the VGA VRAM and accessing the ROM memory with the memory mapper register bit 6 is at "1". Open drain output.
-MEN16	(I)	VRAM 16-bit access enable signal (VGA). 0: Enabled (MEMCS16 issued) 1: Disabled (MEGA) Enables the VGA to access the 16-bit. Controls MEMCS16.
-RMEM16	(I)	ROM memory access enable signal. Controls MEMCS16. 0: Enabled (MEMCS16 issued). 1: Disabled.
IRQ7	(O)	Parallel port 1 interrupt request signal. High impedance when not used.

Signal name	I/O	Explanation
IRQ5	(O)	Parallel port 2 interrupt request signal. High impedance when not used.
-CS8042	(O)	8042 key controller chip select signal. Active address 60H, 64H.
-HDCS0	(O)	Hard disk chip select signal.
-HDCS1	(I)	Hard disk chip select signal. HD_EN HD_SEL -HDCS0 -HDCS1 1 X Not active. 0 0 1F0~1F7 3F6~3F7 0 1 170~177 376~377
-INTKEY	(O)	Internal keyboard enable signal. Contents of the Sharp original port 01, bit 5. 0: Internal 1: External
-EN_CRT	(O)	CRT display enable signal. Turns active when the VGA_EN bit is "0" with the contents of the Sharp original port 01 bit 6 in the CRT mode. L: CRT display mode -LCD/CRT inversion issued.
VGAAEN	(O)	VGA chip select signal. Turns low when the bit 1 of the AEN input is at a "0" with the bit 1 of the Sharp original port 0E (VGA_EN) at "0".
VGACS	(O)	VGA memory chip select signal. Turns "1" when the bit 1 of the Sharp original port 0E (VGA_EN) is at a "0" with -LMSEL at 0, A19 at 1, A18 at 0 and A17 at 1.
-READY	(I)	VRAM ready signal.
IOCHRDY	(O)	System ready signal. Open drain output. Turns low with a "0" state of the -READY signal.
AD0~7	(I/O)	Address multiplex bus. Hands down the address and data to the ROM and the printer. AD0 is an input when word accessing to DOSROM. In the normal operation mode, XA0 and A1~7 latch signals are issued. When accessing the ROM I/O, the contents of the address register 3 is issued. When the printer data is written, XD0~7 are issued. When printer control is written, the printer data is issued. When the printer status is read, it is in the input mode in the floating mode.
AD8~15	(O)	In the normal operating mode, A8~15 latch signal. When ROM I/O is accessed, the contents of the address register 2 are issued. When accessing the ROM, AD14 and 15 are converted. Low order two bits of the mapping register. 00 01 10 11 00→00 01→00 10→00 11→00 A14, A15→AD14, AD15 01→01 10→01 11→01 00→01 10→10 11→10 00→10 01→10 11→11 00→11 01→11 10→11
EA16~20	(O)	In the normal operating time, A16~19, -LMSEL latch signal. When accessing the ROM I/O, the contents of the address register 1 are issued.
-MEMWE	(O)	Memory write enable signal for Sharp memory
-MEMOE	(O)	Memory out enable signal for Sharp memory

Signal name	I/O	Explanation
-MEMCE0~3	(O)	Memory chip enable signal for Sharp memory. Refer to ROM port chip select register.
BYTE	(O)	Turns to "1" when MEMCS16 has turned to "0" by the ROM memory access. ALE latched signal.
VIFCNT	(I)	1: Printer/re232C driver enable. 1 if the printer is connected.
-PRT_EN	(O)	0: Printer driver enable
-STBY	(O)	0: RS232C driver enable
-PDCLK	(O)	Printer data latch clock. Issued when -IOW with address 378, 278H.
-PDIN	(O)	Printer status input. Issued when IOR with address 379/279 or 37A/27A.
STROBE	(O)	Printer strobe signal (externally inverted). The contents of the printer control register bit 0.
AUTFDX	(O)	Printer auto linefeed signal (externally inverted). The contents of the printer control register bit 1.
INIT	(O)	Printer initialize signal (externally inverted). The contents of the printer control register bit 2.
SLCTIN	(O)	Printer select signal (externally inverted). The contents of the printer control register bit 3.
-ACK	(I)	Printer acknowledge signal. Used for the interrupt signal from the printer. Incorporates a pullup resistor (inside the chip).
FDSEL	(O)	FD access signal for LED activation (active when the motor on bit of DOR).

10. Pin description



NO	SIGNAL	BUF TYPE
1	VGACS	OBF2M
2	AD0	IOBF
3	AD1	IOBF
4	AD2	IOBF
5	AD3	IOBF
6	AD4	IOBF
7	AD5	IOBF
8	AD6	IOBF
9	AD7	IOBF
10	GND	
11	AD8	OBF
12	AD9	OBF
13	BCC	
14	AD10	OBF
15	AD11	OBF
16	AD12	OBF
17	AD13	OBF
18	AD14	OBF
19	AD15	OBF
20	EA16	OBF
21	EA17	OBF
22	EA18	OBF
23	EA19	OBF
24	EA20	OBF
25	GND	

NO	SIGNAL	BUF TYPE
26	-BYTE	OBF2M
27	-MEMWE	OBF
28	-MEMOE	OBF
29	-MEMCE0	OBF2M
30	-MEMCE1	OBF2M
31	-MEMCE2	OBF2M
32	-MEMCE3	OBF2M
33	-RMEM16	IBF
34	PDCLK	OBF
35	-PDIN	OBF2M
36	-ACK	IBFSU
37	SLCTIN	OBF2M
38	INIT	OBF2M
39	AUTFDX	OBF2M
40	GND	
41	VCC	
42	STROBE	OBF2M
43	-PRT_EN	OBF
44	-STBY	OBF
45	XD0	IOBF
46	XD1	IOBF
47	XD2	IOBF
48	XD3	IOBF
49	XD4	IOBF
50	XD5	IOBF

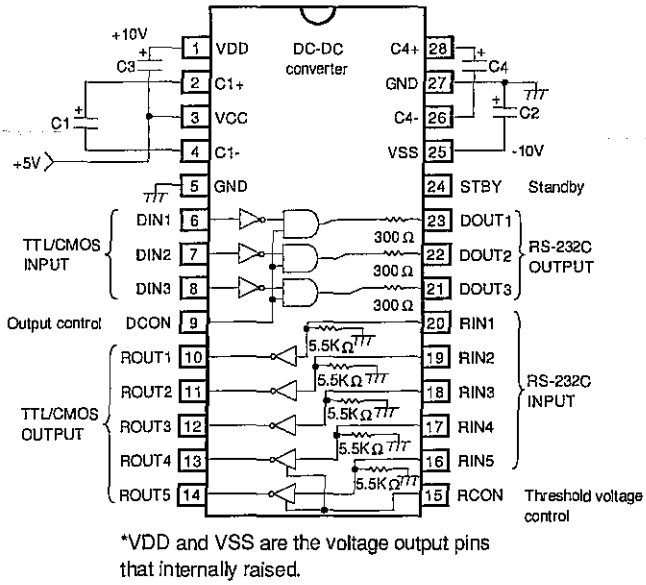
NO	SIGNAL	BUF TYPE
51	XD6	IOBF
52	XD7	IOBF
53	-CS8042	OBF2M
54	-INTKEY	OBF2M
55	-MEMR	IBF
56	-MEMW	IBF
57	-IOR	IBF
58	-IOW	IBF
59	RESET	IBFS
60	-SELTM	OBF2M
61	-MEMCS16	OBFN6M
62	IRQ7	TOBF
63	IRQ5	TOBF
64	AEN	IBF
65	GND	
66	ALE	IBF
67	-LMSEL	IBF
68	A19	IBF
69	A18	IBF
70	A17	IBF
71	A16	IBF
72	A15	IBF
73	A14	IBF
74	A13	IBF
75	A12	IBF

NO	SIGNAL	BUF TYPE
76	A11	IBF
77	A10	IBF
78	A9	IBF
79	A8	IBF
80	A7	IBF
81	A6	IBF
82	A5	IBF
83	A4	IBF
84	A3	IBF
85	A2	IBF
86	A1	IBF
87	XA0	IBF
88	IOCHRDY	OBF
89	VCC	
90	GND	
91	VIFCNT	IBF
92	-HDCS0	OBF
93	-HDCS1	OBF
94	-ENCRT	OBF2M
95	-FDSEL	OBF2M
96	-SELMD	IBF
97	-SELEX10	IBF
98	-READY	IBF
99	-MEN16	IBF
100	VGAAEN	OBF2M

IBF : TTL level input buffer
IBFS : TTL level schmidt trigger input buffer
IBFSU : TTL schmidt trigger input buffer with a pullup resistor
OBF : Output buffer IOL=4mA
OBF2M : Output buffer IOL=2mA
OBFN6M : Nch open drain output buffer IOL=6mA
IOBF : TTL level input/output buffer
TOBF : Tri-state output buffer

9-10. μPD4714GT (RS-232C DRIVER)

Block diagram/pin configuration (top view)



*VDD and VSS are the voltage output pins that internally raised.

Fig. 9-14

Standby line is internally pulled down.

Voltage withstand of C1~C4 must be above 16V.

Truth table

STBY	D_{CON}	D_{IN}	D_{OUT}	Note
H	X	X	Z	Standby mode
L	L	X	L	MARK level output
L	H	H	L	MARK level output
L	H	L	H	SPACE level output

STBY	R_{IN}	R_{OUT}
H	X	Z
L	H	L
L	L	H

H: High level L: Low level Z: High impedance X: H or L

9-11. Sharp original port map (SOP)

9-11-1. Access method

① Write the pointer address in the I/O address 7CH.

② Read or write the data in the I/O address 7DH.

9-11-2. Register groups

Pointer	Register name		
01	FD, etc. control	SI (R/W)	GA (W/O)
02	Device control	SI (W/O)	GA (R/W)
03	Modem control	SI (R/W)	
04	EMS control	SI (R/W)	
05	PSRAM control	SI (R/W)	
06	Power supply control	SI (R/W)	
07	Auto standby control	SI (R/W)	
08	Power supply status	SI (R/O)	
09	Power save timer	SI (R/W)	
0A	Auto resume timer	SI (R/W)	
0B	Resume enable	SI (R/W)	
0C	RSTCPU cause register	SI (R/O)	
0D	Expansion unit	SI (R/O)	
0E	VGA control	SI (R/W)	GA (W/O)
0F	NMI cause register	SI (R/O)	
10	Reserved		
11	Reserved		
12	ROM support control		GA (R/W)
13 ~ 1F	Reserved		

9-11-3. Explanation of registers

Pointer [01] FD, etc. control SI (R/W) GA (W/O)

BIT	7	6	5	4	3	2	1	0	
	*								Not used
		*							DISPLAY MODE (-ENCRT)
			*						KEY ASSIGN
				*					SIO SELECT
					*				SIO ASSIGN
						*	*	*	FDD ASSIGN

DISPLAY MODE 0: LCD MODE 1: CRT MODE

KEY ASSIGN 0: INTERNAL KEY ENABLE
1: INTERNAL KEY DISABLE

SIO SELECT 0: PORT 1 1: PORT 2

SIO ASSIGN 0: ENABLE 1: DISABLE

FDD ASSIGN

BIT	INT-FDD		EXT-FDD	
210	0	1	0	1
000	0	1	2	3
001	2	1	0	3
010	0	3	1	2
011	1	3	0	2
100	2	3	0	1
101	0	2	1	3
110	2	3	0	1
111	0	2	1	3

SIO SELECT affects the pointer 02 setting.

Pointer [02] Device control SI (W/O) GA (R/W)

BIT	7	6	5	4	3	2	1	0	
	*								HD EN
		*							HD SEL
			*						SIO EN
				*					SIO SEL
					*				PRT EN
						*			PRT SEL
							*		IMS EN (Inport Mouse)
7								*	IMS SEL

HD EN 0: INTERNAL HD ENABLE
1: INTERNAL HD DISABLE

HD SEL 0: PRIMARY
1: SECONDARY

SIO EN 0: INTERNAL SIO ENABLE
1: INTERNAL SIO DISABLE

SIO SEL 0: PRIMARY
1: SECONDARY

PRT EN 0: INTERNAL PRT ENABLE
1: INTERNAL PRT DISABLE

PRT SEL 0: PRIMARY
1: SECONARY

IMS EN 0: INTERNAL IMS ENABLE (Not used)
1: INTERNAL IMS DISABLE

IMS SEL 0: PRIMARY
1: SECONDARY (Not used)

IMS=INPORT MOUSE

Pointer [03] Modem control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					MODEM_EN
					*	*	*		Not used
								*	OUTSEL

MODEM EN 0: INTERNAL MODEM ENABLE
1: INTERNAL MODEM DISABLE

OUTSEL 0: MORST signal is issued
1: 202H decode signal output

Model port selection is set opposite to the internal SIO port setting.

Pointer [04] EMS control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*								Not used
		*	*						SW6, 5
				*	*				JP3, 2
						*	*	*	SW2, 1, 0 2x8~2xB (X_{16}=XXX0_2

SW6,5 Extended memory area setting

SW2,1,0 EMS control register I/O address setting

JP3,2 Pointer 05 JP1, 0 expansion

Pointer [05] PSRAM control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*							MAP1, 0
			*						PVTMEM
				*	*				JP1, 0
						*			PCS3EN
							*		INTVL
								*	Not used

MAP2,1 Private memory bank selection

PVTMEM 1: Private memory access enable (E0000H~EFFFFH)
0: Disable

PCS3EN Standard RAM capacity setting
1: 256KB used for a private memory area

INTLV 1: PSRAM interleave access enable
0: Disable

Pointer [06] Power supply control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					VMDM CNT
					*				VBL CNT
						*			VCC CNT
							*		VLCD CNT
								*	VIF CNT

VMDMCNT 0: Off 1: On Modem power supply

VBLCNT 0: Off 1: On Backlight power supply

VCCNT 0: Off 1: On System power supply

VLCDCNT 0: Off 1: On LCD power supply

VIFCNT 0: Off 1: On Printer/RS232C driver power supply

LCD and backlight power on needs to be in the LCD mode with the pointer 01 and display circuit enabled with the pointer 0E.

Pointer [07] Auto standby control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*				Not used
						*			VCC STB
							*		VLCD SAVE
								*	VIF SAVE

VCCSAVE 0: Auto resume disabled (with timer) 1: Enabled

VLCDSAVE 0: Auto power save disabled (with timer) 1: Enabled

VIFSAVE 0: Auto driver power save disabled 1: Enabled

Pointer [08] Power supply status SI (R/O)

BIT	7	6	5	4	3	2	1	0	
	*	*	*						Not used
				*					VMDM STS
					*				VBL STS
						*			VCC STS
							*		VLCD STS
								*	VIF STS

VMDMSTS 0: Off state 1: On state

VBLSTS 0: Off state 1: On state

VCCSTS 0: Off state 1: On state

VLCDSTS 0: Off state 1: On state

VIFSTS 0: Off state 1: On state

(Even though set to on by the power supply control, off is established by the auto standby.

Pointer [09] Power save timer SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*	*	*	*	PST3~0 0=0 min.~1 min. F=15 min.~16 min.

PST3~0 VLCD, VBL off timer count time is set between 0 and 15 minutes. The set value is read when read.

Pointer [0A] Auto resume timer SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*								Not used
		*	*	*	*	*	*	*	ART6~0

ART6~0 VCC off time-out time is set between 0 and 127 minutes. The set value is read when read.

Pointer [0B] Resume enable SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*				Not used
						*			MRI
							*		CI
								*	RE

MRI 1: Enabled to return from resume by the RI signal from the modem.

CI 1: Enabled to return from resume by the CI signal from the 232C.

RE 1: Resume enabled

Pointer [0C] RSTCPU cause register SI (R/O)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*				MRI
						*			CI
							*		R
								*	Not used

MRI 1: Resume return BY MRI

CI 1: Resume return by CI

R 1: Resume return by the resume switch

Pointer [0D] Expansion unit SI (R/O)

BIT	7	6	5	4	3	2	1	0	
*	*	*	*	*	*	*			Not used
								*	EXU

EXU 0: Expansion unit exists
1: Expansion unit does not exist

Pointer [0E] VGA control SI (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*				PWRDWN2
						*			PWRDWN1
							*		VGA EN
								*	SIO_POL

PWRDWN2,1 0 0 Normal operation
0 1 Relax mode
Though power turns down, R/W is enabled for VRAM and REG.
1 0 Retire mode
Power turns down and R/W is not enabled for VRAM and REG. Needs refresh timer to set.

VGA EN 0: VGA enable
1: Disable

SIO_POL 0: Normal 1: 232C input/output polarity inverted

Pointer [0F] NMI cause register SI (R/O)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*	*	*	*		Not used
								*	RSNNMI

RSMNMI 0: Resume request NMI does not occur
1: Resume request NMI occurred.

Pointer 0B Cleared by setting the bit 0 of RE sets to 0.

Pointer [12] ROM port control GA (R/W)

BIT	7	6	5	4	3	2	1	0	
	*	*	*	*					Not used
					*	*	*	*	IOA3~0

IOA3~0 Specifies the part of "X" of the I/O address 1X8~BH that set by the dip switch for the UE-1R06/06 (AX dictionary ROM board).

Chapter 10. CRT I/F unit (CE-621A)

10-1. Am81EC176 VGA Enhanced CMOS Color Palette

10-1-1. DISTINCTIVE CHARACTERISTICS

- **VGA hardware and software compatible with Low-Power "Sleep" Mode**
- **Full static operation during SLEEP mode – no pixel clock needed**
- **Compatible with the Am81C176 and in most IMSG171/176/176L**
- **Clock rates up to 80 MHz**
- **Available in 32-pin PLCC package**
- **256 x 18 Color Lock-Up Table (LUT)**
- **Triple 6-bit DACs**
- **RS-170A compatible RGB outputs**
- **External current reference**
- **Asynchronous CPU interface**
- **Single monolithic, high-performance CMOS**
- **Single +5V power supply**

10-1-2. GENERAL DESCRIPTION

The Am81EC176 has been designed specifically for Laptop Personal Computer manufacturers offering VGA compatibility and the option of driving an external RGB monitor. This part is hardware and software compatible with the Am81C176. The Am81EC176 operates at speeds up to 80 MHz and can support monitors with resolutions up to 1024 x 768.

The low-power option is enabled by pulling the SLEEP pin high. Enabling the SLEEP feature reduced power consumption of the Am81C176 by about 98.

In the SLEEP mode, the LUT RAM and states of all internal registers are maintained and can be read from and written to as in the normal mode.

An internal pull-down resistor has been provided at the SLEEP pin to maintain full compatibility with the Am81C176. The Am81EC176 defaults to normal operation when the SLEEP pin is left open (N/C).

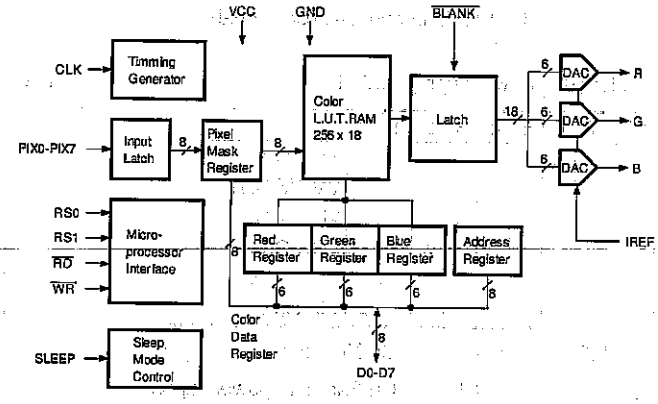
The Am81EC176 has a 256 x 18 Look-Up Table and triple 6-bit DACs. It can simultaneously display 256 colors out of an available set of 256K colors.

A proprietary technique allows read and write operations to the Color look-up table during active video without the "snow effect" (white noise) appearing on the display.

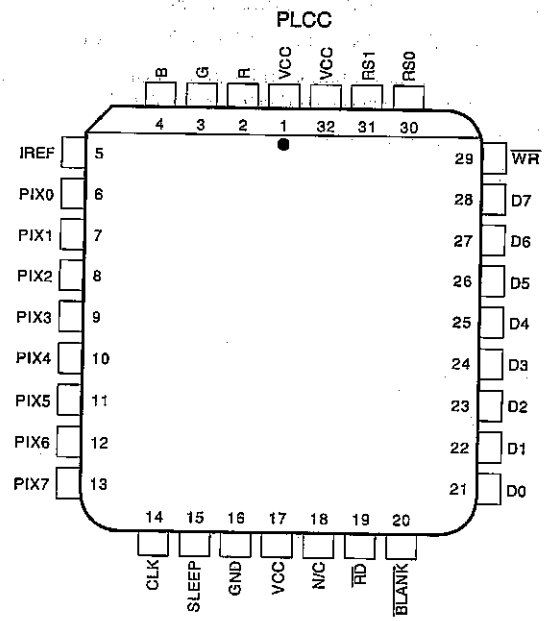
The Am81EC176 generates RS-170A compatible outputs into doubly-terminated 75Ω loads, without external buffers.

The Am81EC176 is fabricated using AMD's state-of-the-art 1.2μ CMOS process. The device is available in a 32-lead PLCC package.

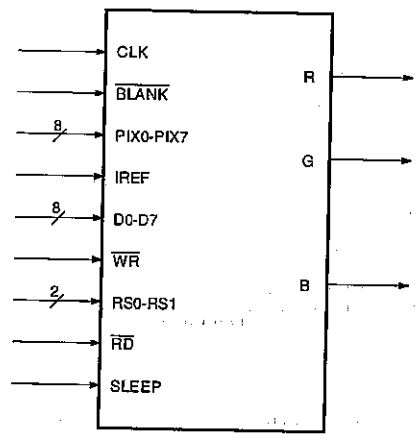
10-1-3. BLOCK DIAGRAM



10-1-4. CONNECTION DIAGRAMS



10-1-5. LOGIC SYMBOL



10-2. PIN DESCRIPTION

10-2-1. Timing Section

CLK

Clock Source Pin (TTL Compatible Input)

This input is the pixel clock of the video system and is to be driven by a dedicated TTL buffer. The rising edge of CLK latches the $\overline{BLANK}$ and $PIX_0 - PIX_7$ inputs and also controls the flow of these signals through the pipeline stages of the Color Palette and DACs to the R, G, and B outputs.

$\overline{BLANK}$

Blank (TTL Compatible Input)

The $\overline{BLANK}$ input, when active, overrides the color pixel data to force the R, G, and B outputs to their blank levels. This blank level is required during the monitor's vertical and horizontal retrace times. It is latched on the rising edge of CLK. typically, blank time is used to update the Look-Up Table through $D_0 - D_7$.

Bit Map Interface Section

$PIX_0 - PIX_7$

Color Pixel Data Addresses (TTL Compatible Inputs)

These 8 inputs select which of the 256 entries in the Color Look-Up Table is to be used to provide pixel color information. These inputs run at the pixel rate of the system and are latched on the rising edge of CLK. PIX_0 is the least significant bit.

10-2-2. CPU Interface Section

$D_0 - D_7$

Data and Address Bus (TTL Compatible Bi-Directional)

These 8 pins are used by the host microprocessor to write to (with $\overline{WR}$ low) and read from (with $\overline{RD}$ low) the internal registers (Pixel Mask Register, Pixel Address Register, and Color Data Register). D_0 is the least significant bit.

During write cycles, the rising edge of $\overline{WR}$ latches data from the $D_0 - D_7$ inputs into the register selected by the $RS_0 - RS_1$ inputs. During read cycles, $\overline{RD}$ drives the $D_0 - D_7$ lines from the register selected by $RS_0 - RS_1$. The end of a read cycle is determined by the rising edge of $\overline{RD}$.

When both $\overline{WR}$ and $\overline{RD}$ are a logical one, the $D_0 \sim D_7$ pins go into three-state.

$\overline{WR}$

Write Control Input (TTL Compatible Input)

$\overline{WR}$ is the control signal used for writing data into internal registers. $\overline{WR}$ must be a logical zero to write data to the internal registers. During Write operations, $RS_0 - RS_1$ are latched on the falling edge of $\overline{WR}$ and $D_0 - D_7$ are latched on the rising edge of $\overline{WR}$. When active, information on the external data bus is available to the $D_0 - D_7$ inputs.

$\overline{RD}$

Read Control input (TTL Compatible Input)

$\overline{RD}$ must be a logical zero to read data from the internal registers. During Read operations, $RS_0 \sim RS_1$ are latched on the falling edge of $\overline{RD}$. When active, information on the internal data bus is available to the $D_0 \sim D_7$ pins.

$RS_0 - RS_1$

Register Select inputs (TTL Compatible Inputs)

$RS_0 - RS_1$ allow the CPU to select any of the internal registers. These inputs determine the type of read or write operation being performed. See Table 1.

SLEEP

Sleep Mode Input (TTL Compatible Input)

SLEEP is the control signal used to initiate the power down "Sleep" mode. SLEEP must be a logical one to initiate the Sleep mode, an internal pull-down resistor has been provided at the SLEEP pin to maintain full compatibility with the Am81C176. The Am81EC176 defaults to normal operation when the SLEEP pin is left open (N/C). The SLEEP pin will typically draw 20µA when a logical one is applied.

10-2-3. Analog Output Section

R

Red Video Output (Analog Output)

Analog output of the red DAC. This output is capable of driving an RS-170A compatible doubly-terminated 75Ω cable.

G

Green Video Output (Analog Output)

Analog output of the green DAC. This output is capable of driving an RS-170A compatible doubly-terminated 75Ω cable.

B

Blue Video Output (Analog Output)

Analog output of the blue DAC. This output is capable of driving an RS-170A compatible doubly-terminated 75Ω cable.

I_{REF}

Current Reference (Analog Input)

I_{REF} is the reference current input. through this pin the user provides the reference current for the DAC which, in turn, control the full-scale output currents.

$$I_{REF} = \frac{1V_{WHITE}}{2.1\ R_{LOAD}\ (=37.5\Omega)}$$

10-2-4. Power Supply Section

V_{CC}

+5 Volt analog Power Supply

GND

Ground

10-3. FUNCTIONAL DESCRIPTION

The Am81EC176 CMOS color palette integrates all major functions required in the video section of a graphics system and supports pixel rates sufficient to drive monitors with resolutions up to 1024 x 768.

A programmable 256 x 18 Color Look-Up Table (LUT) maps pixel data from a bit-map memory into physical color, and three 6-bit Digital-to-Analog-Converters (DACs) convert the outputs of the LUT into RS170A compatible RGB analog format. Up to 8-bits per pixel are supported for a maximum of 256 simultaneous colors out of 256K color combinations available.

10-3-1. CPU Interface

The Am81EC176 is designed to support a standard CPU bus interface with direct access to 256 Color Look-Up Table RAM locations and two control registers. The CPU interface is completely asynchronous with respect to pixel clock. However, data transfers between the LUT RAM and Red Register, Green Register, and Blue Register (see block diagram) are internally synchronized to pixel clock. Double sampling techniques have been utilized in order to minimize metastability problems occurring when synchronizing an asynchronous event (such as $\overline{RD}$ or $\overline{WR}$) with a free running clock (such as CLK).

The Read and Write access to the LUT take one and two pixel clock cycles, respectively.

The nature of the CPU access is determined by the Register Select (RS_1, RS_0) inputs. RS_1 and RS_0 select among Address Register (LUT write), Address Register (LUT read), Color Data Register and Pixel Mask Register, as shown in Table 10-1.

Table 10-1. RS_0, RS_1 Decoding

RS_1	RS_0	Access Type
0	0	Address Reg. (LUT write)
0	1	Color Data Register
1	0	Pixel Mask Register
1	1	Address Reg. (LUT read)

A typical *color data write cycle* is initiated by setting the 8-bit Address Register (LUT write) with the address of the LUT RAM into which data is to be written. Next the CPU performs three write cycles to the Color Data Register: one for red, one for green, one for blue intensity. At the end of the blue cycle the data is concatenated into an 18-bit word and written to the LUT RAM location pointed to by the Address Register. the Address Register is then auto-incremented to point to the next location in LUT RAM. This process may be repeated again as required. If the user needs to access consecutive LUT locations the Address Register needs to be written to only at the beginning of the sequence. See Table 10-2.

A typical *color data read cycle* is initiated by setting the 8-bit Address Register (LUT read) with the address of the LUT RAM to be read. At this point, 18 bits of color data are transferred from the LUT RAM to the Red, Green and Blue portions of the Color Data Register, and the Address Register is again auto-incremented. This process may be repeated as required. If the user needs to access consecutive LUT locations the Address Register needs to be written to only at the beginning of the sequence. See table 2.

The 6-bit color data occupy the six least significant positions in the data bus. Bits D_6 and D_7 are ignored during write cycles and are set to 0 during read cycles. Bit D_0 is the least significant bit.

Table 10-2. Read/Write Access to the Am81EC176

$\overline{RD}$	$\overline{WR}$	RS_1	RS_0	ARb	ARa	Function
1	0	0	0	X	X	Write Address Register (LUT Write); AR(7:0) ← D(7:0); ARb, ARa ← 0
1	0	0	1	0	0	Write Color Data Reg. (red); RREG(5:0) ← D(5:0); ARb, ARa ← 0.
1	0	0	1	0	1	Write color Data Reg. (green); GREG(5:0) ← D(5:0); ARb, ARa ← 0.
1	0	0	1	1	0	Write Color Data Reg. (blue); BREG(7:0) ← D(5:0); Arb, ARa ← 0; Write Color Look-Up-Table; R(5:0) ← RREG; G(5:0) ← GREG; B(5:0) ← BREG; INC. AR(5:0).
1	0	1	1	X	X	Write Address Register (LUT Read); AR(7:0) ← D(7:0); ARb, ARa ← 0. Read Color Look-Up Table; RREG(5:0) ← R(5:0); G(5:0) ← GREG; B(5:0) ← BREG; INC. AR(7:0).
0	1	0	1	0	0	Read Color Data Reg (red); D(5:0) ← RREG(5:0); ARb, ARa; D(7:6) ← 0.
0	1	0	1	0	1	Read Color Data Reg (green); D(5:0) ← GREG(5:0); ARb, ARa; D(7:6) ← 0.
0	1	0	1	1	0	Read Color Data Reg (blue); D(5:0) ← BREG(5:0); ARb, ARa; D(7:6) ← 0; GREG; B(5:0) ← G(5:0); INC. AR(7:0).
0	1	0	0	X	X	Read Address Register; D(7:0) ← AR(7:0); ARb, ARa ← 0.
1	0	1	0	X	X	Write Pixel Mask Register; PMREG(7:0) ← D(7:0); ARb, ARa ← 0.
0	1	1	0	X	X	Read Pixel Mask Register; D(7:0) ← PMREG(7:0); ARb, ARa ← 0.

The Am81EC176 uses one 8-bit *Address Register* to address the LUT RAM. The Address Register resets to 0 after a blue read/write cycle to the LUT RAM address 255. A user transparent modulo-3 counter (ARb, ARa) keeps track of the red, green and blue cycles and auto-increments at the end of each read/write access to the LUT RAM. This counter is reset to zero after a write access to the Address Register, and is unchanged following a read access to the Address Register. Thus a write to the Address Register will abort any unfinished read or write sequence.

The Am81EC176 uses one 8-bit *Pixel Mask Register* to modify the address of the LUT RAM as provided by PIX_0 – PIX_7. The eight bits of this register are ANDed with PIX_0 – PIX_7, and the result used as the address to the LUT RAM. This mechanism provides a quick way to after the appearance of one or more colors on the display unit with just one CPU access, without the need for changing the bit-map memory or the LUT contents. The CPU addresses are not affected by this register.

10-3-2. Display Memory Interface

Pixel data PIX_0 – PIX_7 are latched on the rising edge of CLK and are used as address to the 256 locations of the LUT RAM. The total pipeline delay from PIX_0 – PIX_7 and $\overline{BLANK}$ inputs, to R, G, B outputs is four clock cycles.

10-3-3. Video Generation

During each clock cycles, a 18-bit word from the LUT RAM is presented to three DACs: 6 bits for red, 6 for green and 6 for blue. The three DACs convert the digital color memory output input RGB RS-170A analog format.

The $\overline{BLANK}$ input is latched on the rising edge of CLK. It is routed to the three DACs after a delay of four clock periods, identical to the delay incurred by the video stream.

$\overline{BLANK}$, when active, forces a zero to the input to the DACs, overriding the current LUT output.

The three analog outputs of the Am81EC176 are each capable of driving a doubly terminated 75Ω coaxial cable.

10-3-4. SLEEP Mode Operation

The SLEEP mode operation is initiated by providing a logical one to the SLEEP mode input pin. In the SLEEP mode, the DACs and internal pixel clock are automatically disabled and the LUT RAM is placed in a low-power static state. The LUT RAM and internal registers may be read from and written to as in normal operation. Since the internal pixel clock is disabled, the state of the external pixel clock has no effect on operation and may be held low, high, or left in a metastable state. It is suggested that the external pixel clock be held low or high to reduce system power consumption. If the external pixel clock is left in a metastable state, the input buffer will draw unnecessary current.

The Am81EC176 has been designed with SLEEP control circuitry to reduce current surging when the part is switched between SLEEP and normal modes. The latency period for SLEEP to normal and normal to SLEEP is approximately 20 µs and 5 µs respectively.

The return to the normal operation mode, a logical zero should be applied to the SLEEP mode input pin. the Am81EC176 may be powered up in either the SLEEP or normal modes.

Chapter 11. Add-on battery (CE-621EV)

11-1. PRODUCT OUTLINE

Name	PC6220 optional battery pack
Description:	The battery pack available as an option to the PC6220.
	Because the Note computer uses an 80C286 CPU has a large power consumption, the computer goes out of the power after a short time. If this battery option is added beside the internal battery, the PC6220 operating time may be expanded from normal 1.7 hours to 5 hours. For the battery pack is directly housed in the back of the PC6220, so it can be carried along with the computer. The following introduces the general specifications. ❑ Battery: 9.6V, 2.2Ah (Ni-Cd type 1.2V, 2200mAh x 8pcs) ❑ Operating time: 3 hours nominal for this pack only. ❑ Recharge: Recharged via the AC adaptor as connected to the computer, or directly recharged via the AC adaptor as connected directly to the CE-621EV. Recharge time: About 3.5 hours.

11-2. EXTERNAL BATTERY (Add-on battery pack)

Option

1) Model : CE-621EV Attaches to rear of PC6220.
2) Type : Ni-Cd battery 1.2V x 8pcs.
3) Capacity : 21.1Wh (9.6V 2200mAh)
4) Battery life : 3 hours (only with CE-621EV)
   4.7 hours (internal battery + CE-621EV)
5) size : 279(W) x 59(D) x 34.5(H)mm 800g
   (11.0" x 2.3" x 1.4") (1.9 lbs)

11-3. BATTERY INDICATOR

On the External (Add-on) Battery Pack

1) Green LED is lit: : 70% or over (fully charged)
   Green LED is off: : 0 ~ 70%
   The status of the battery can be checked without connecting to the computer by pressing the push button on the external battery pack.

   ☆ Care should be exercised that the green LED will be lit by pressing the push switch if the battery pack is charging with AC adaptor or if the battery pack is connected to the computer and operating the computer or charging the battery pack with AC adaptor.

11-4. ADD-ON BATTERY PACK

The CE-621EV add-on battery pack attaches to the rear of the PC-6220. With this pack attached, it is possible to extend battery operation time to up to 4.7 hours.

In order to save some weight, and still have a longer battery life, it is possible to use the add-on battery pack without the internal battery installed. In this case, 3 hours of battery operation can be achieved.

11-4-1. Installing the Battery Pack

- Turn off the power and place the computer and battery pack as shown in Fig. 11-1.

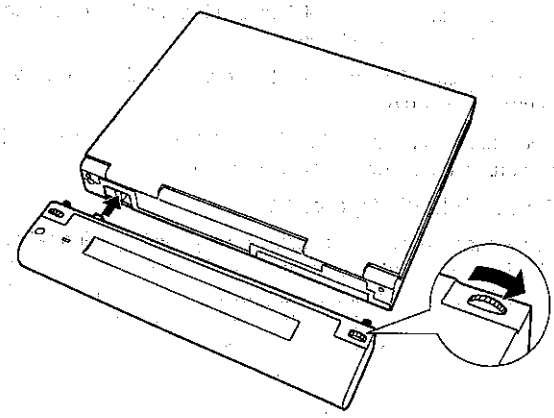


Fig. 11-1

- Bring the battery pack up to the rear of the computer, and slowly push the two units together. Make sure that the two alignment pins that project from the battery pack are located in their holes on the rear of the PC6220.
- Push together firmly until the connector mates, then use a finger to turn the two lock screws clockwise until tight.
  NOTE: If the screws are not tightened securely, they might be loosened during operation.

11-4-2. Charging the Battery Pack

The add-on battery pack can be charged either when attached to the computer, or as a separate unit.

11-4-3. Charging as a Separate Unit

To charge as a separate unit, plug the AC adaptor into the jack on the side of the pack as shown in Fig. 11-2.

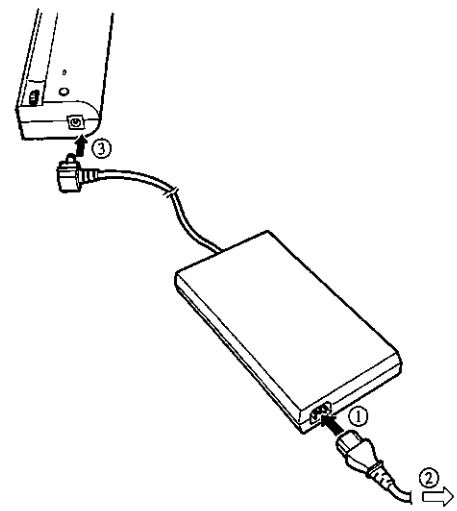


Fig. 11-2

It takes about 3.5 hours to fully charge the pack. First the LED next to the button goes on and off. It goes on lighting if the pack is approx. 70 percent charged. It takes about another 45 minutes at this state to fully charge the pack.

11-4-4. Charging While Connected to the PC6220

To charge while connected to the computer, plug in the AC adaptor in to the PC6220's power socket. The battery pack is charged in parallel with the computer's internal battery. It takes about 3.5 hours to fully charge the PC6220 with the battery pack attached.

When connected to the main computer, the add-on battery pack is connected in parallel with the internal battery. In this configuration, the computer will automatically draw power from whichever of the two batteries has more charge at a particular time, equalizing the power demands between both batteries.

11-4-5. State of Charge

1) Charge indication

When charging the computer with the add-on battery pack attached, the state of charge of the battery pack is shown by the pack's own LED. The state of charge of the add-on pack can also be checked when the AC adaptor is not connected, provided that a few hours have passed since disconnecting the adaptor. Press and hold down the button next to the pack's LED for at least 3 seconds. The LED shows green if the pack is at least 70 percent charged. If you press the button with the AC adaptor still connected or within a few hours of disconnecting it, the LED may show green independent of the actual state of charge.

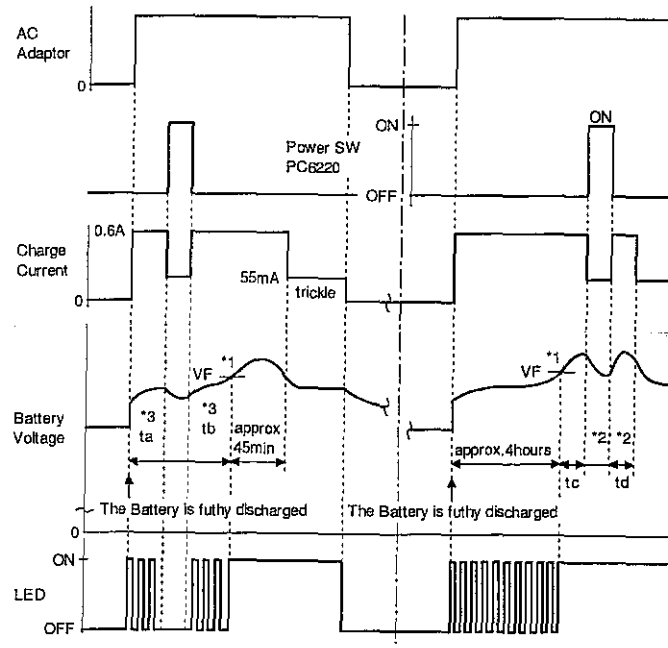
2) Low battery indication

The computer's battery indicator displays the low battery indication for the internal battery and the add-on pack in parallel. When the indicator shows red, the combined power of both batteries is low. When the indicator blinks red, the computer is about to shut down.

11-5. ADD-ON BATTERY PACK (CE-621EV)

11-5-1 CHARGE

Charge Time	About 3.5 hours	POWER SW:OFF When connected the PC6220
Charge Current	Typ. 0.6A	POWER SW:OFF When connected the PC6220
	Typ. 55mA	POWER SW turned ON or after fully recharging



*1;

Ta	V_F
40°C	approx. 11.2V
25°C	11.7 ± 0.1V
5°C	approx. 12.4V

V_F is compensated by the thermistor inside the battery.

Fig. 11-3

*2; ta+tb ≒ 4 hour
*3; tc+td ≒ 45 minutes

In case of connecting to the PC6220, the battery is recharged rapidly and the LED goes on and off when POWER SW is turned off, and it is recharged slowly (trickle mode) and the LED goes out when the POWER SW is turned on.

If the voltage of the battery already comes up to 11.7V (at 25°C), the LED has going on when the POWER SW is turned on.

In case of recharging as a separate unit, it is always recharged rapidly and the LED goes on and off.

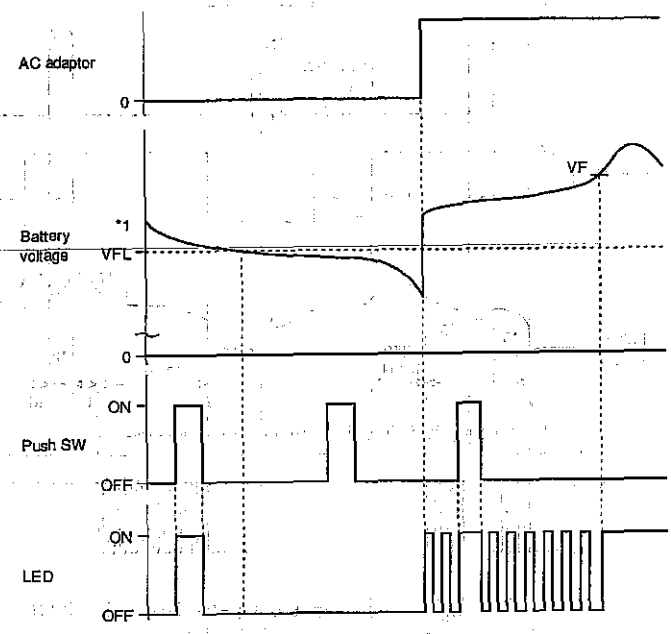
During recharging rapidly, the LED on the Battery Pack goes on and the 45-minutes timer starts when the voltage of the battery comes up to 11.7V (at 25°C).

When the LED goes on, the battery is approx. 70 percent charged.

And after about 45-minutes, the recharging is finished and the charge mode is charged to the trickle mode.

If the POWER SW is turned on while the 45-minutes timer is working, the operation of the timer is ceased, not reset.

11-5-2. CHECK THE BATTERY BY THE PUSH SW



*1; V_{FL} = 10.2 ± 0.1V

If the voltage of the battery is more than about 10.2V, the LED shows green when the button next to the LED is pressed and held down. In this case, the battery is more than about 70 percent charged.

If pressing the button with an AC Adaptor connected or within a few hours of disconnecting it, the LED may be green. Because the voltage of the battery comes more than 10.2V.

11-6. Ni-Cd Battery

Electrical characteristics

	Item	Test method	Standard
1	Open voltage	Use a DC voltmeter (class 0.5 or higher, internal resistance 1000 Ohm/V or more) to measure the voltage between pins.	Min. 10V (within 14 days from charging)
2	Capacity	After charging for 5 hours with 660mA current and leaving for 1 hour, make continuous discharging with a constant current of 440mA to the end voltage (8V) of discharging.	Discharging time: min. 5 hours
3	High-efficiency discharging performance	After charging for 5 hours with 660mA current and leaving for 1 hour, make continuous discharging with a constant current of 220mA to the end voltage (8V) of discharging.	Discharging time: min. 50 minutes
4	Overcharging performance	Charge a discharged battery for 48 hours with a constant current of 660mA under ambient temperature of 10 ± 2°C. Leave it for 16 to 24 hours under 20 ± 5°C. Then perform discharging according to item 2.	Must be free from remarkable deformation and leakage. The standard in item 2 must be met.
5	Capacity storage performance	After charging for 5 hours with 660mA current and leaving for 28 days, make continuous discharging with a constant current of 440mA to the end voltage (8V) of discharging.	Discharging time: min. 3 hours
6	Lifetime	Discharge a charged battery for 2 hours and 20 minutes with 550mA current. Discharge it for 3 hours and 10 minutes with 550mA current. Repeat these charging and discharging. To check the capacity during the test, repeat 50 cycles of charging and discharging, discharge the battery (which finished the former discharging) with a 440mA current to 8V, then charge and discharge according to item 2.	Until the capacity falls to 60 % of the rated capacity, Min. 500 times.
7	Safety valve operation (Destructive test)	Discharge continuously with a 440mA current to the end voltage (8V) of discharging. Then charge it with a constant current of 2200mA.	The safety valve must operate in 5 hours.

CHAPTER 12. 3.5" FDD unit (CE-621F)

12-1. General

This is an external 3.5" floppy disk drive option that connected to the expansion bus connector behind the PC-6220. This floppy disk drive can read/write a 1.44MB and 720KB disks. When the CE-621E expansion box option is connected to the PC-6220, the floppy disk drive can be installed to the CE-621E. For this unit also has the 5.25" FDD (CE-452F)/external keyboard (PS/2 keyboard) interfaces, those devices can connect to CE-621E.

12-2. System configuration

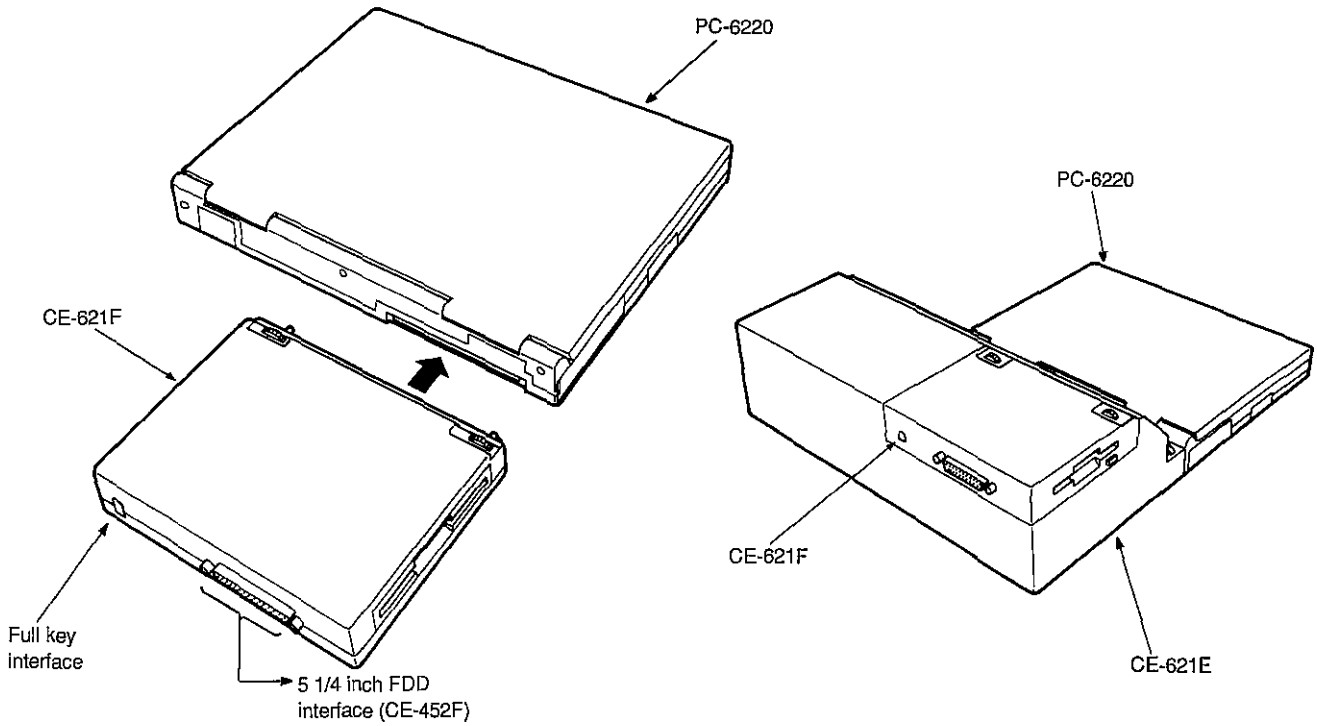


Fig.12-1

12-3. General specifications

FDD	(Internal) 3.5" : 1 FDD • Storage capacity 1.44MB/720KB • Transfer speed 500K-bit/250K-bit (External) 5.25" : FDD connectable • Interface 25-pin D-SUB • CE-452F connectable
External keyboard	• PS/2 full keyboard supported • 6-pin mini-DIN connector
Connection with PC-6220	Directly connected to the system bus with a 120-pin connector
Power supply	+5V (from the PC-6220)
Physical dimensions	166mm(W) x 143mm(D)x34.5mm(H) (6.5" x 5.6" x 1.4")
Weight	630 g (1.4 lbs)

12-4. Block diagram

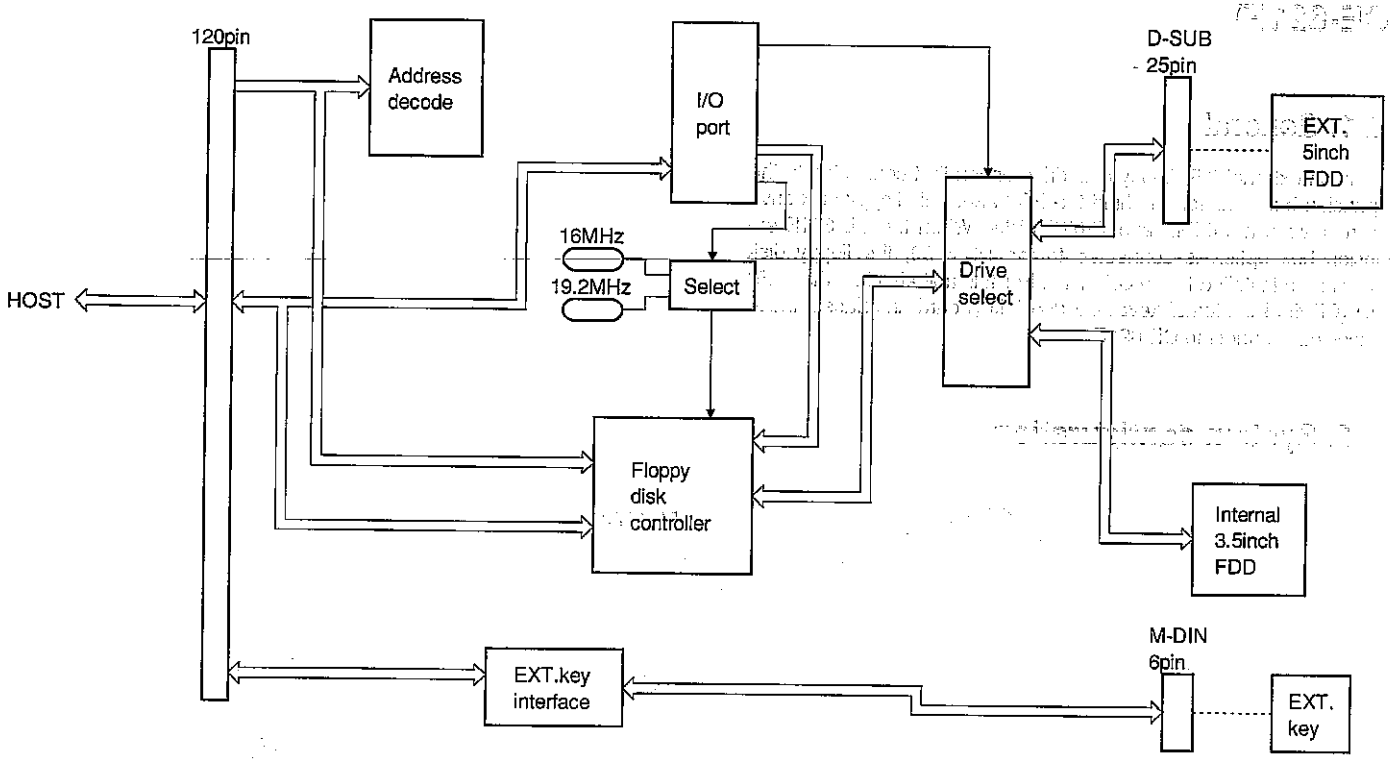


Fig.12-2 3.5 inch Portable FDD

12-5. Circuit description

It incorporates the 3.5" floppy disk drive and its interface to make expansion of the PC-6220. In the CE-621F is contained the IBM PS/2 full keyboard, 5.25" floppy disk drive interface, and external keyboard interface.
Assignment of the 3.5" and 5.25" FDD can be selected via the Sharp original port (SOP). To make it connected, write the pointer address 01H) in 7CH, then write data in SOP 7DH. 7CH will be cleared to 00H.

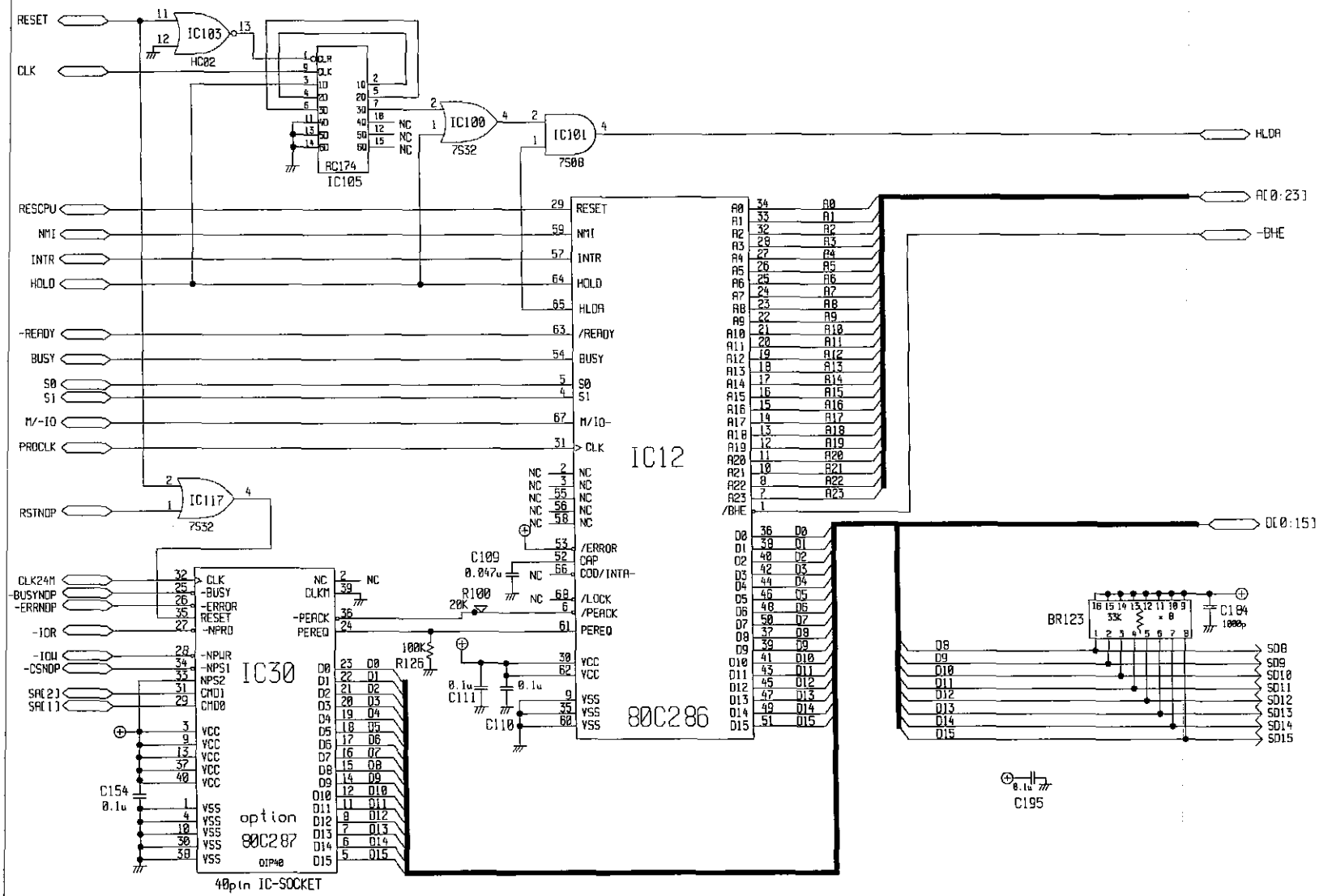
(1) I/O address

Address	Read/Write	Function	I/O allocation
7CH	Write	Pointer address setting	01H
7DH	Write	Key allocation setting	Bit5
7DH	Write	FDD allocation setting	Bit2,1,0

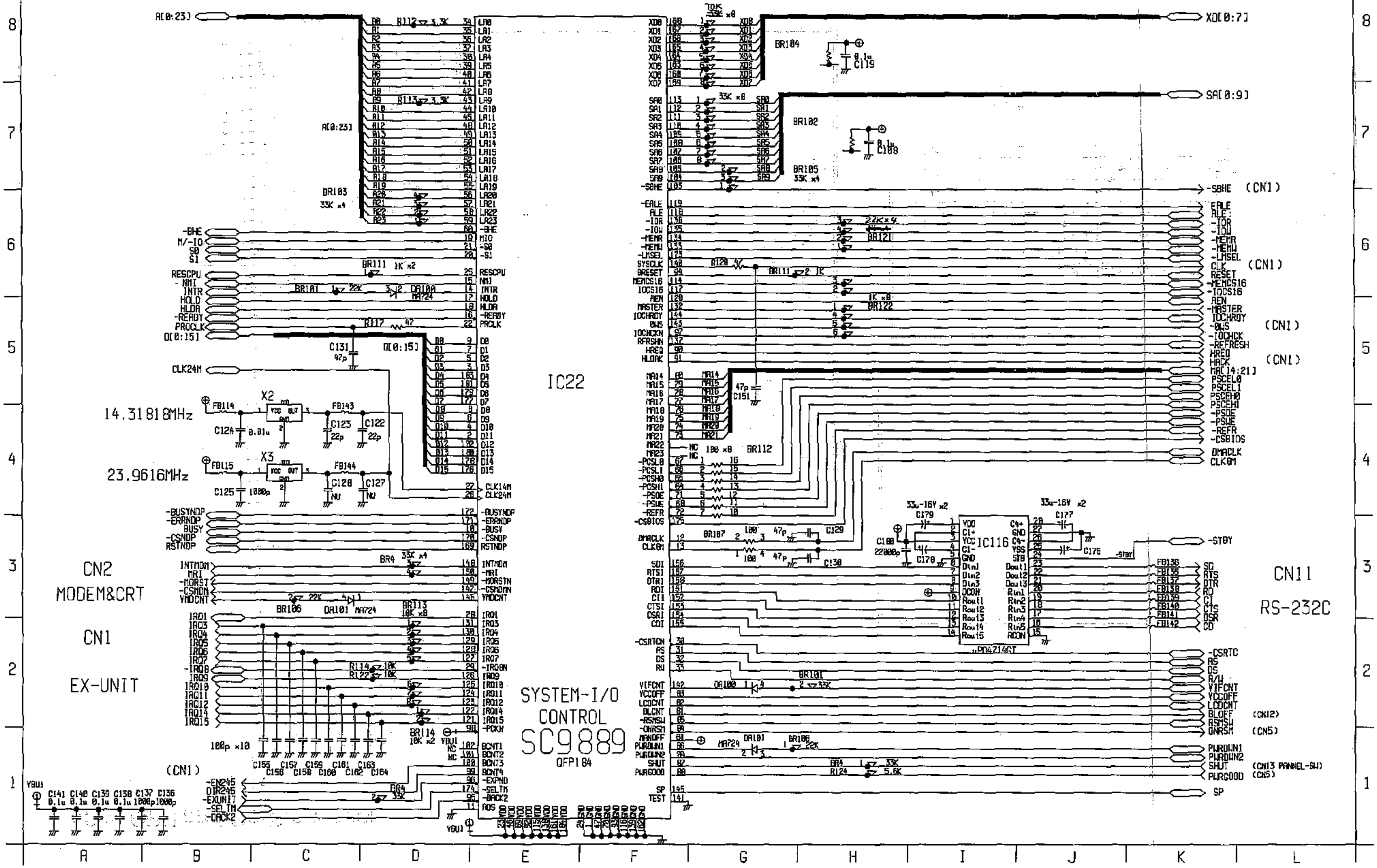
bit5	Key selection
0	Internal key
1	External key

bit2	bit1	bit0	Internal drive	External drive
0	0	0	Drive0	Drive1
0	0	1	Drive1	Drive0

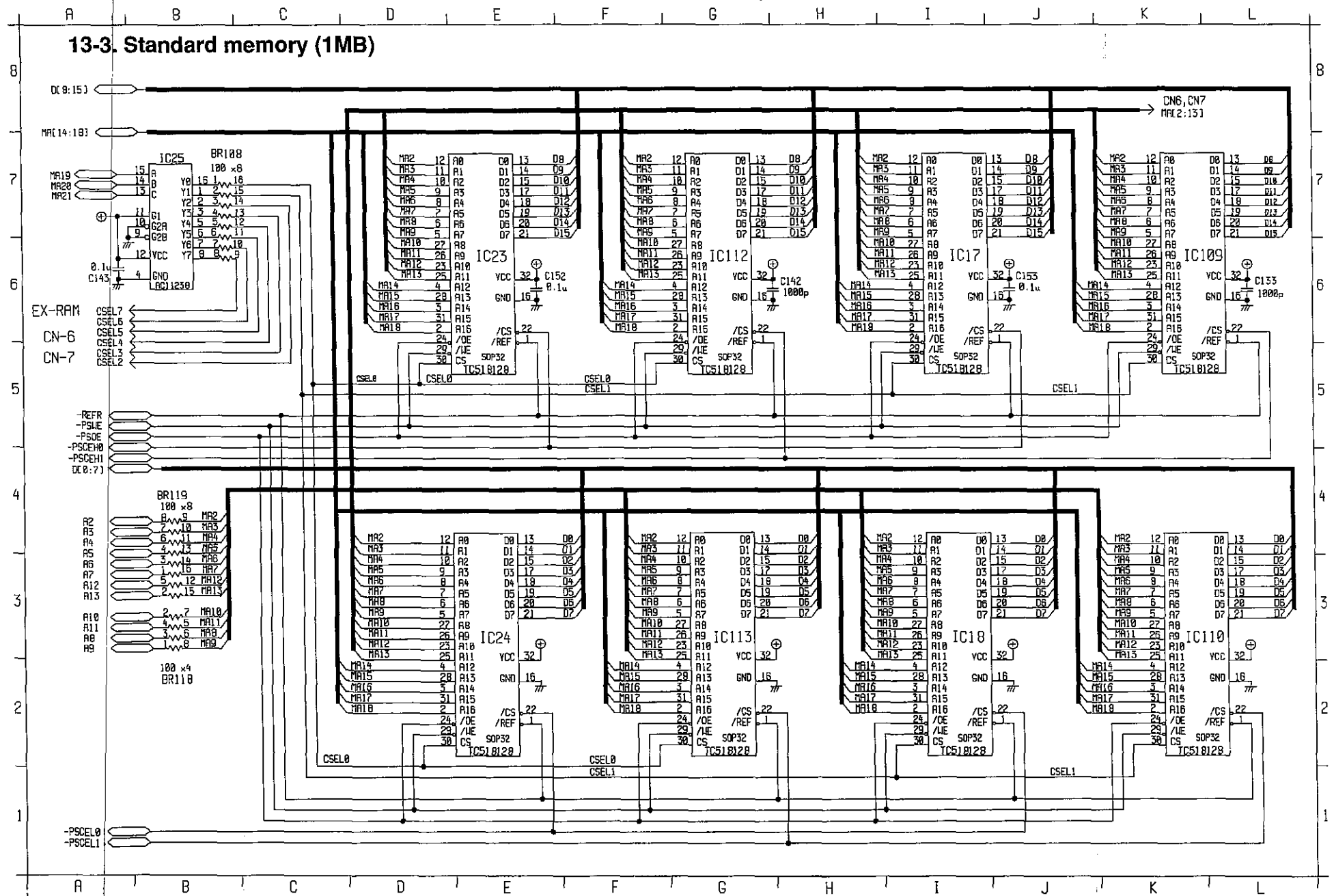
13-1. CPU and Co-Processor



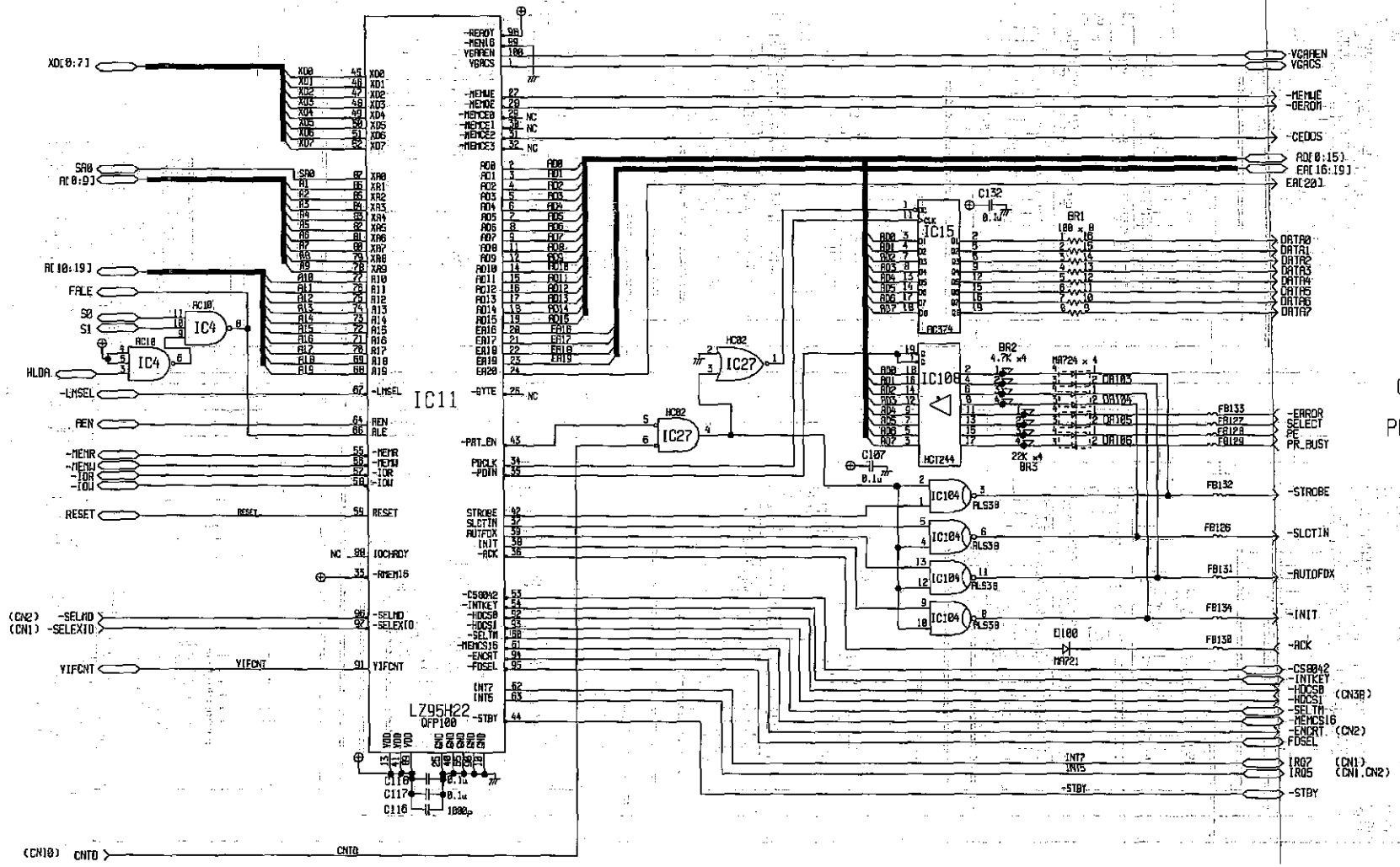
13-2. System-I/O control RS-232C



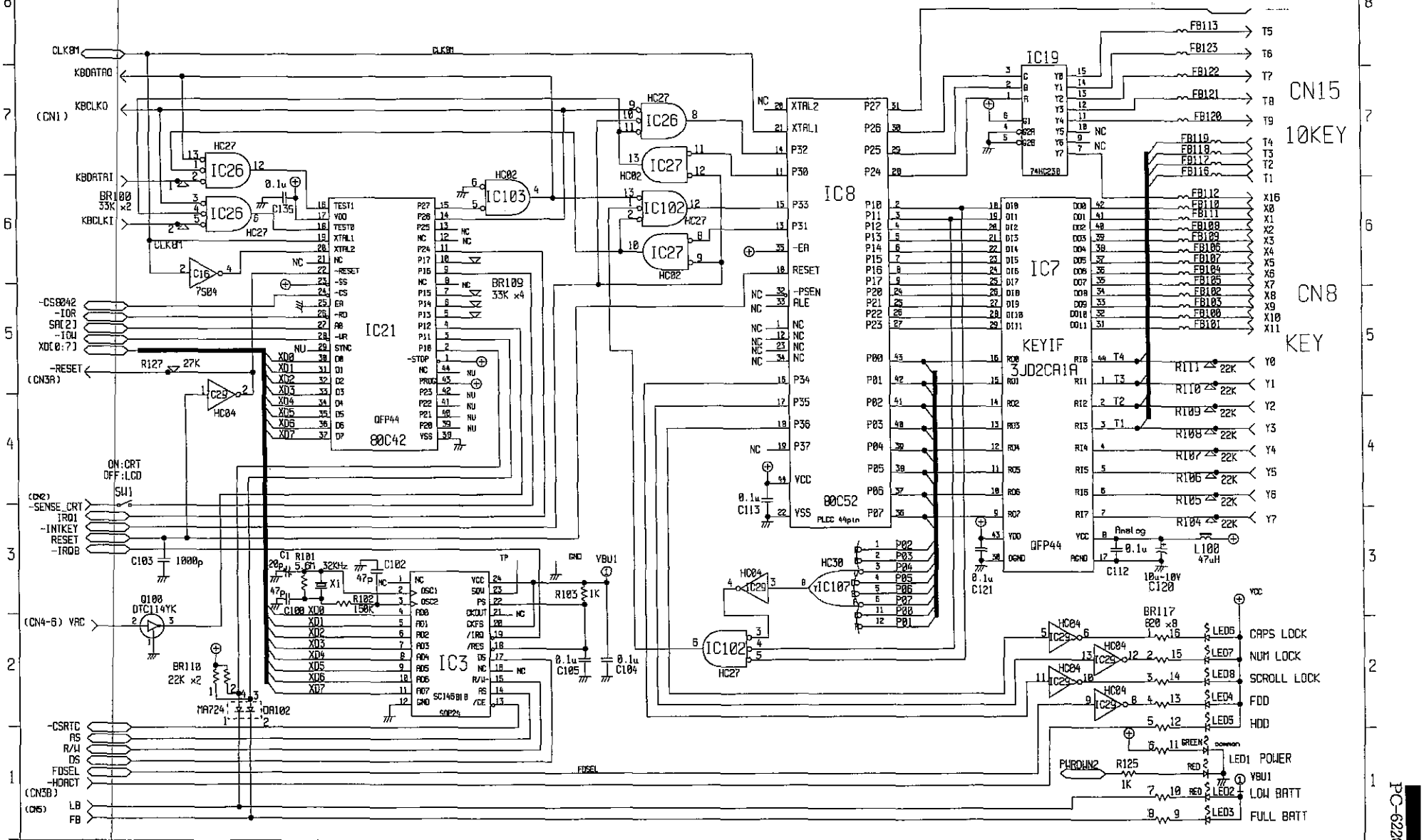
13-3. Standard memory (1MB)



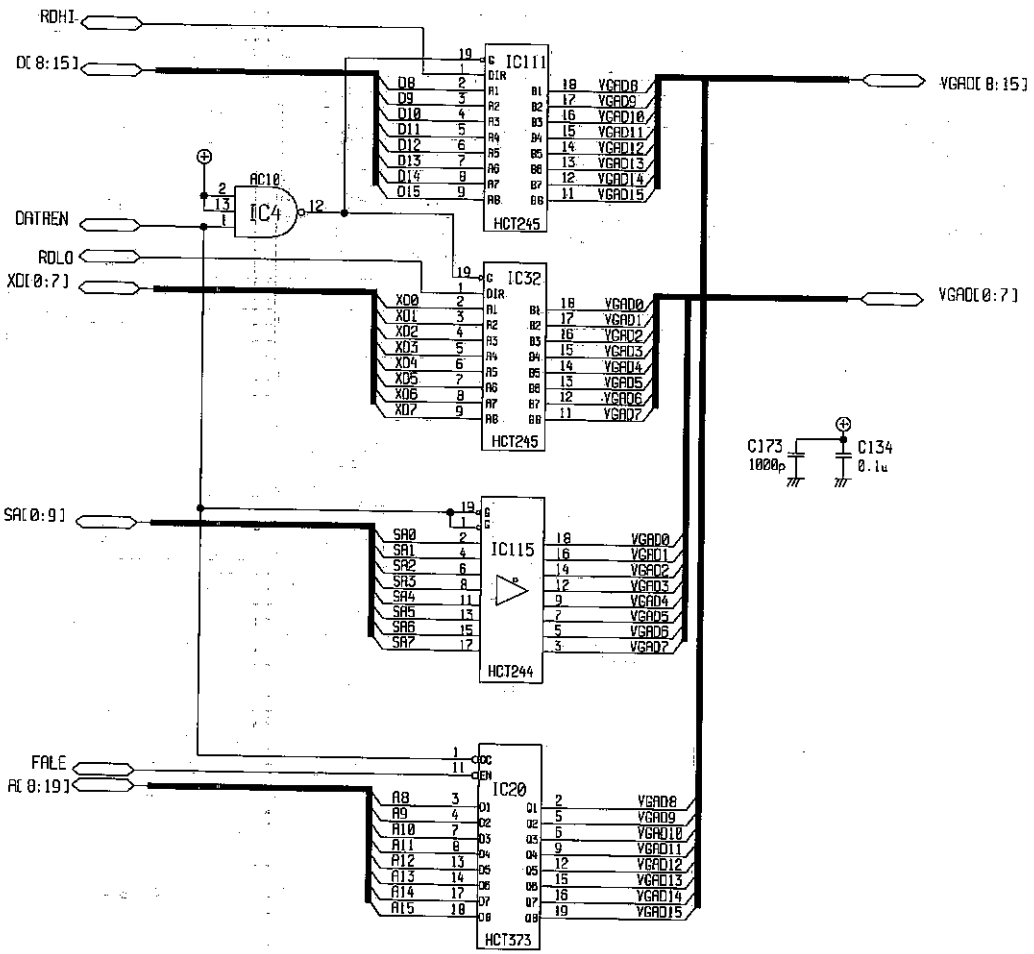
13-4. ROM & Printer I/F



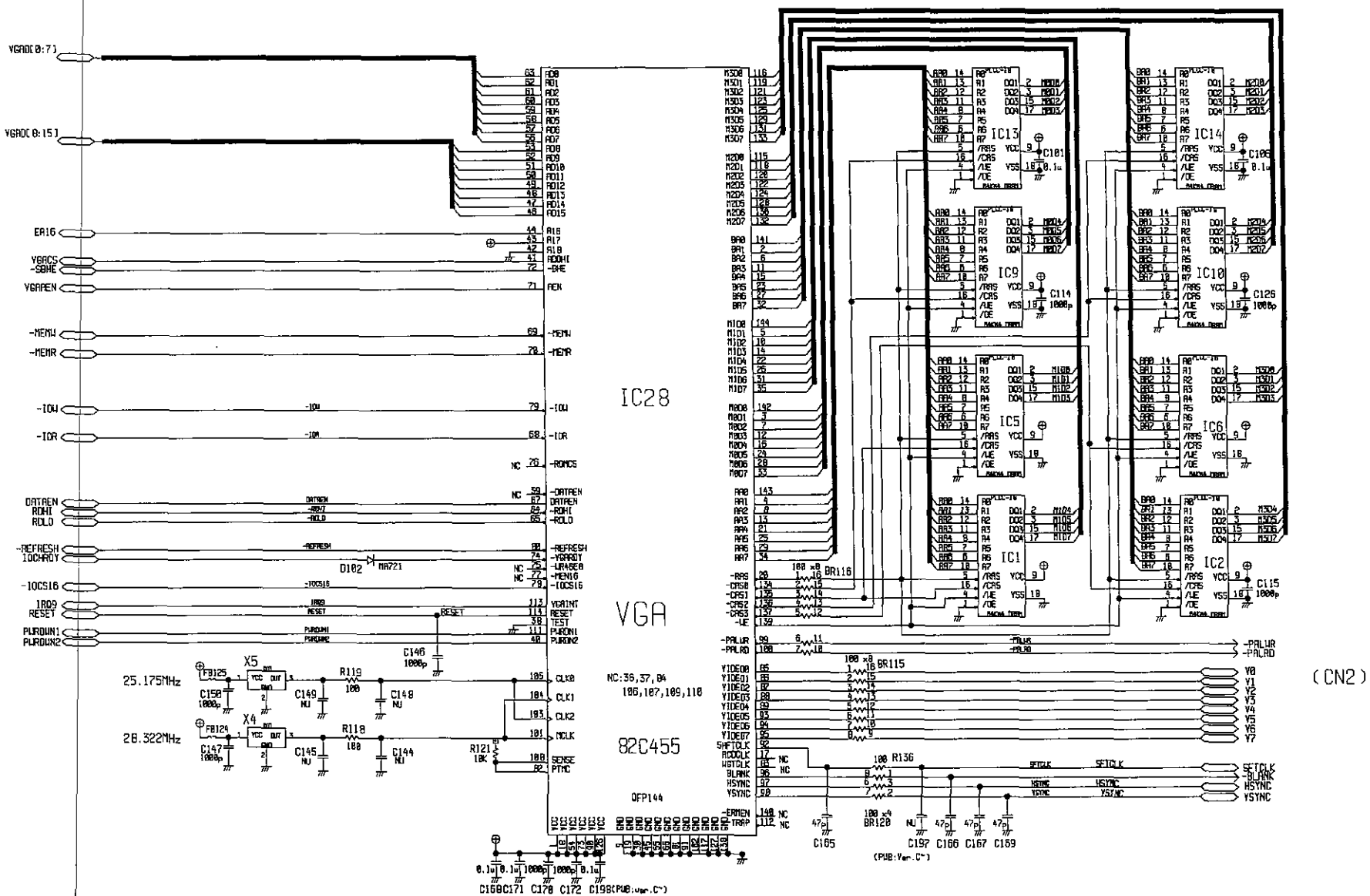
13-5. Key I/F & RTC



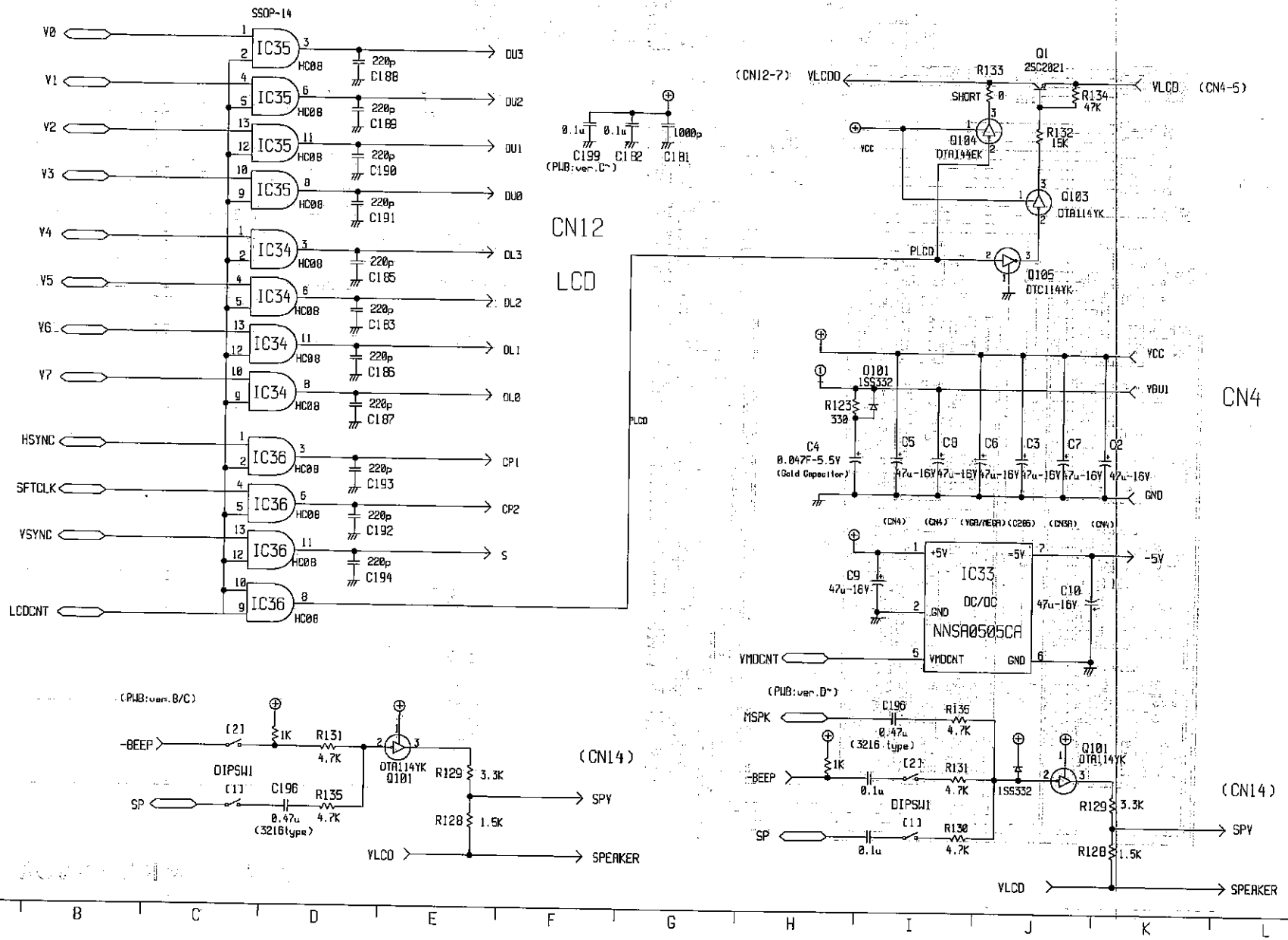
13-6. VGA Data/Address



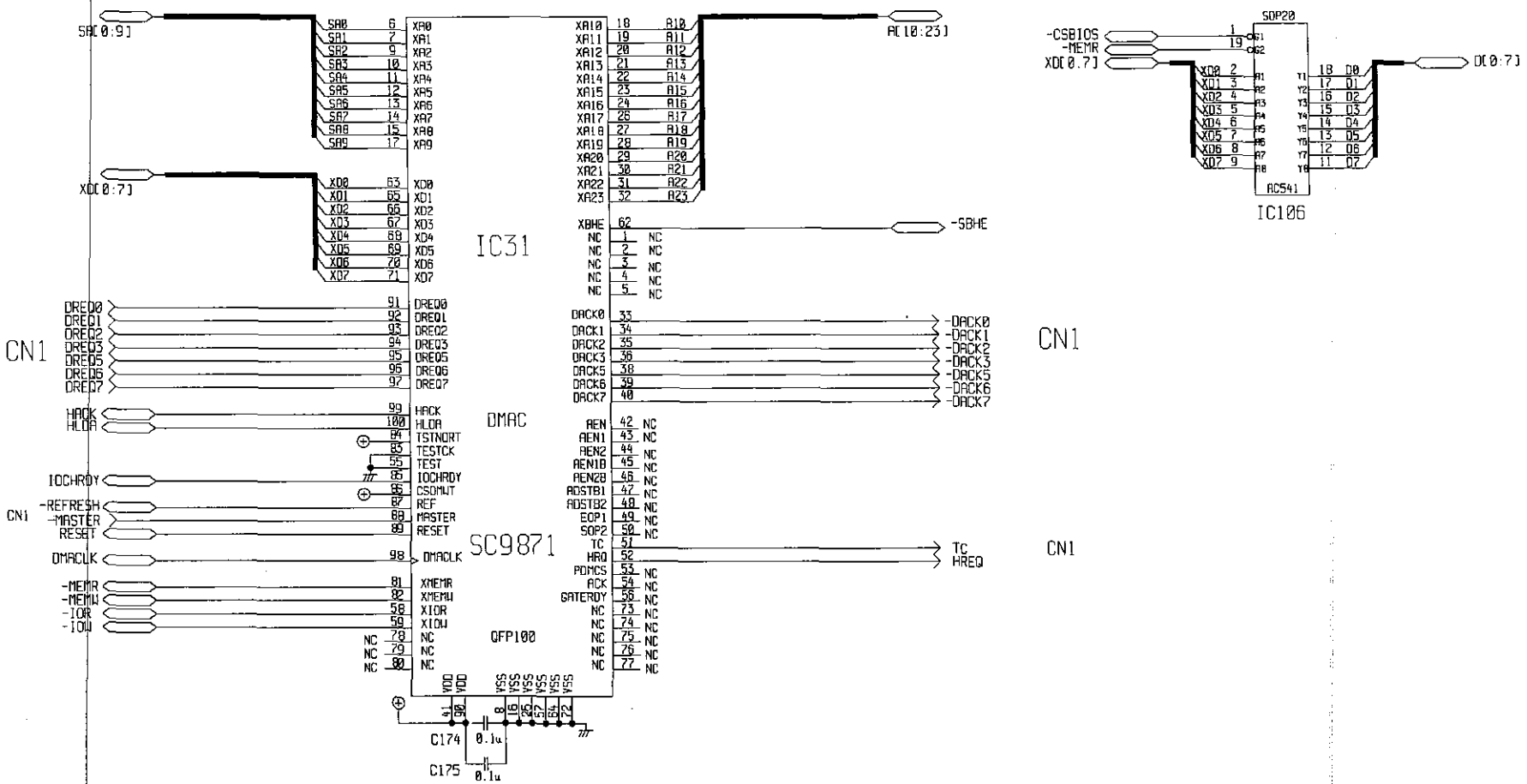
13-7. VGA controller & VRAM



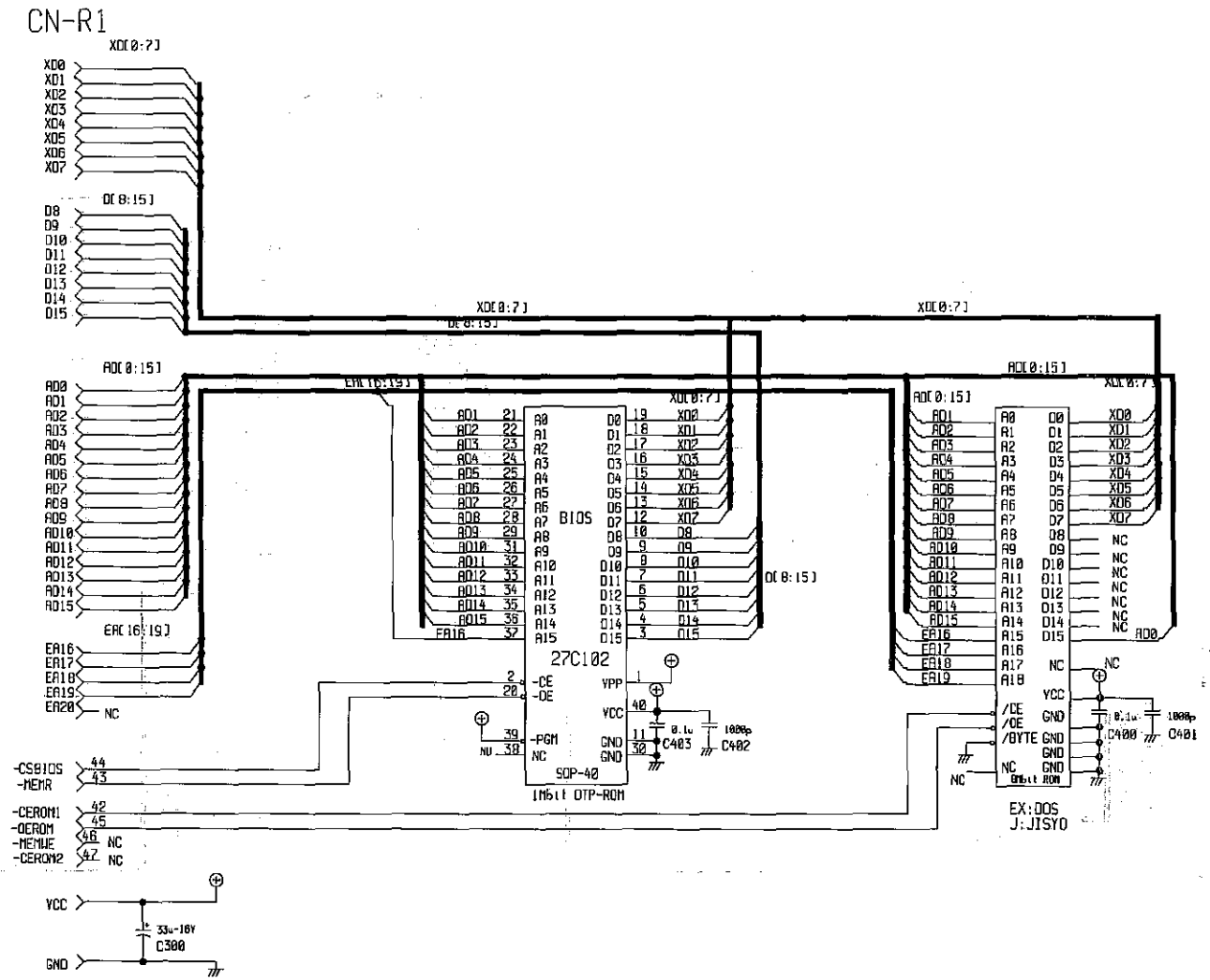
13-8. LCD OUT P/S speaker



13-9. DMAC


IC31
DMAC
SC9871
QFP100
CN1
SA[0:9]
XD[0:7]
XA[10:23]
-SBHE
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
HACK
HLDA
IOCHRDY
-REFRESH
-MASTER
RESET
DMACLK
-MEMR
-MEMW
-IOR
-IOW
-DACK0
-DACK1
-DACK2
-DACK3
-DACK5
-DACK6
-DACK7
TC
HREQ
C174
0.1u
C175
0.1u
-CSBIOS
-MEMR
XD[0.7]
D[0:7]
SOP20
AC541
IC106

13-10. ROM board unit (1Mbit-OTP)



13-11. Main PWB connector Table-(1)

CN1 EX-UNIT

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	SD15	61	GND
2	SD14	62	-MASTER
3	SD13	63	VCC
4	SD12	64	DREQ7
5	SD11	65	-DACK7
6	SD10	66	DREQ6
7	SD9	67	-DACK6
8	SD8	68	DREQ5
9	-MEMW	69	-DACK5
10	-MEMR	70	DREQ0
11	A17	71	-DACK0
12	A18	72	IRQ14
13	A19	73	IRQ15
14	A20	74	IRQ12
15	A21	75	IRQ11
16	A22	76	IRQ10
17	A23	77	-IOCS16
18	-SBHE	78	-MEMCS16
19	GND	79	GND
20	SA0	80	GND
21	SA1	81	VCC
22	SA2	82	VCC
23	SA3	83	ALE
24	SA4	84	TC
25	SA5	85	-DACK2
26	SA6	86	IRQ3
27	SA7	87	IRQ4
28	SA8	88	IRQ5
29	SA9	89	IRQ6
30	A10	90	IRQ7

CN1 EX-UNIT (CONT)

PIN NO.	SIGNAL	PIN NO.	SIGNAL
31	A11	91	CLK
32	A12	92	-REFRESH
33	A13	93	DREQ1
34	A14	94	-DACK1
35	A15	95	DREQ3
36	A16	96	-DACK3
37	VCC	97	-IOR
38	VCC	98	-IOW
39	VCC	99	PWRGOOD
40	AEN	100	DIR245
41	IOCHRDY	101	-EN245
42	XD0	102	GND
43	XD1	103	-OWS
44	XD2	104	GND
45	XD3	105	DREQ2
46	XD4	106	GND
47	XD5	107	IRQ9
48	XD6	108	GND
49	XD7	109	RESET
50	-IOCHCK	110	GND
51	HLDA	111	NC
52	EALE	112	-SELEXIO
53	KBCLK0	113	KBCLKI
54	KBDATA0	114	KBDATAI
55	NC	115	NC
56	NC	116	NC
57	NC	117	NC
58	NC	118	NC
59	-INTKEY	119	NC
60	-EXUNIT	120	AT/-XT (NC)

CN3A HDD CONNECTOR

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	-RESET	2	GND
3	XD7	4	D8
5	XD6	6	D9
7	XD5	8	D10
9	XD4	10	D11
11	XD3	12	D12
13	XD2	14	D13
15	XD1	16	D14
17	XD0	18	D15
19	GND	20	NC
21	NC	22	GND

CN3B HDD CONNECTOR

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	-IOW	2	GND
3	-IOR	4	GND
5	NC	6	NC
7	NC	8	GND
9	IRQ14	10	-IOCS16
11	SA1	12	NC
13	SA0	14	SA2
15	-HDCS0	16	-HDCS1
17	-HDACT	18	GND
19	VCC	20	VCC
21	GND	22	VCC

13-12. Main PWB connector Table-(2)

CN2 MODEM & CRT

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	VCC	35	GND
2	GND	36	VCC
3	-5V	37	-SELMD
4	SA0	38	SA1
5	SA2	39	SA3
6	SA4	40	SA5
7	SA6	41	SA7
8	SA8	42	SA9
9	RESET	43	-MORST
10	MSPK	44	INTMDM
11	-CSMDM	45	-IOR
12	-IOW	46	VMDCNT
13	-MRI	47	VCC
14	XD0	48	XD1
15	XD2	49	XD3
16	XD4	50	XD5
17	XD6	51	XD7
18	AEN	52	IRQ10
19	IRQ11	53	IRQ5
20	VGAD0	54	VGAD1
21	VGAD2	55	VGAD3
22	VGAD4	56	VGAD5
23	VGAD6	57	VGAD7
24	PWRDWN1	58	-ENCRT
25	SFTCLK	59	-PALRD
26	GND	60	-PALWR
27	V0	61	V1
28	V2	62	V3
29	V4	63	V5
30	V6	64	V7
31	-BLANK	65	VSYNC
32	HSYNC	66	-SENSE_CRT
33	VCC	67	GND
34	GND	68	VCC

CN4 P/S POWER

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	VCC	2	VCC
3	VCC	4	VBU1
5	VLCD	6	VAC
7	GND	8	GND
9	VBD	10	VBD
11	TEMP (GND)	12	CB
13	B_GND	14	B_GND

CN5 P/S SIGNAL

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	NC	2	ON RSM
3	PWRGOOD	4	RSMSW (NC)
5	RSMKEY (NC)	6	FB
7	LB	8	-BEEP
9	NC		

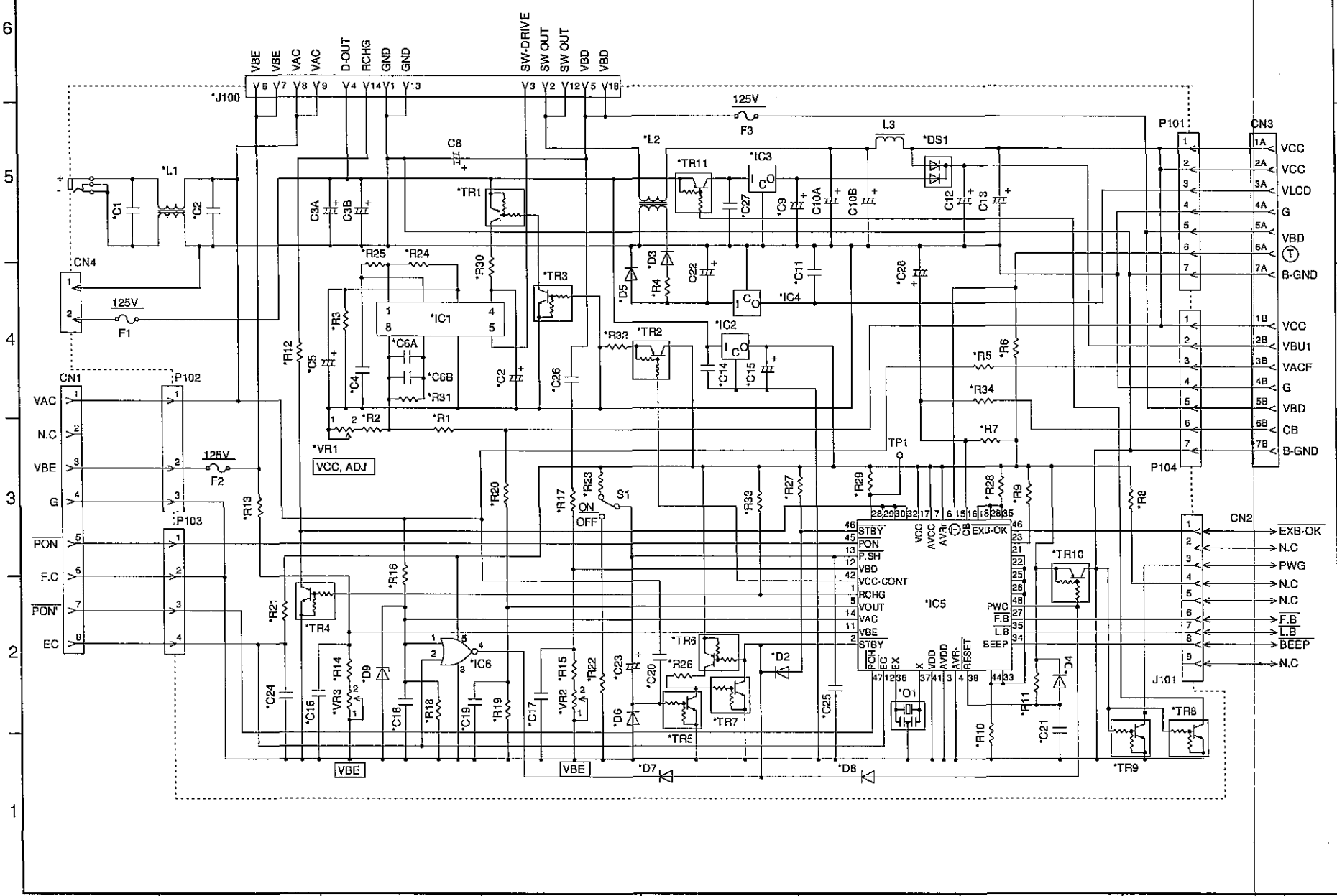
CN6 EX-RAM A

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	VCC	26	GND
2	CSEL4	27	CSEL5
3	CSEL2	28	CSEL3
4	-REFR	29	MA18
5	MA17	30	MA16
6	MA15	31	MA14
7	MA13	32	MA12
8	MA11	33	MA10
9	MA9	34	MA8
10	MA7	35	MA6
11	MA5	36	MA4
12	MA3	37	MA2
13	GND	38	GND
14	-PSCEL0	39	-PSCEL1
15	-PSCEH0	40	-PSCEH1
16	-PSOE	41	-PSWE
17	D15	42	D14
18	D13	43	D12
19	D11	44	D10
20	D9	45	D8
21	D7	46	D6
22	D5	47	D4
23	D3	48	D2
24	D1	49	D0
25	GND	50	VCC

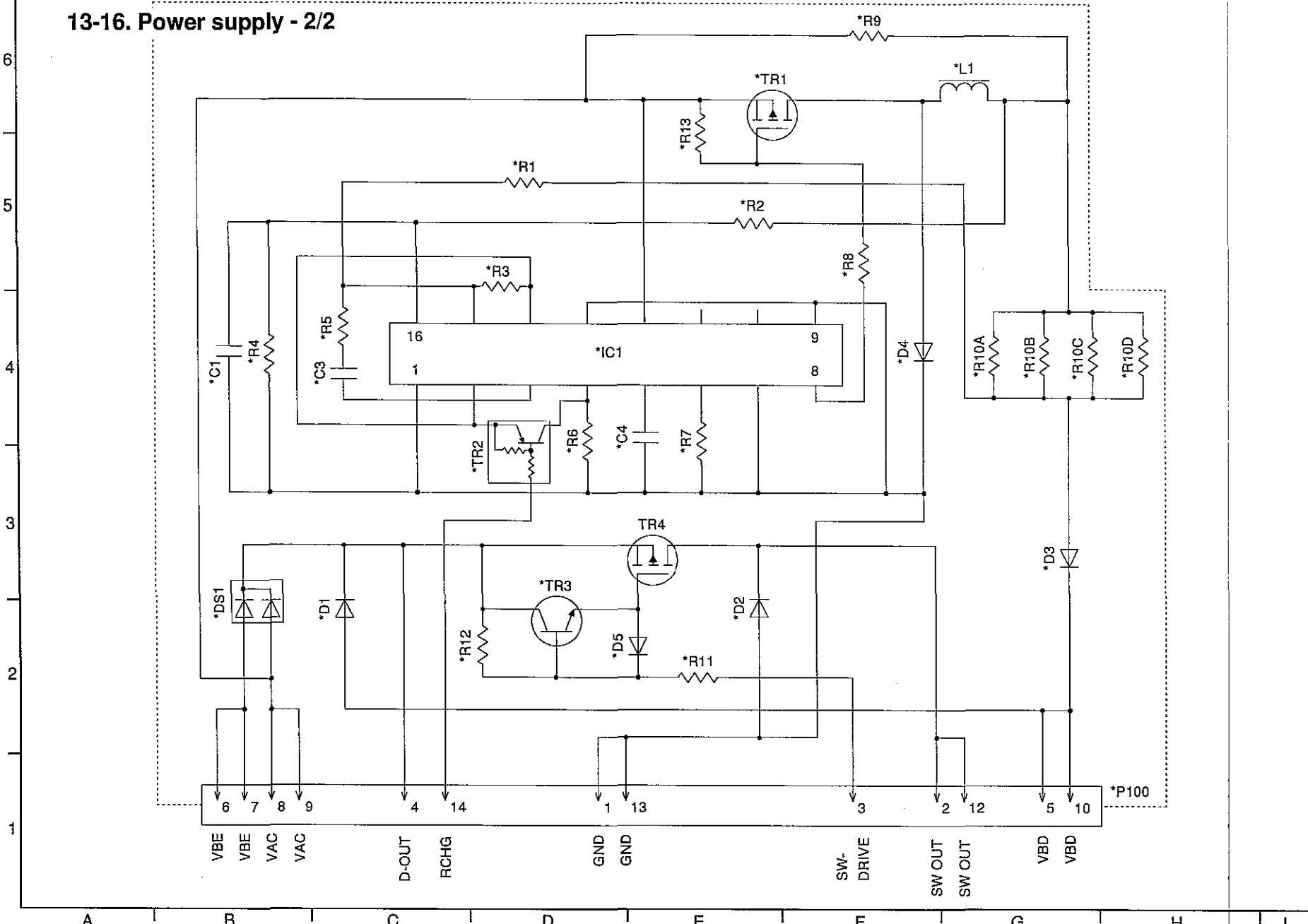
CN7 EX-RAM B

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	VCC	26	GND
2	CSEL6	27	CSEL7
3	CSEL4	28	CSEL5
4	-REFR	29	MA18
5	MA17	30	MA16
6	MA15	31	MA14
7	MA13	32	MA12
8	MA11	33	MA10
9	MA9	34	MA8
10	MA7	35	MA6
11	MA5	36	MA4
12	MA3	37	MA2
13	GND	38	GND
14	-PSCEL0	39	-PSCEL1
15	-PSCEH0	40	-PSCEH1
16	-PSOE	41	-PSWE
17	D15	42	D14
18	D13	43	D12
19	D11	44	D10
20	D9	45	D8
21	D7	46	D6
22	D5	47	D4
23	D3	48	D2
24	D1	49	D0
25	GND	50	VCC

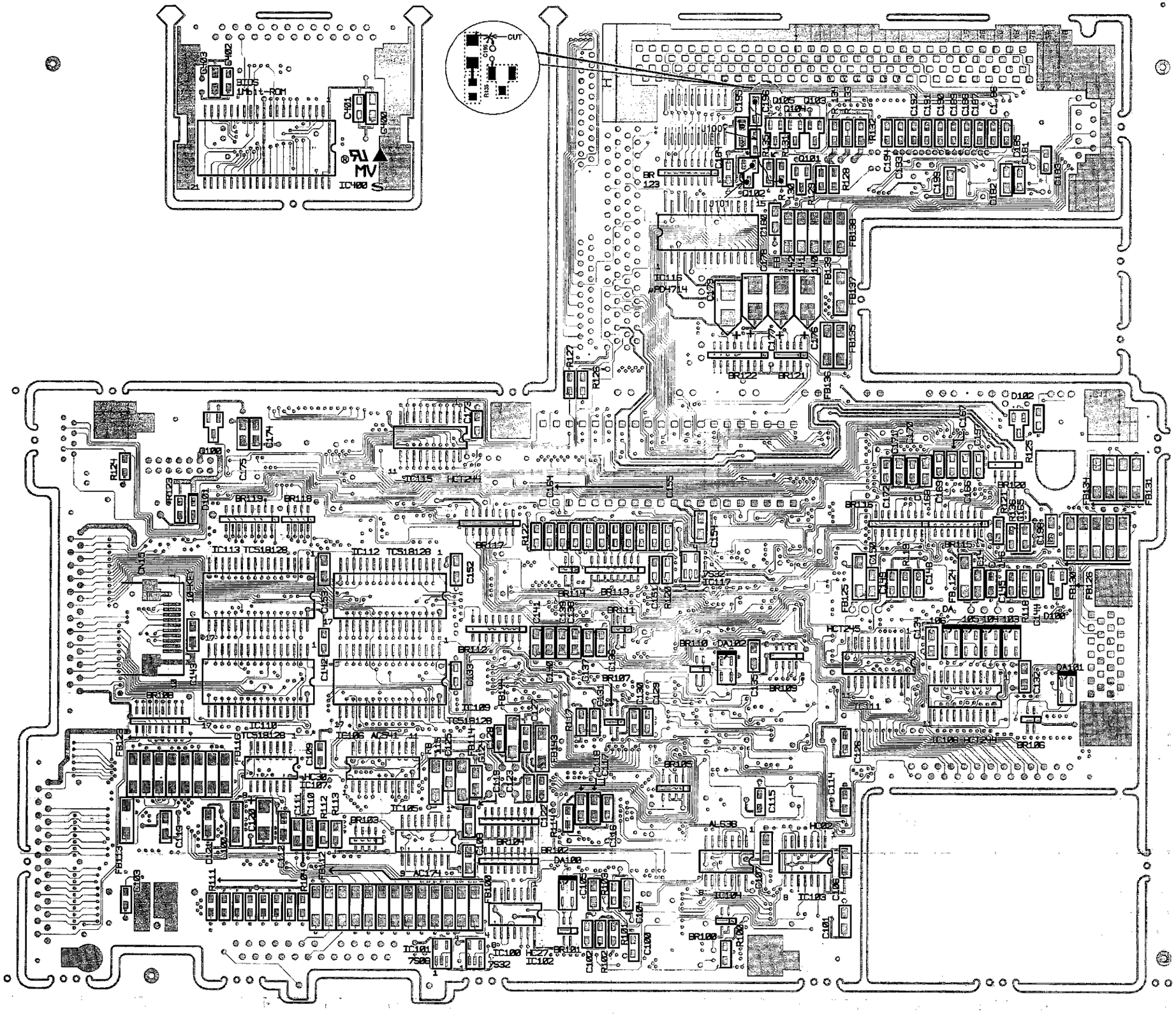
13-15. Power supply - 1/2



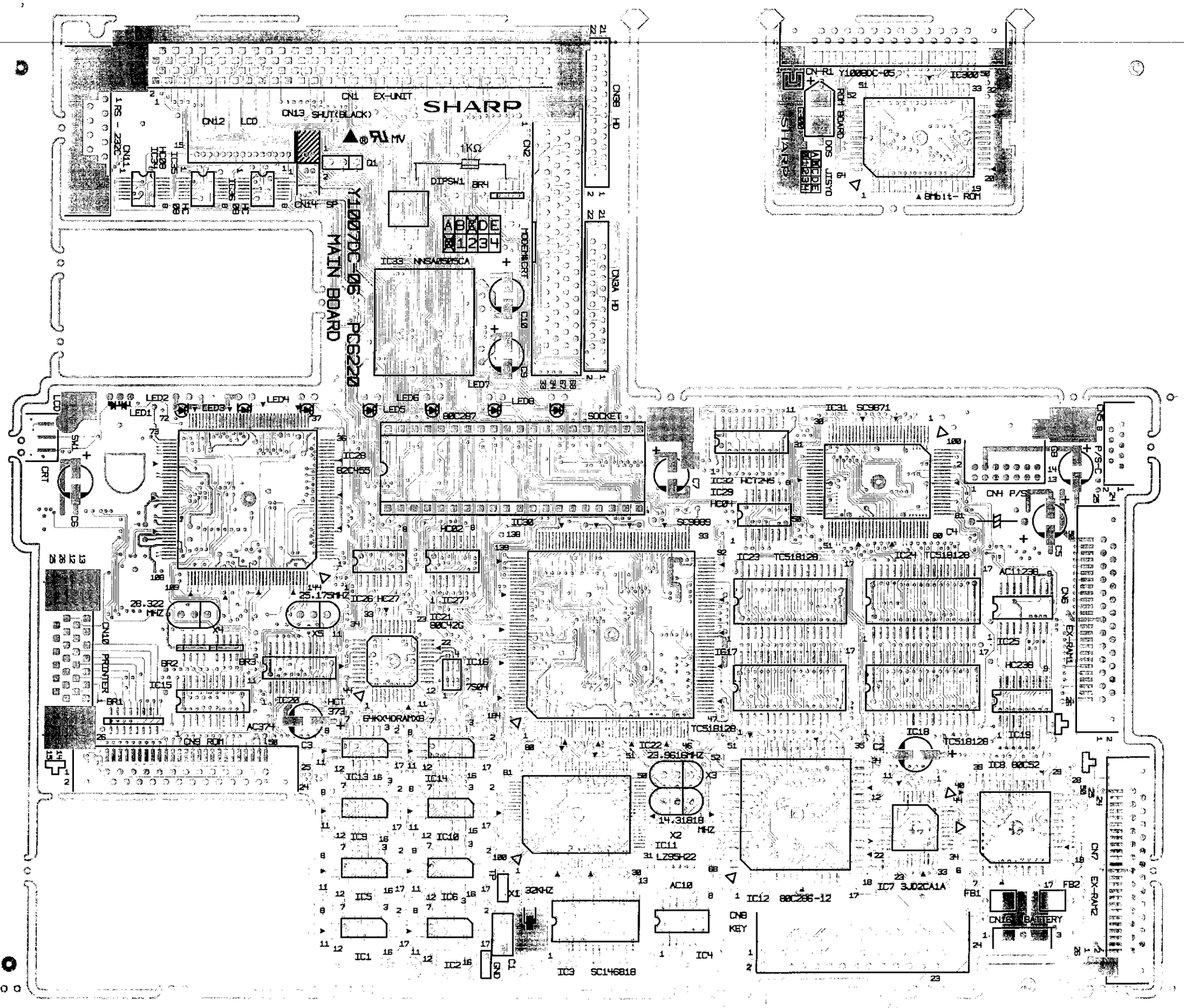
13-16. Power supply - 2/2



PC-6220


CUT
1Mbit-ROM
IC400
IC115 HCT244
IC113 TC518128
IC112 TC518128 1
IC110 TC518128 1
IC109 TC518128
IC106 AC541
IC105
IC101 7S08
IC100 HC27
IC102
IC117 7S32
IC107 HC30
IC104 AC174
IC103
IC108 HCT245
IC116 AHC7414
IC111 AL538
IC114 HC02
DA100
DA101
DA102
D100
D101
D102
D103
D104
D105
BR100
BR101
BR102
BR103
BR104
BR105
BR106
BR107
BR108
BR109
BR110
BR111
BR112
BR113
BR114
BR115
BR116
BR117
BR118
BR119
BR120
BR121
BR122
BR123
Q101
Q102

13-14. Main board and ROM board layout



13-13. Main PWB connector Table-(3)

CN8 KEY MTX

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	Y0	2	Y1
3	Y2	4	Y3
5	Y4	6	Y5
7	Y6	8	X16
9	Y7	10	NC
11	NC	12	NC
13	X0	14	X1
15	X2	16	X3
17	X4	18	X5
19	X6	20	X7
21	X8	22	X9
23	X10	24	X11

CN9 ROM

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	VCC	2	GND
3	GND	4	VCC
5	XD7	6	D8
7	XD6	8	D9
9	XD5	10	D10
11	XD4	12	D11
13	XD3	14	D12
15	XD2	16	D13
17	XD1	18	D14
19	XD0	20	D15
21	AD0	22	AD1
23	AD2	24	AD3
25	AD4	26	AD5
27	AD6	28	AD7
29	AD8	30	AD9
31	AD10	32	AD11
33	AD12	34	AD13
35	AD14	36	AD15
37	EA16	38	EA17
39	EA18	40	EA19
41	EA20	42	-CEDOS
43	-MEMR	44	-CSBIOS
45	-OEROM	46	-MEMWE
47	NC	48	GND
49	GND	50	VCC

CN10 PRINTER

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	-STROBE	14	-AUTFDX
2	DATA0	15	-ERROR
3	DATA1	16	-INIT
4	DATA2	17	-SLCTIN
5	DATA3	18	GND
6	DATA4	19	GND
7	DATA5	20	GND
8	DATA6	21	GND
9	DATA7	22	GND
10	-ACK	23	GND
11	PR_BUSY	24	GND
12	PE	25	GND
13	SELECT	26	CNTD

CN11 RS-232C

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	CD	6	DSR
2	RD	7	RTS
3	SD	8	CTS
4	DTR	9	CI
5	GND		

CN12 LCD

PIN NO.	SIGNAL
1	S
2	CP1
3	CP2
4	BLOFF
5	VCC
6	GND
7	VLCD0
8	DU0
9	DU1
10	DU2
11	DU3
12	DL0
13	DL1
14	DL2
15	DL3

CN13 PANNEL SW

PIN NO.	SIGNAL
1	SHUT
2	GND

CN14 SPEAKER

PIN NO.	SIGNAL
1	SPEAKER
2	SPV

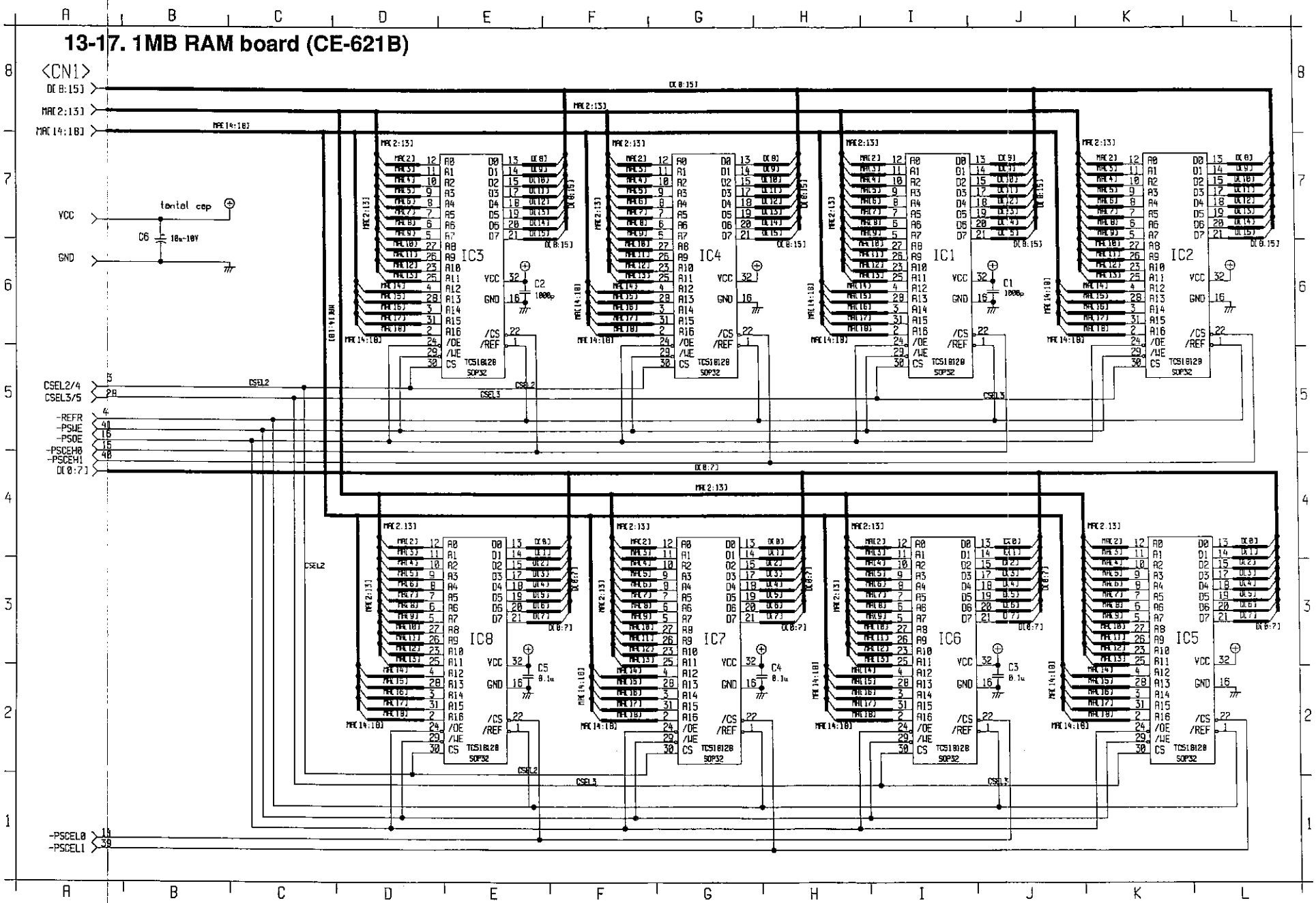
CN15 10-KEY

PIN NO.	SIGNAL
1	T1
2	T2
3	T3
4	T4
5	T5
6	T6
7	T7
8	T8
9	T9
10	GND

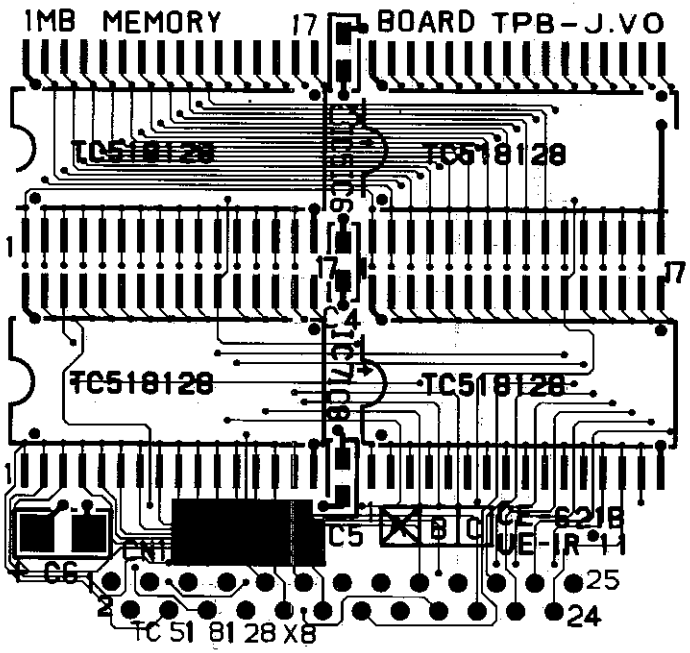
CN16BATTERY

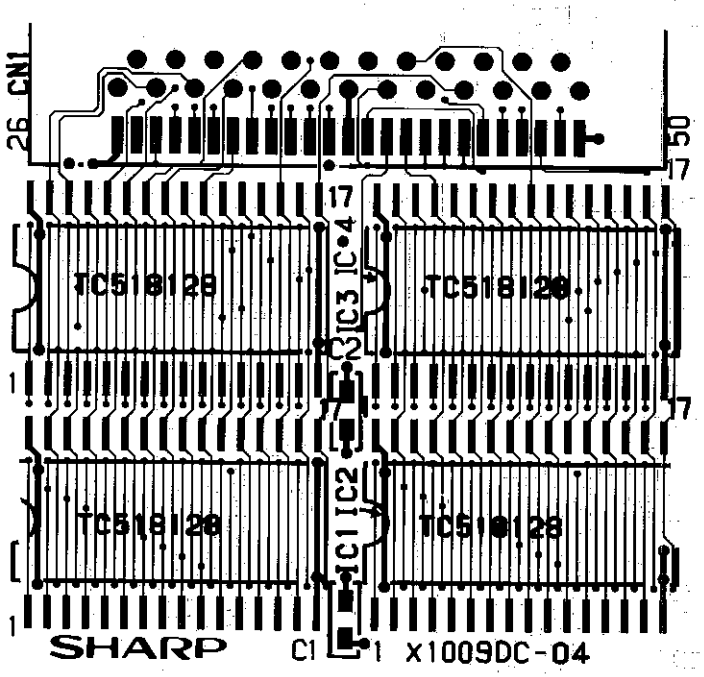
PIN NO.	SIGNAL
1	B_GND
2	CB
3	VBD

13-17. 1MB RAM board (CE-621B)



13-18. 1MB RAM board layout

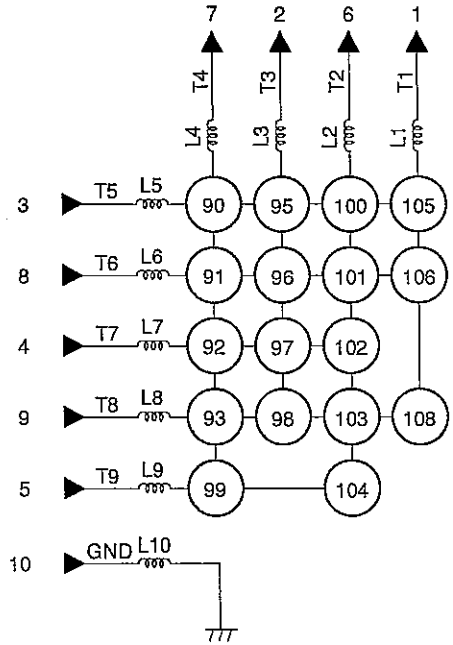


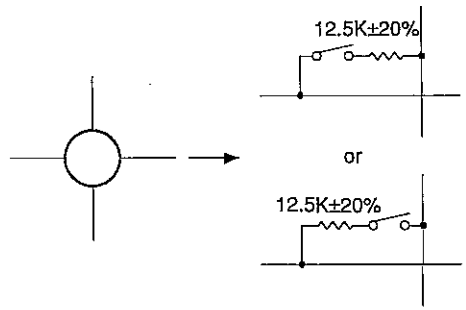


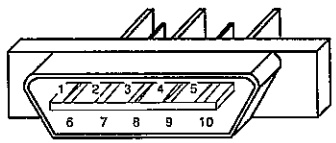
[CN1]

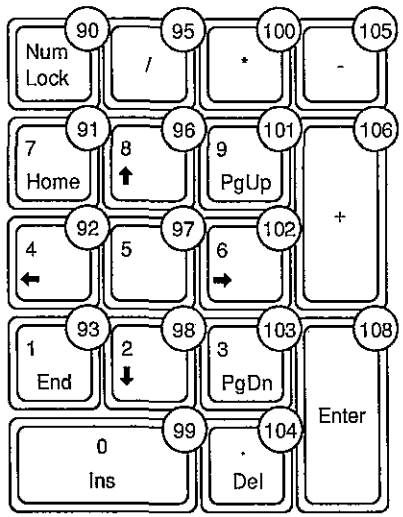
PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	VCC	26	GND
2	CSEL4	27	CSEL5
3	CSEL2	28	CSEL3
4	-REFR	29	MA18
5	MA17	30	MA16
6	MA15	31	MA14
7	MA13	32	MA12
8	MA11	33	MA10
9	MA9	34	MA8
10	MA7	35	MA6
11	MA5	36	MA4
12	MA3	37	MA2
13	GND	38	GND
14	-PSCEL0	39	-PSCEL1
15	-PSCEH0	40	-PSCEH1
16	-PSOE	41	-PSWE
17	D15	42	D14
18	D13	43	D12
19	D11	44	D10
20	D9	45	D8
21	D7	46	D6
22	D5	47	D4
23	D3	48	D2
24	D1	49	D0
25	GND	50	VCC

13-19. CE-621NK circuit



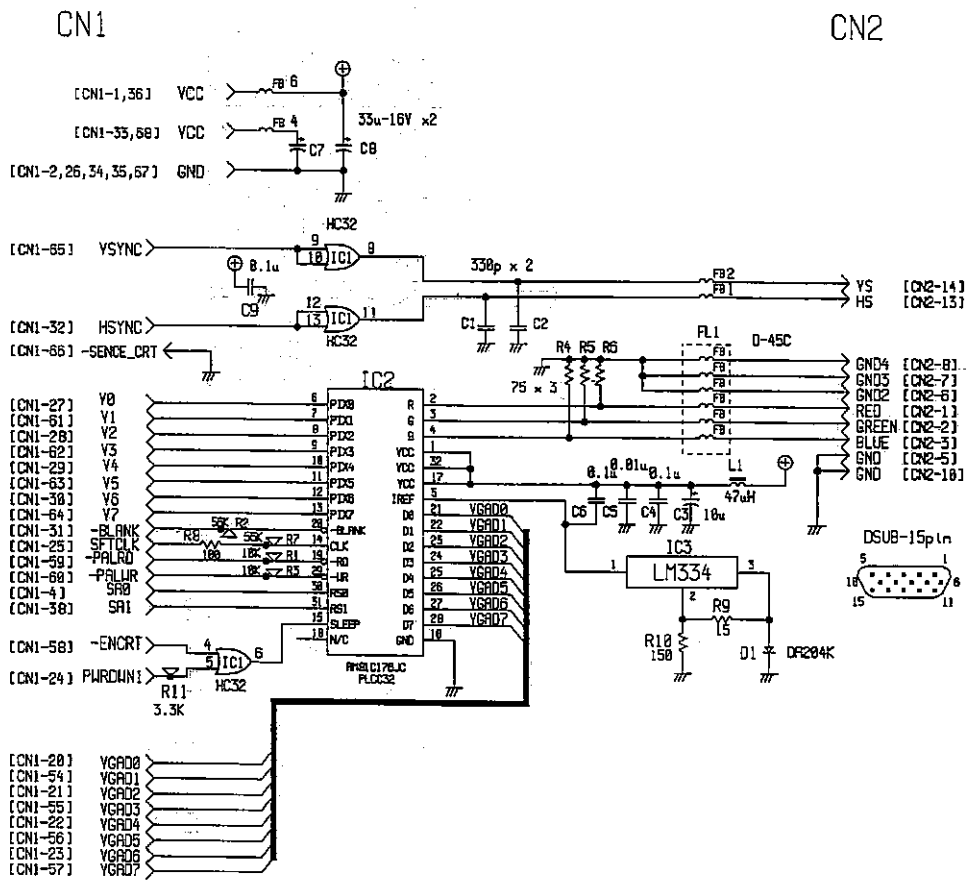






PIN NO.	SIGNAL
1	T1
2	T3
3	T5
4	T7
5	T9
6	T2
7	T4
8	T6
9	T8
10	GND

13-20. CRT adaptor (CE-621A)



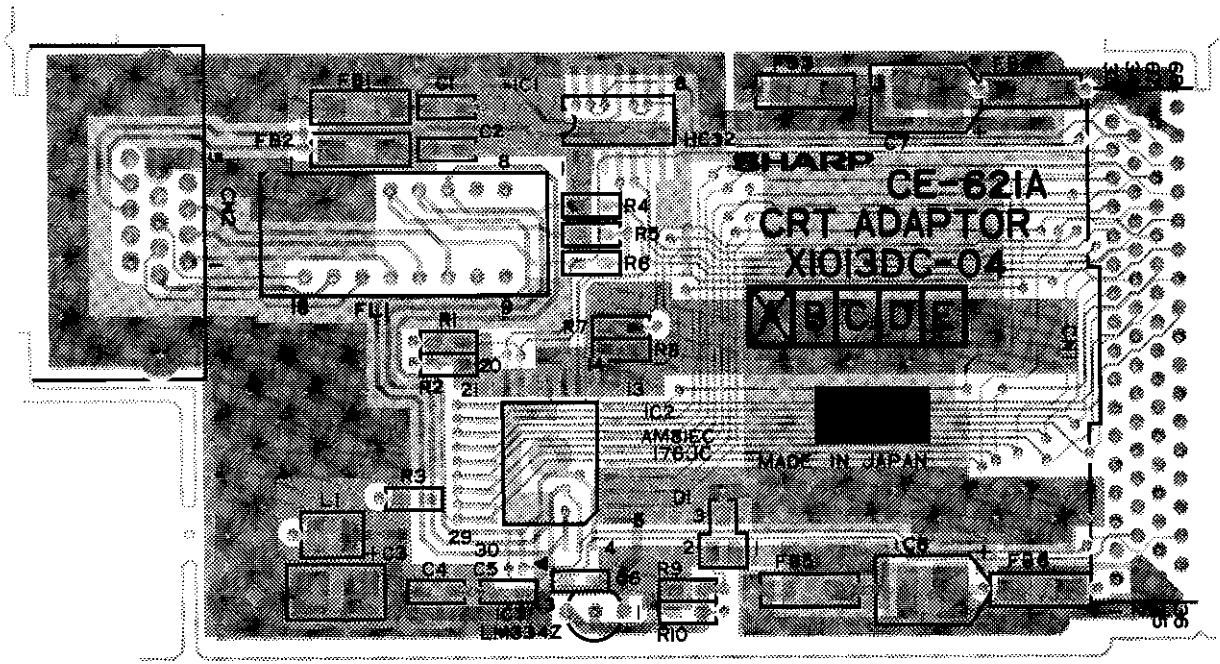
CN1

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	VCC	35	GND
2	GND	36	VCC
3	-5V	37	-SELMD
4	SA0	38	SA1
5	SA2	39	SA3
6	SA4	40	SA5
7	SA6	41	SA7
8	SA8	42	SA9
9	RESET	43	-MORST
10	MSPK	44	INTMDM
11	-CSMDM	45	-IOR
12	-IOW	46	VMDCNT
13	MRI	47	VBU1
14	XD0	48	XD1
15	XD2	49	XD3
16	XD4	50	XD5
17	XD6	51	XD7
18	AEN	52	IRQ10
19	IRQ11	53	IRQ5
20	VGAD0	54	VGAD1
21	VGAD2	55	VGAD3
22	VGAD4	56	VGAD5
23	VGAD6	57	VGAD7
24	PWRDWN1	58	-ENCRT
25	SFTCLK	59	-PALRD
26	GND	60	-PALWR
27	V0	61	V1
28	V2	62	V3
29	V4	63	V5
30	V6	64	V7
31	-BLANK	65	VSYNC
32	HSYNC	67	GND
33	VCC	67	GND
34	GND	68	VCC

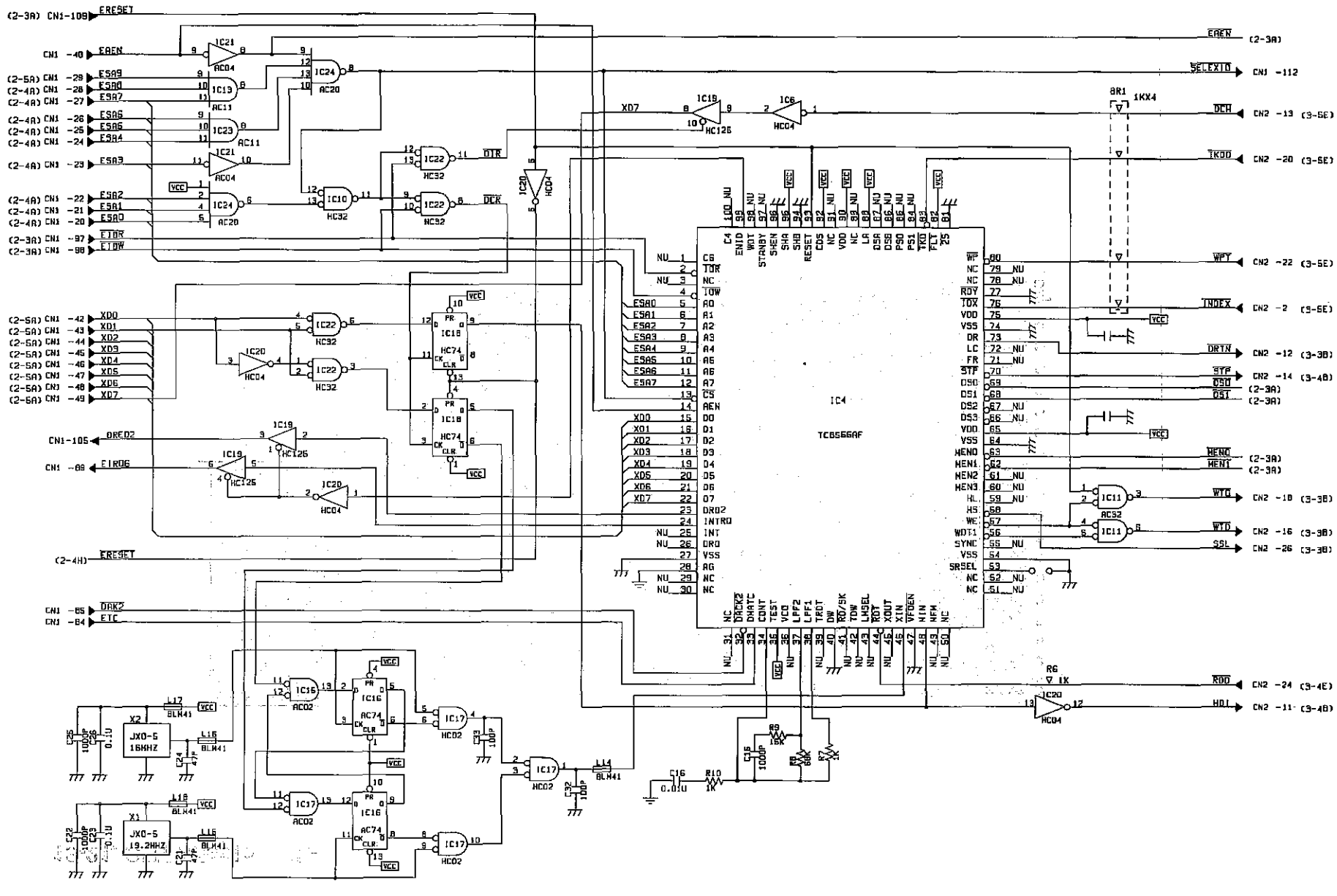
CN2

PIN NO.	SIGNAL
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND2
7	GND3
8	GND4
9	NC
10	GND
11	NC
12	NC
13	HS
14	VS
15	NC

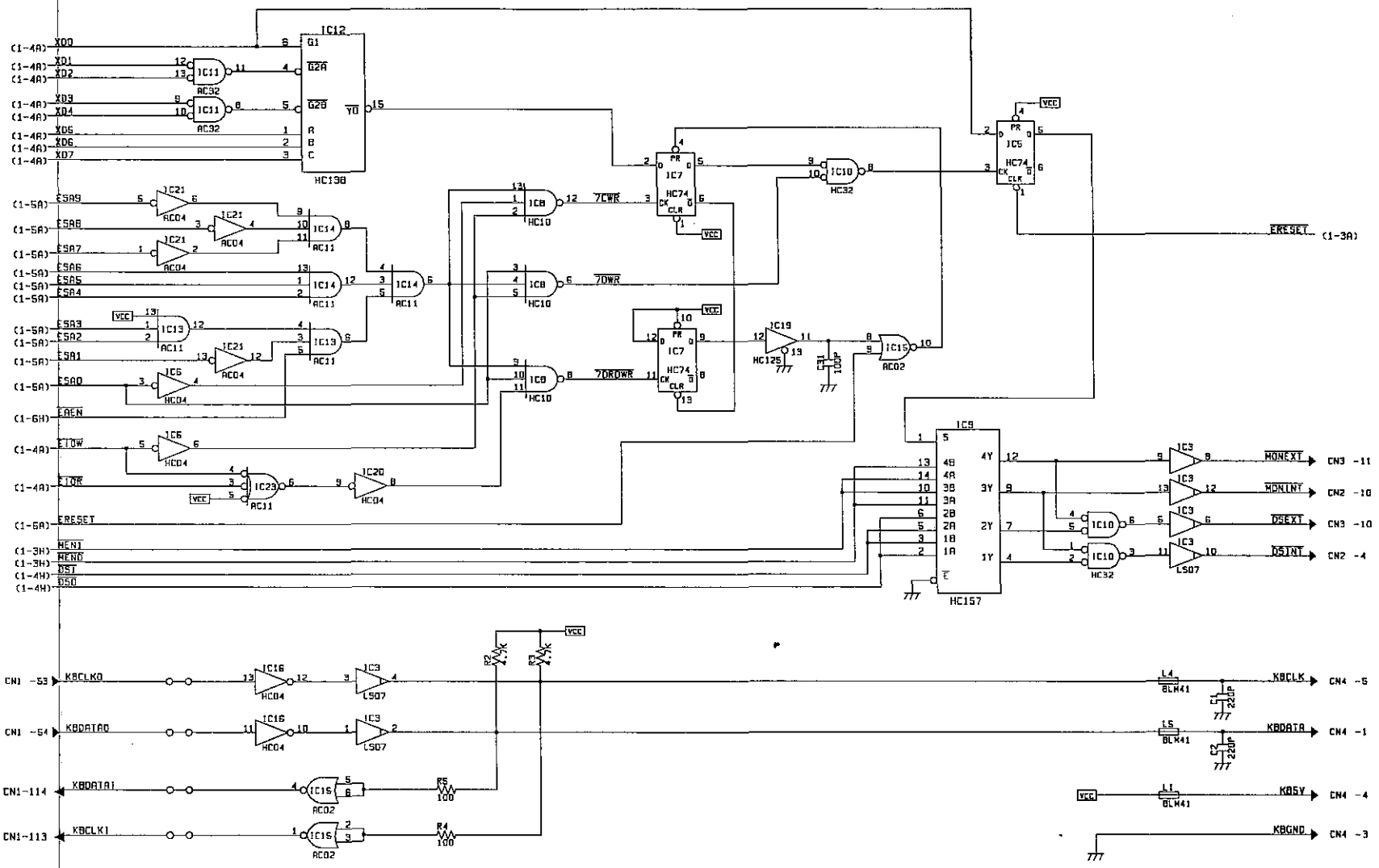
13-21. CRT adaptor (CE-621A) layout



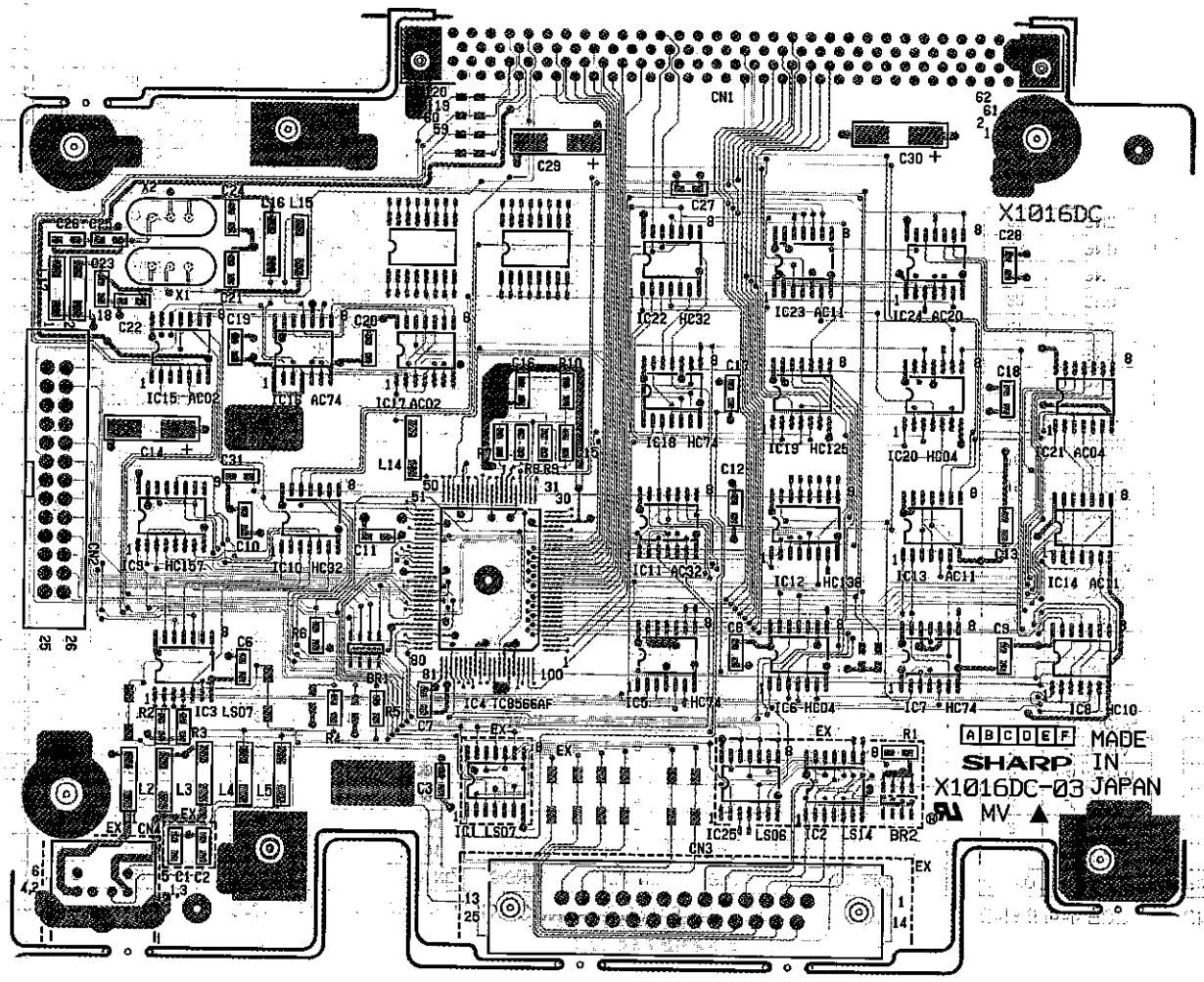
13-22. FD unit board (CE-621F) - 1/3



13-23. FD unit board (CE-621F) - 2/3



13-26. CE-621F board layout



SHARP PARTS GUIDE

PC-6220
CE-621A/CE-621B
CE-621F/CE-621NK
MODEL CE-621EV

CONTENTS

DESTINATION TABLE

U	USA	E	EJ	Korea
Y	Canada		ESH	South Africa
G	Germany, Austria		ESB	Saudi Arabia
H	U.Kingdom		ESG	Indonesia
Q	Australia		EH	Malaysia
K	Hong Kong			
S	Singapore			

DEFINITION

The definition of each Rank is as follows and also noted in the list

A : Parts necessary to be stocked as High usage parts.

B : Parts necessary to be stocked as Standard usage parts.

C : Low usage parts.

D : Parts necessary for refurbish.

E : Unit parts recommended to be stocked for efficient after sales service.

~~Please note that the lead time for the said parts may be longer than normal parts.~~

S : Consumable parts.

Please note that the following parts used in Copier under the same description are classified into A or B Rank depending upon the place used.

Example : Gear made of Metal, Sprocket, Bearing, Belt made of Rubber, Spring clutch mechanism.

A Rank : The parts which may be with the revolution or loading.

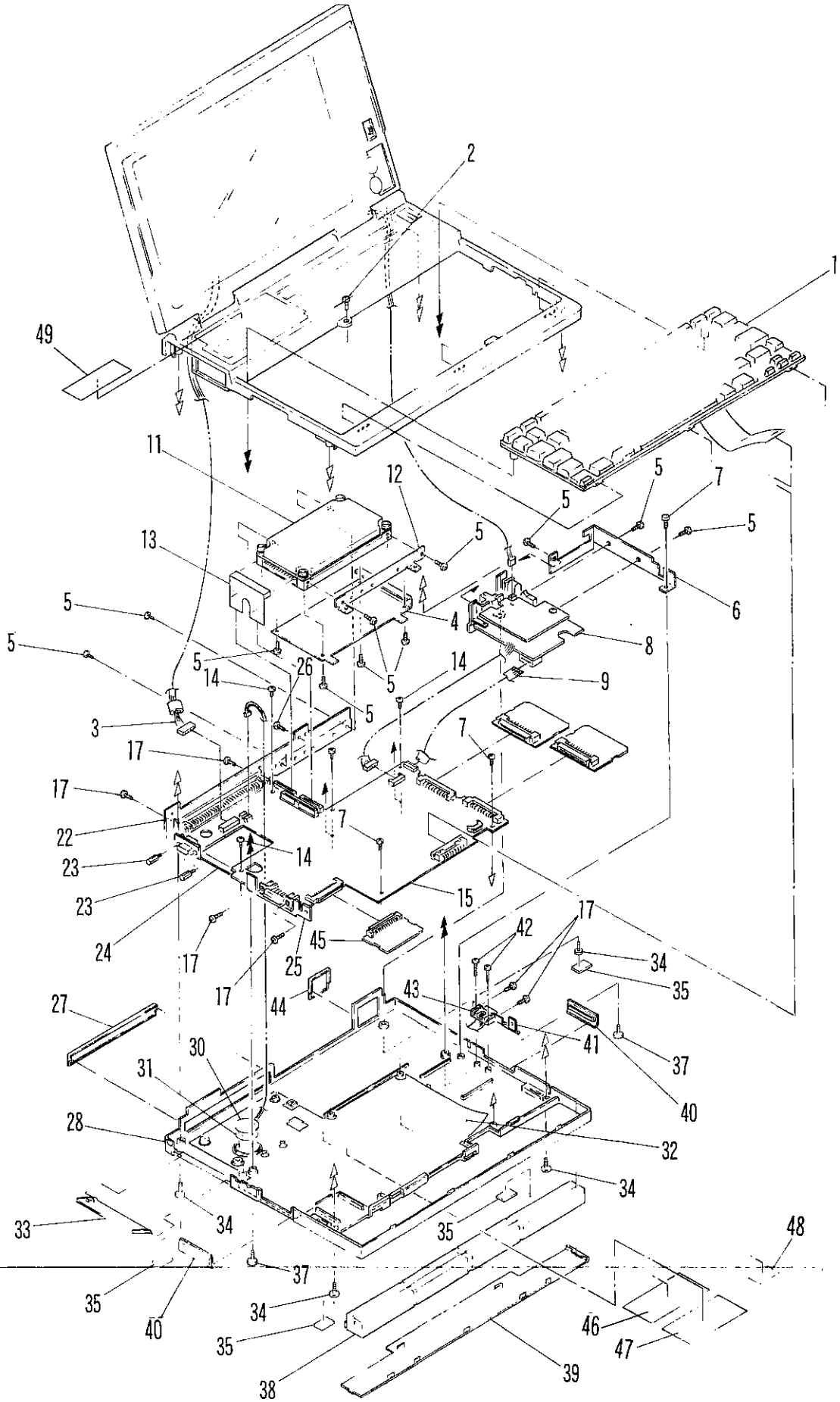
B Rank : Parts similar to A Rank parts, but are not included in Rank A.

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

1 PC-6220 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
	DUNT-1020DCZZ	BG	N	E	Keyboard	[Except H,G]
1	DUNT-1021DCZZ	BH	N	E	Keyboard	[G]
	DUNT-1022DCZZ	BH	N	E	Keyboard	[H]
2	LX-BZ1018ECZZ	AA		C	Screw	
3	QCNW-1011DCZZ	AW		C	LCD cable	
4	PSLDM1001DCZZ	AF	N	C	HD shield plate	
5	LX-BZ1187CCZZ	AA		C	Screw (2×2.8)	
6	LANGT1009DCZZ	AH	N	C	Hold angle D	
7	LX-BZ1155CCZZ	AA		C	Screw (2×3.5)	
8	RDENC1002DCZZ	BV	N	E	Power supply unit	
9	QPWBM1031DCZZ	AK	N	C	PS-FPC	
11	DUNTK1037DCZZ	**	N	E	HDD	
12	LANGT1007DCZZ	AE	N	C	HD angle	
13	QCNW-1018DCZZ	AX	N	C	HD harness	
14	LX-BZ1147CCZZ	AA		C	Screw	
15	CPWBY1007DC01	**	N	E	Main PWB unit	
17	XBPSN20P04000	AA		C	Screw (2×4)	
22	LANGT1008DCZZ	AH	N	C	Hold angle C	
23	LX-BZ1141CCZZ	AA		C	Screw	
24	LANGT1006DCZZ	AF	N	C	Hold angle B	
25	LANGT1005DCZZ	AF	N	C	Hold angle A	
26	XBSSF26P04000	AA		C	Screw (2.6×4)	
27	GCOVH1004DCZZ	AD	N	C	Connector cover EX	
28	GCABA1003DCZZ	BB	N	D	Cabinet A	
30	RALMB1002DCZZ	AM	N	B	Speaker	
31	PSHEZ1010DCZZ	AA	N	C	Speaker fixing sheet	
32	PSHEZ1009DCZZ	AF	N	C	Insulator sheet	
33	GCOVH1005DCZZ	AD	N	C	Connector cover RS	
34	XUPSD30P08000	AA		C	Screw (3×8)	
35	GLEGG1002DCZZ	AA	N	D	Rubber foot	
37	XBBSF30P06000	AA		C	Screw (3×6)	
38	UBATN1002DCZZ	BU		B	Battery	
39	GCOVH1006DCZZ	AN	N	D	Battery cover	
40	GCOVH1002DCZZ	AD	N	D	Connector cover CE	
41	LANGT1010DCZZ	AE	N	C	Hold angle E	
42	LX-BZ1199CCZZ	AA		C	Screw	
43	QCNW-1013DCZZ	AV	N	C	Connector cable (10pin)	
44	GCOVH1003DCZZ	AE	N	C	Connector cover PS	
45	DUNTK1090DC01	BG	N	E	ROM board unit	
46	TCAUS1001DCZZ	AC	N	D	Service label	
47	TLABS1009DCZZ	AC	N	D	F mark label	[G]
48	TLABZ1546ACSA	AC		D	TUV label	[G]
49	TLABM1004DCZZ	AF	N	D	Pop label	

1 PC-6220 Exteriors



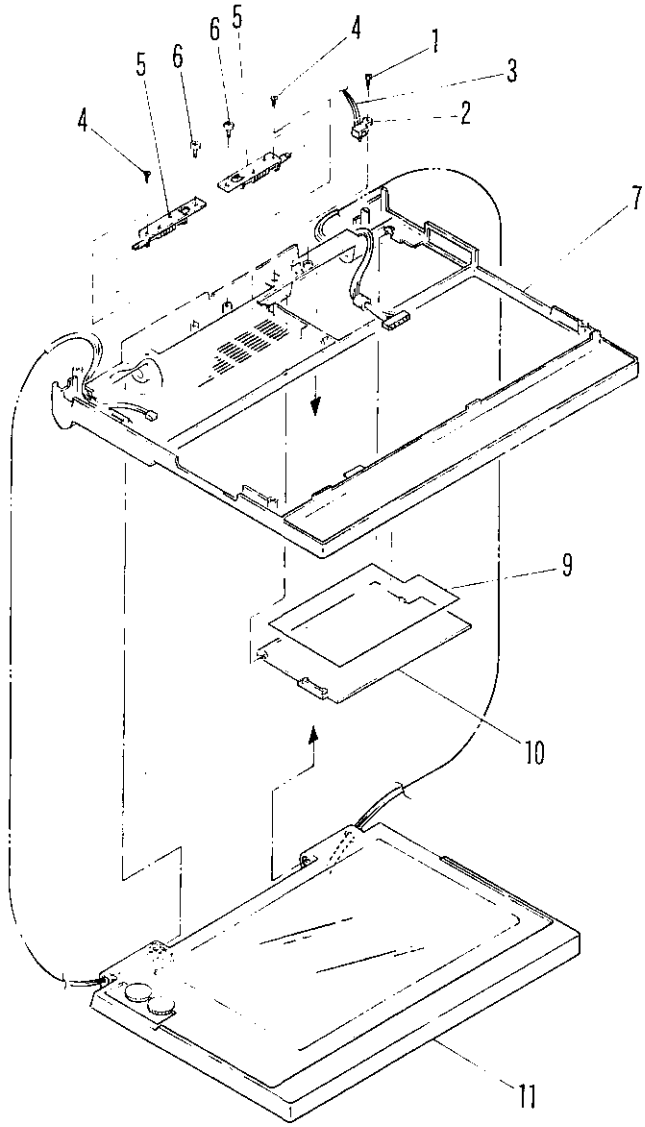
2 PC-6220 Top cabinet

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LX-BZ1147CCZZ	AA		C	Screw
2	QSW-P1004DCZZ	AE	N	B	Push switch
3	QCNW-1014DCZZ	AD	N	C	Harness (2pin)
4	XBSSD20P04000	AA		C	Screw (2×4)
5	PDMP-1001DCZZ	AL	N	C	Damper
6	XUSSD30P06000	AA		C	Screw (3×6)
7	GCABB1004DCZZ	BB	N	D	Cabinet B
9	PZETZ1004DCZZ	AB	N	C	Insulator sheet A
10	GCOVA1008DCZZ	AP	N	D	Option cover
11	DUNT-1038DCZZ	CQ	N	E	Display unit (include 4block)

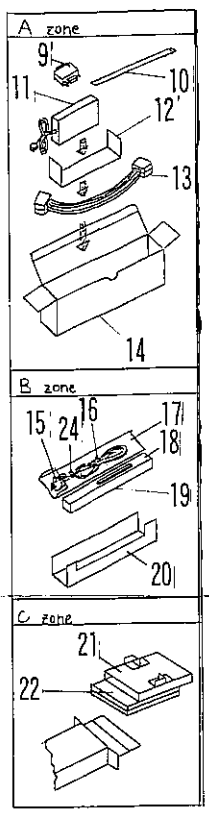
3 PC-6220 Packing material & Accessories

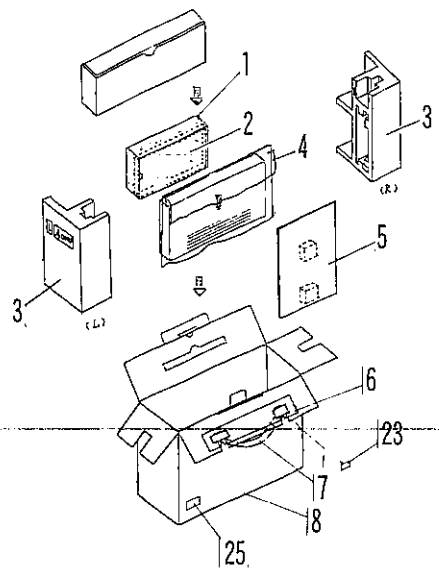
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKA1058DCZZ	AF	N	D	Manual case
2	TINSE1008DCZZ	AU	N	D	Instruction book (Laplink)
	TINSE1005DCZZ	AX	N	D	Instruction book (Operation) [U]
	TINSE1007DCZZ	AX	N	D	Instruction book (Operation) [Except U,Y,G]
	TINSE1006DCZZ	AX	N	D	Instruction book (Operation) [Y]
	CCADZ1003DC01	AM	N	D	Service information [U]
	TCADZ1075ACZZ	AF		D	Card [Except U]
	TGANE2002HCZZ	AN		C	Guaranty [Q]
3	SPAKA1011DCZZ	AM	N	D	Packing cushion A
4	SSAKH1028CCZZ	AA		D	Vinyl bag (320×380mm)
5	SPAKA1059DCZZ	AG		D	Packing cushion
6	SPAKA5416SCZZ	AB		D	Protector,handle (61400675)
7	JHNDP2008SCZZ	AB		C	Handle
8	SPAKC1015DCZZ	AU	N	D	Packing case
9	DUNT-1060DCZZ	BD	N	E	Connector box
10	LPLTP1004DCZZ	AF	N	C	Tem plate
⚠ 11	RADPA1004DCZZ	BS	N	B	AC adaptor [U,Y]
⚠ 11	RADPA1003DCZZ	BQ	N	B	AC adaptor [Except U,Y]
12	SPAKA1014DCZZ	AC	N	D	Packing cushion B
13	QCNW-1016DCZZ	BB	N	C	Laplink cable
14	SPAKA1012DCZZ	AG	N	D	Accessory case
⚠ 15	QACCB7621QCZZ	AN		B	AC cord [H,EH]
⚠ 15	QACCV6620QCZZ	AV		B	AC cord [G,K,ESG]
⚠ 15	QACCL7620QCZZ	AW		B	AC cord [Q]
⚠ 15	QACCD7611QCZZ	AT		B	AC cord [EJ]
⚠ 15	CCNW-2814SC01	AX		B	AC cord [ESB]
⚠ 15	QACCB7521QCZZ	AS		B	AC cord [ESH]
15	PHOG-1023CCZZ	AB		C	Protect sleeve [ESH]
15	QPLGA0018WRE0	AN		C	AC plug [ESH]
⚠ 15	QACCF7622QCZZ	AX	N	B	AC cord [S]
15	QPLGA0010UCZZ	AM		C	3P AC cord adaptor [EJ]
16	UBNDA1008CCZZ	AA		C	AC cord band (120mm)
17	SSAKA3001CCZZ	AA		D	Vinyl bag (140×360mm)
18	SSAKA0330QCZZ	AA		D	Vinyl bag (50×320mm)
19	UBATN1002DCZZ	BU		B	Battery
20	SPAKA1013DCZZ	AE	N	D	Packing cushion A for accessory
21	SPAKA1060DCZZ	AE	N	D	Packing cushion D
22	SSAKH3015CCZZ	AA		D	Vinyl bag (240×360mm)
23	TLABM2270SCZZ	AB		D	Packing label
24	TCAUS1054CCZZ	AB		C	AC cord caution label [H,EH]
25	TLABB1381ACZZ	AC		D	Label [Y]

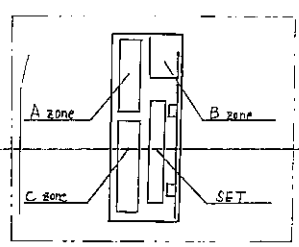
2 PC-6220 Top cabinet



3 PC-6220 Packing material & Accessories



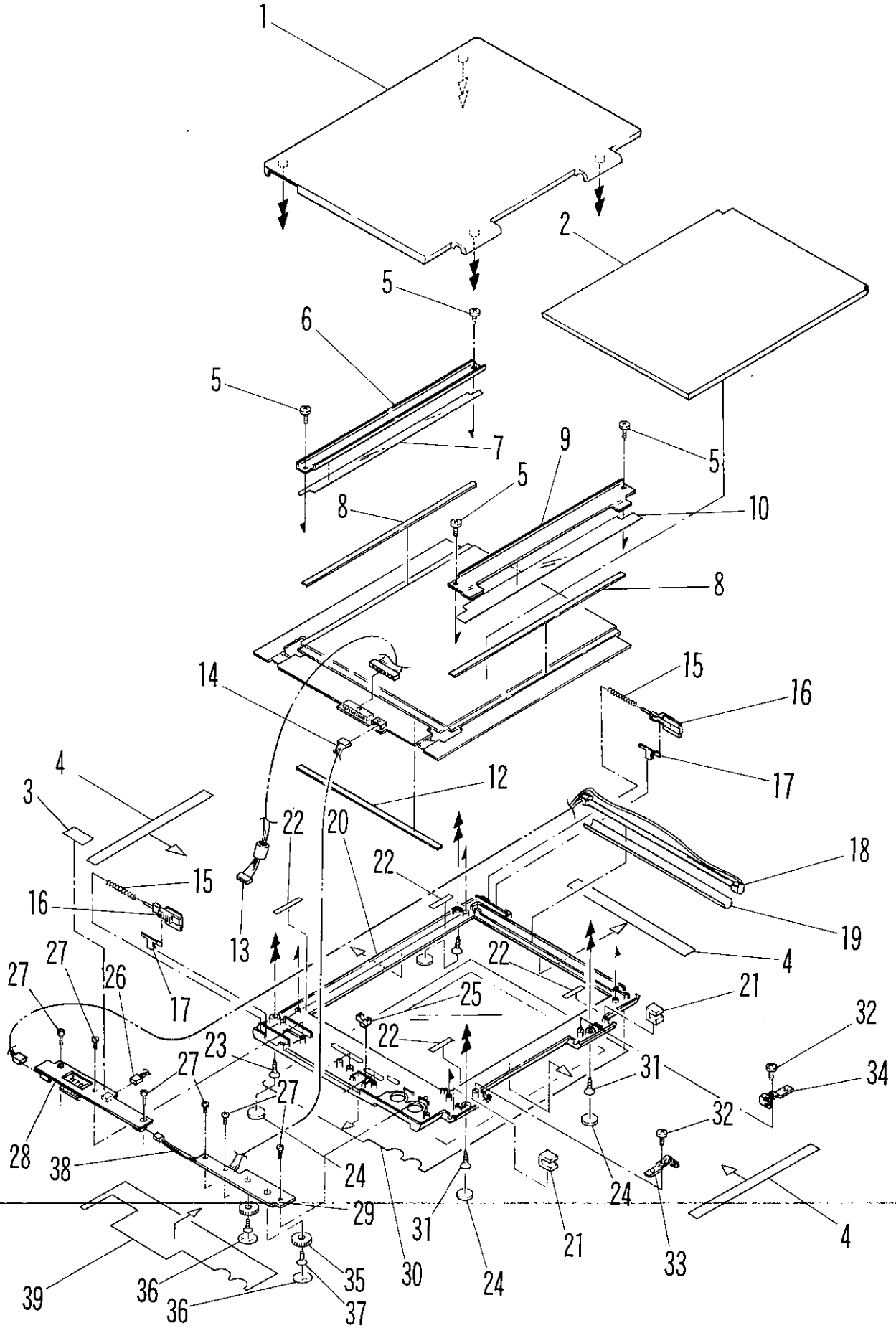




4 PC-6220 Display unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GCABC1009DCZZ	BB		D	Cabinet C
2	DUNTM1034DCZZ	BC		E	Optical conduct plate unit
3	TLABH1065DCZZ	AA	N	D	Caution label
4	PTPEZ1002DCZZ	AA		D	Tape B
5	XEBSD26P04000	AA		C	Screw (2.6×4)
6	LANGT1002DCZZ	AE		C	Install B
7	PZETZ1002DCZZ	AC		C	Insulator sheet B
8	PCUSS1007DCZZ	AD		C	Cushion A
9	LANGT1001DCZZ	AF		C	Install A
10	PZETZ1001DCZZ	AC		C	Insulator sheet A
12	PCUSS1008DCZZ	AD		C	Cushion B
13	QCNW-1011DCZZ	AW		C	LCD cable
14	QCNW-1009DCZZ	AF		C	VR cable
15	MSPRC1001DCZZ	AA		C	Spring
16	JBTN-1001DCZZ	AB		C	Stopper button
17	LSTPF1001DCZZ	AD		C	Stopper
18	DUNT-1033DCZZ	AW		E	CCFT unit
19	PSHEZ1008DCZZ	AE		C	Reflection sheet
20	GCABD1011DCZZ	AL		D	Cabinet D
21	LHLDW5023NCZZ	AB		C	Holder
22	PTPEH1323CCZZ	AA		C	Key sheet fixing tape
23	XESSD26P10000	AA		C	Screw (2.6×10)
24	PCAPZ1001DCZZ	AB		C	Rubber cap
25	JBTN-1002DCZZ	AB		C	Slide switch button
26	QCNW-1012DCZZ	AD		C	PS cable
27	LX-BZ1003DCZZ	AA		C	Screw
28	DUNTK1036DCZZ	BA		E	Inverter unit
29	CPWBF1019DC01	AZ	N	E	VR PWB unit
30	PSHEZ1005DCZZ	AZ		C	Display sheet
31	XUSSD26P07000	AA		C	Screw (2.6×7)
32	XUSSD26P06000	AA		C	Screw (2.6×6)
33	LANGT1003DCZZ	AD		C	Damper L
34	LANGT1004DCZZ	AD		C	Damper R
35	JBTN-1003DCZZ	AB		C	VR button
36	PSHEZ1007DCZZ	AA		C	VR sheet
37	LX-BZ1004DCZZ	AA		C	Screw
38	QCNW-1010DCZZ	AD		C	INV cable
39	PTPEZ1001DCZZ	AD		D	Tape A

4 PC-6220 Display unit



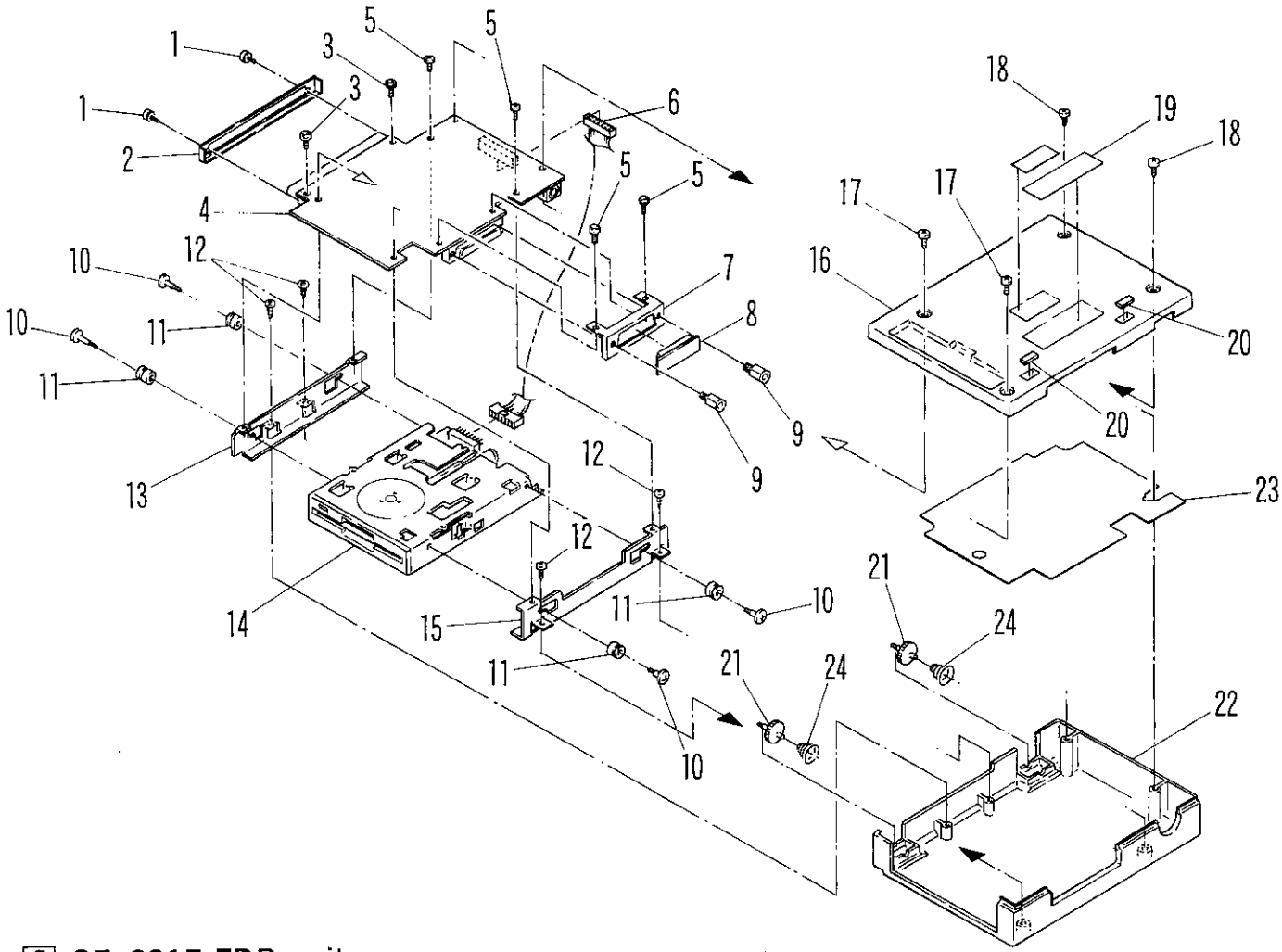
5 CE-621F Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	XBPSN20P04000	AA		C	Screw (2×4)
2	LANGQ1013DCZZ	AE	N	C	Connector angle B
3	XBBSD20P06000	AA		C	Screw (2×6)
4	CPWBX1016DC01		N	E	FDD I/F PWB unit
5	XBBSD30P06000	AA		C	Screw (3×6)
6	QCNW-1017DCZZ	AS	N	C	FD harness (26pin)
7	LANGQ1012DCZZ	AE	N	C	Connector angle A
8	PCAPH1016ACZZ	AD		C	25P cap
9	LX-BZ1141CCZZ	AA		C	Screw
10	LX-BZ1011DCZZ	AB		C	Screw
11	PGUMM1562CCZA	AD		C	Rubber
12	XUPSD30P08000	AA		C	Screw (3×8)
13	LANGT1015DCZZ	AF	N	C	FD angle R
14	DUNTK1062DCZZ	BW	N	E	FDD unit
15	LANGT1014DCZZ	AF	N	C	FD angle L
16	GCABA1012DCZZ	AX	N	D	Cabinet A
17	XBPSF30P06000	AA		C	Screw (3×6)
18	XUBSF30P10000	AA		C	Screw (3×10)
19	TLABG1025DCZZ	AC	N	D	Label [Y]
	TLABS1026DCZZ	AC	N	D	Label [G]
20	GLEGG1002DCZZ	AA		D	Rubber foot
21	LX-BZ1007DCZZ	AG		C	Screw
22	GCABB1013DCZZ	AY	N	D	Cabinet B
23	PSHEZ1012DCZZ	AF	N	C	Insulator sheet
24	MSPRC1005DCZZ	AA	N	C	Spring

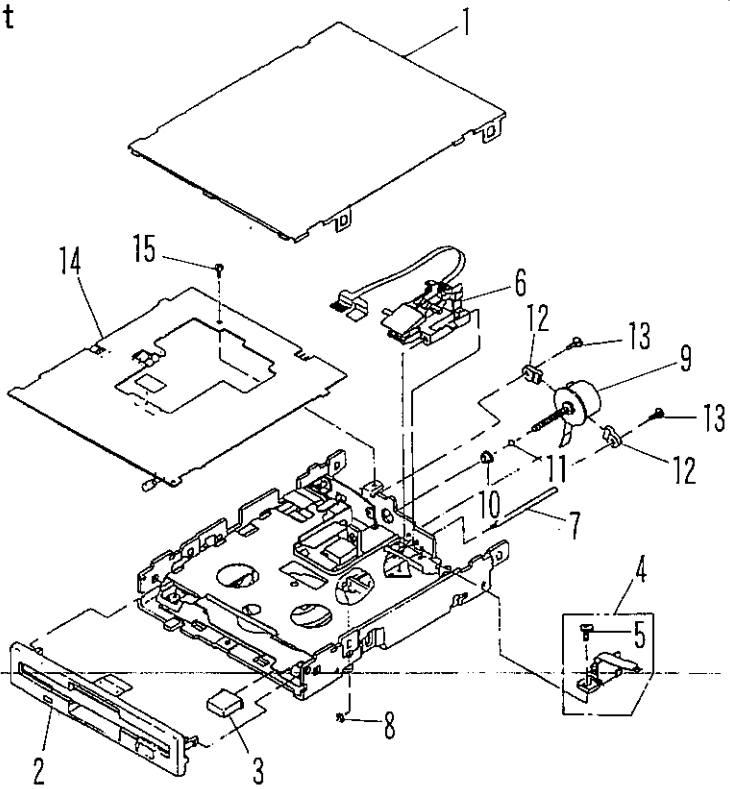
6 CE-621F FDD unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0iEK902157///	AM	N	D	Case
2	0iEK902156 03/	AN	N	D	Panel Ass'y(For 30)
3	0iEK320034 03/	AD	N	C	Komb(For 30)
4	0iEK902160///	AN	N	S	Track 00 Switch Ass'y
5	0iEXB12260405	AA	N	C	Screw
6	0iEK790700///	BR	N	B	Head Ass'y
7	0iEK160205///	AG	N	C	Guide Bar
8	0iEXD21200122	AA	N	C	E type Ring
9	0iEK790740///	BB	N	B	Stepping Motor
	0iEK790742///	BB	N	B	Stepping Motor
10	0iEK790741///	AK	N	C	Pivot Bearing
	0iEK790677///	AK	N	C	Pivot Bearing
11	0iEK790678///	AA	N	C	Ball
12	0iEK410793///	AB	N	C	Clapper
13	0iEXB12260405	AA	N	C	Screw
14	0iEK902193///	BQ	N	E	PCB Ass'y
16	0iEE162000 26/	AA	N	C	Screw
	(Unit)				
901	DUNTK1062DCZZ	BW	N	E	FDD unit

5 CE-621F Exteriors



6 CE-621F FDD unit



7 CE-621NK Ten key pad

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	00P40AAA0131A	BA	N	D	Upper case
2	00P74AAA0123A	AN	N	C	Torsion bar
3	00P2B72AA005A	AG	N	C	T screw
4	00P2A09AA002A	AG	N	C	M screw
5	00P4KA4AA019A	AV	N	C	Connector
6	00P62AAA0271A	AV	N	C	Plate
7	00P2A02AA005A	AG	N	C	M screw
8	00P4KA4AA020A	BH	N	C	Connector
9	00P2C02AA002A	AG	N	C	W screw
10	00P42AAA0271C	BF	N	C	Sub case
11	00P72AAA0052A	AN	N	C	Bushing
12	00P49AAA2002A	AR	N	D	Label
13	00P2B72AA001B	AG	N	C	T screw
14	00P41AAA0103A	BA	N	D	Lower case
101	00PJ1AAA2006B	BL	N	C	Key top ass'y

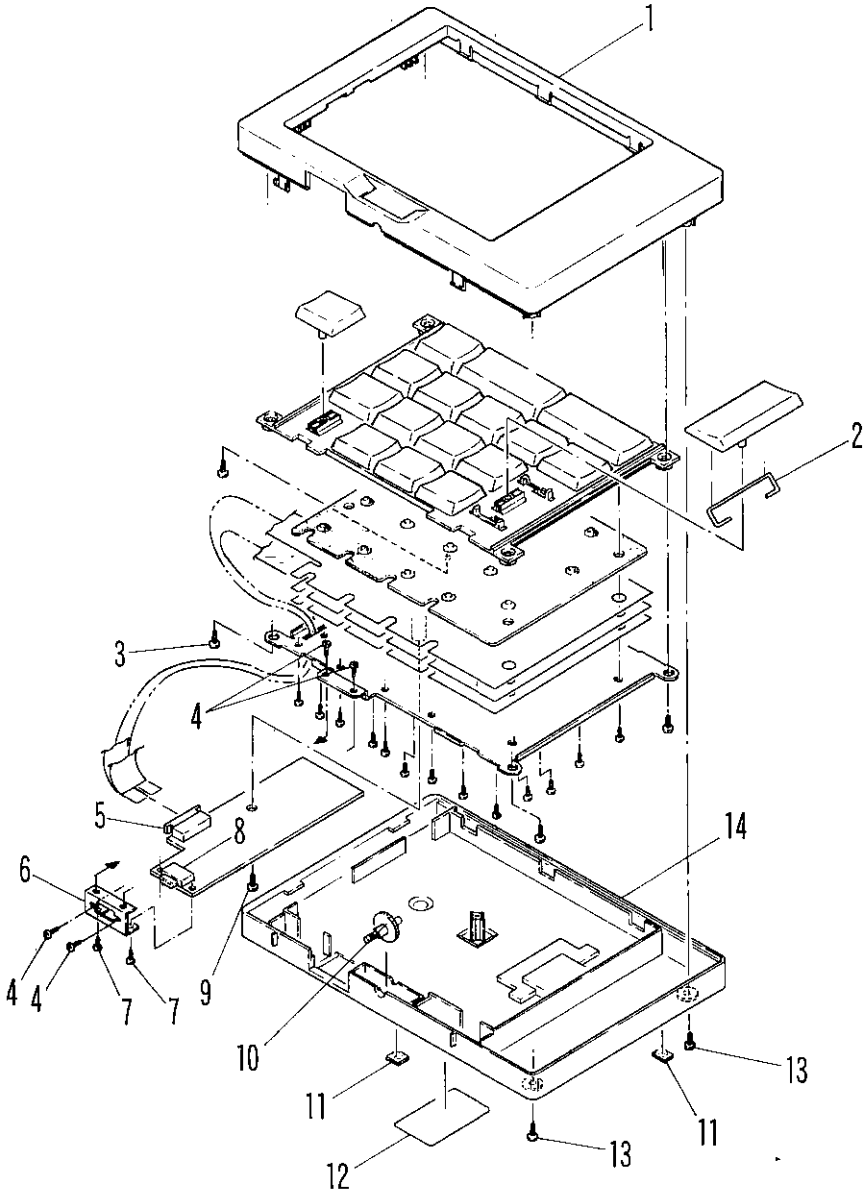
8 CE-621EV Battery pack

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	0DBCABiNET-AU	BH	N	D	Cabinet A(upper)
2	0DBBATT8-2200	BQ	N	B	Ni-cd
3	0DBCABiNET-B	BH	N	D	Cabinet B(lower)
4	0DBCONNECTOR	BF	N	C	Connector
5	0DBCHARGER-UT	CF	N	E	Charger unit

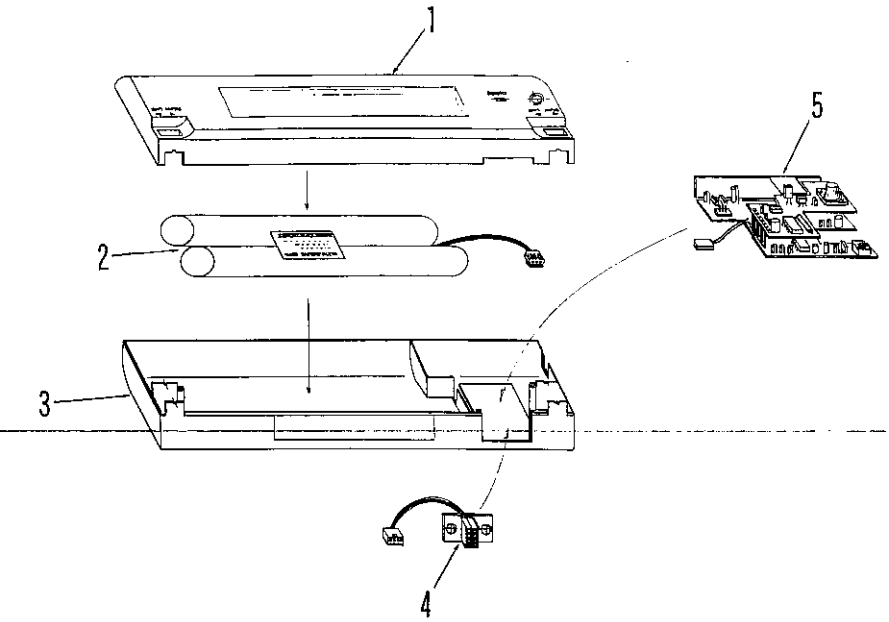
9 CE-621A Packing material&Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKP1038DCZZ	AB	N	D	Vinyl bag
3	SPAKA1057DCZZ	AD	N	D	Packing cushion
4	SPAKA1044DCZZ	AH	N	D	Packing cushion
5	TiNSM1021HCZZ	AD		D	Operation manual(E,F,G,S) [Y]
	TiNSM1024DCZZ	AF	N	D	Operation manual [Except Y]
6	SPAKC1032DCZZ	AG	N	D	Packing case
7	TLABP1023DCZZ	AA	N	D	UPC barcord label [Y]
8	TLABM2121HCZZ	AD		D	Packing label
	TLABM1466ACZZ	AC		D	Packing label [Y]

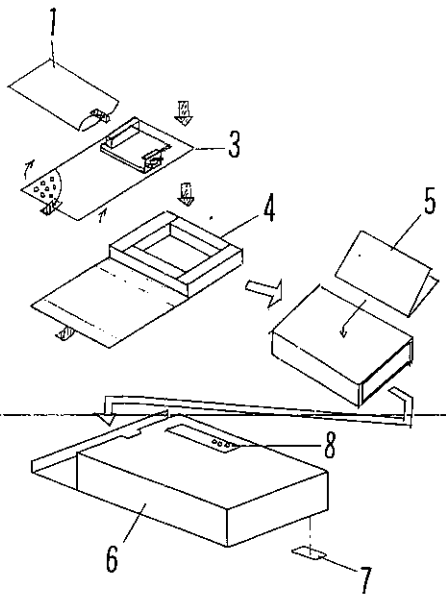
7 CE-621NK Ten key pad



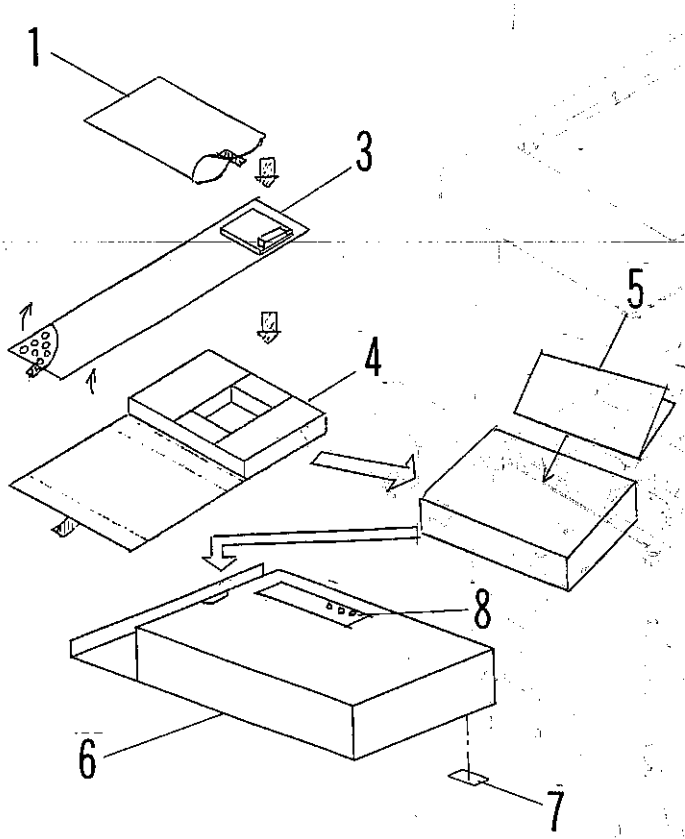
8 CE-621EV Battery pack



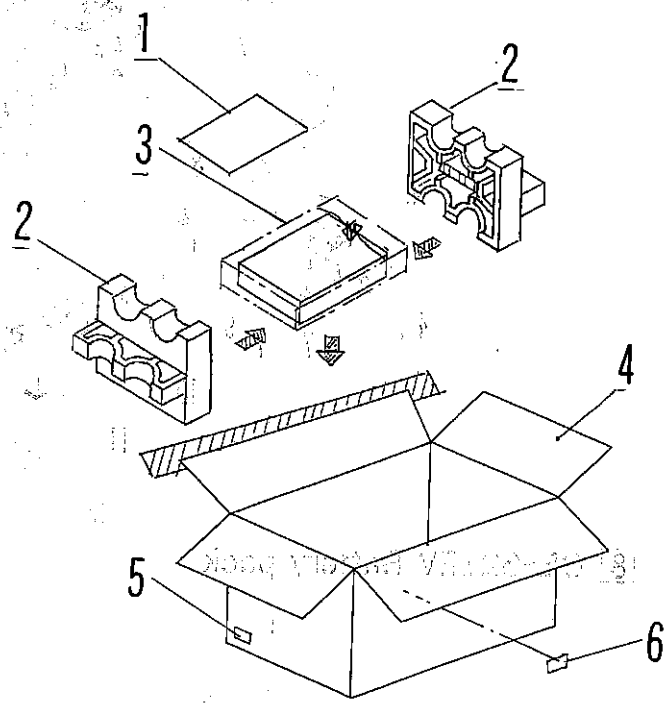
9 CE-621A Packing material &Accessories



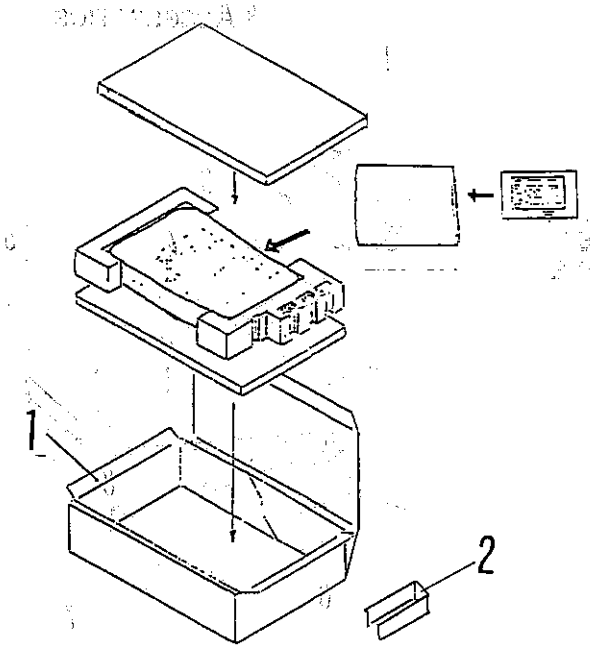
10 CE-621B Packing material&Accessories



11 CE-621F Packing material&Accessories



12 CE-621NK Packing material



10 CE-621B Packing material&Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKP1031DCZZ	AA	N	D	Vinyl bag
3	SPAKA1056DCZZ	AC	N	D	Packing add
4	SPAKA1043DCZZ	AK	N	D	Packing add
5	TiNSM1021HCZZ	AD		D	Operation manual(E,F,G,S)
6	SPAKC1032DCZZ	AG	N	D	Packing case
7	TLABP1022DCZZ	AA	N	D	UPC barcord label [Y]
8	TLABM2121HCZZ	AD		D	Packing label
	TLABM1466ACZZ	AC		C	Packing label [Y]

11 CE-621F Packing material&Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	TiNSM1021HCZZ	AD		D	Operation manual(E,F,G,S) [Except Y,U,G]
	TiNSM1011DCZZ	AF	N	D	Operation manual [Y,U,G]
2	SPAKA1027DCZZ	AV	N	D	Packing add
3	SSAKH3010CCZZ	AA		D	Vinyl bag (0.03t×180×240)
4	SPAKC1025DCZZ	AM	N	D	Packing case
5	TLABP1019DCZZ	AA	N	D	UPC barcord label [Y]
6	TLABM2121HCZZ	AD		D	Packing label
	TLABM1466ACZZ	AC		C	Packing label [Y]

12 CE-621NK Packing material

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	00P5B115A090A	AT	N	D	Packing case
2	00P98AAA0020A	AY	N	D	Accessory

13 PC-6220 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	RR-DZ8101ACZZ	AC		B	Block resistor (100Ω×8) [BR1]
2	RR-DZ4472ACZZ	AB		B	Block resistor (4.7KΩ×4) [BR2]
3	RR-DZ4223ACZZ	AB		B	Block resistor (22KΩ×4) [BR3]
4	RR-DZ4333ACZZ	AB		B	Block resistor (33KΩ×4) [BR4]
5	RR-DZ2333ACZZ	AA		B	Block resistor (33KΩ×2) [BR100]
6	RR-DZ2223ACZZ	AA		B	Block resistor (22KΩ×2) [BR101]
7	RR-DZ8333ACZZ	AC		B	Block resistor (33KΩ×8) [BR102]
8	RR-DZ4333ACZZ	AB		B	Block resistor (33KΩ×4) [BR103]
9	RR-DZ8103ACZZ	AC		B	Block resistor (10KΩ×8) [BR104]
10	RR-DZ4333ACZZ	AB		B	Block resistor (33KΩ×4) [BR105]
11	RR-DZ2223ACZZ	AA		B	Block resistor (22KΩ×2) [BR106]
12	RR-DZ2101ACZZ	AA		B	Block resistor (100Ω×2) [BR107]
13	RR-DZ8101ACZZ	AC		B	Block resistor (100Ω×8) [BR108]
14	RR-DZ4333ACZZ	AB		B	Block resistor (33KΩ×4) [BR109]
15	RR-DZ2223ACZZ	AA		B	Block resistor (22KΩ×2) [BR110]
16	RR-DZ2102ACZZ	AA		B	Block resistor (1KΩ×2) [BR111]
17	RR-DZ8101ACZZ	AC		B	Block resistor (100Ω×8) [BR112]
18	RR-DZ8103ACZZ	AC		B	Block resistor (10KΩ×8) [BR113]
19	RR-DZ2103ACZZ	AA		B	Block resistor (10KΩ×2) [BR114]
20	RR-DZ8101ACZZ	AC		B	Block resistor (100Ω×8) [BR115]
21	RR-DZ8101ACZZ	AC		B	Block resistor (100Ω×8) [BR116]
22	RR-DZ8821ACZZ	AC		B	Block resistor (820Ω×8) [BR117]
23	RR-DZ4101ACZZ	AB		B	Block resistor (100Ω×4) [BR118]
24	RR-DZ8101ACZZ	AC		B	Block resistor (100Ω×8) [BR119]
25	RR-DZ4101ACZZ	AB		B	Block resistor (100Ω×4) [BR120]
26	RR-DZ4102ACZZ	AB		B	Block resistor (1KΩ×4) [BR121]
27	RR-DZ8102ACZZ	AC		B	Block resistor (1KΩ×8) [BR122]
28	RR-DZ8333ACZZ	AC		B	Block resistor (33KΩ×8) [BR123]
29	RTO-R1001ACZZ	AE		C	T.Capacitor (20pF) [C1]
30	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C2]
31	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C3]
32	RC-EZ1003DCZZ	AK		C	Capacitor (0.047F) [C4]
33	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C5]
34	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C6]
35	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C7]
36	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C8]
37	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C9]
38	RC-EZ1001DCZZ	AD		C	Capacitor (16WV 47μF) [C10]

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NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
39	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C100]
40	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C101]
41	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C102]
42	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C103]
43	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C104]
44	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C105]
45	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C106]
46	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C107]
47	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C108]
48	VCKYTV1EF473Z	AA		C	Capacitor (25WV 0.047μF)	[C109]
49	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C110]
50	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C111]
51	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C112]
52	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C113]
53	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C114]
54	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C115]
55	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C116]
56	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C117]
57	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C118]
58	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C119]
59	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10μF)	[C120]
60	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C121]
61	VCCCTV1HH220J	AA		C	Capacitor (50WV 22pF)	[C122]
62	VCCCTV1HH220J	AA		C	Capacitor (50WV 22pF)	[C123]
63	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C125]
64	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C126]
65	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C129]
66	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C130]
67	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C131]
68	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C132]
69	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C133]
70	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C134]
71	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C135]
72	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C136]
73	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C137]
74	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C138]
75	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C139]
76	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C140]
77	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C141]
78	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C142]
79	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C143]
80	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C146]
81	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C147]
82	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C150]
83	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C151]
84	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C152]
85	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C153]
86	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C154]
87	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C155]
88	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C156]
89	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C157]
90	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C158]
91	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C159]
92	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C160]
93	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C161]
94	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C162]
95	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C163]
96	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C164]
97	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C165]
98	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C166]
99	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C167]
100	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C168]
101	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C169]
102	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C170]
103	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C171]
104	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C172]
105	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C173]
106	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C174]
107	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C175]
108	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C176]
109	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C177]
110	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C178]
111	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C179]
112	VCKYTV1EF223Z	AA		C	Capacitor (25WV 0.022μF)	[C180]
113	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C181]
114	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C182]
115	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C183]
116	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C184]
117	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C185]
118	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C186]

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NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
119	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C187]
120	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C188]
121	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C189]
122	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C190]
123	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C191]
124	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C192]
125	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C193]
126	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C194]
127	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C195]
128	VCKYTQ1EF474Z	AB		C	Capacitor (25WV 0.47μF)	[C196]
129	QCNCW1012DCCJ	AW		C	Connector (120pin)	[CN1]
130	QCNCM1148AC6H	AN		C	Connector (68pin)	[CN2]
131	QCNCW1004DC2B	AG		C	Connector (22pin)	[CN3A]
132	QCNCW1004DC2B	AG		C	Connector (22pin)	[CN3B]
133	QCNCM2354SC1D	AF		C	Connector (14pin)	[CN4]
134	QCNCW2370SC0i	AD		C	Connector (9pin)	[CN5]
135	QCNCM1013DC5J	AR		C	Connector (50pin)	[CN6]
136	QCNCM1013DC5J	AR		C	Connector (50pin)	[CN7]
137	QCNCW1014DC2D	AG		C	Connector (24pin)	[CN8]
138	QCNCM1013DC5J	AR		C	Connector (50pin)	[CN9]
139	QCNCW1012DC2F	AT		C	Connector (26pin)	[CN10]
140	QCNCM1022DC0i	AK		C	Connector (9pin)	[CN11]
141	QCNCM2572RC1E	AD		C	Connector (15pin)	[CN12]
142	QCNCM1015DC0B	AB		B	Connector (2pin)	[CN13]
143	QCNCM2572RC0B	AB		B	Connector (2pin)	[CN14]
144	QCNCW2370SC1J	AE		C	Connector (10pin)	[CN15]
145	QCNCM1023DC0C	AB		B	Connector (3pin)	[CN16]
146	VHDMA721///−1	AC		B	Diode (MA721)	[D100]
147	VHD1SS332///−1	AB		B	Diode (1SS332)	[D101]
148	VHDMA721///−1	AC		B	Diode (MA721)	[D102]
149	VHDMA724///−1	AD		B	Diode (MA724)	[DA100]
150	VHDMA724///−1	AD		B	Diode (MA724)	[DA101]
151	VHDMA724///−1	AD		B	Diode (MA724)	[DA102]
152	VHDMA724///−1	AD		B	Diode (MA724)	[DA103]
153	VHDMA724///−1	AD		B	Diode (MA724)	[DA104]
154	VHDMA724///−1	AD		B	Diode (MA724)	[DA105]
155	VHDMA724///−1	AD		B	Diode (MA724)	[DA106]
156	QSW−Z1008DCZZ	AH		B	Dip switch	[Dipsw1]
157	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB100]
158	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB101]
159	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB102]
160	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB103]
161	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB104]
162	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB105]
163	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB106]
164	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB107]
165	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB108]
166	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB109]
167	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB110]
168	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB111]
169	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB112]
170	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB113]
171	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB114]
172	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB115]
173	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB116]
174	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB117]
175	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB118]
176	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB119]
177	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB120]
178	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB121]
179	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB122]
180	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB123]
181	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB124]
182	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB125]
183	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB126]
184	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB127]
185	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB128]
186	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB129]
187	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB130]
188	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB131]
189	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB132]
190	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB133]
191	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB134]
192	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB135]
193	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB136]
194	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB137]
195	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB138]
196	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB139]
197	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB140]
198	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB141]

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NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
199	RCORF1003ACZZ	AB		C	Core (BLM41A01)	[FB142]
200	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC1]
201	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC2]
202	VHiSC146818P1	AW		B	RTC(Real time clock) (SC146818P1)	[IC3]
203	VHiTC74AC10FN	AD		B	IC (TC74AC10)	[IC4]
204	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC5]
205	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC6]
206	VHi3JD2CA1A-1	AU		B	IC (3JD2CA1A)	[IC7]
207	VHi80C52N//-1	AZ		B	IC (80C52N)	[IC8]
208	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC9]
209	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC10]
210	VHiLZ95H22/-1	AZ		B	IC (LZ95H22)	[IC11]
211	VHi80C286/-12	BP		B	IC (80C286)	[IC12]
212	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC13]
213	VHiKM41C464-1	AQ		B	IC (KM41C464)	[IC14]
214	VHiTC74AC374F	AK		B	IC (TC74AC374)	[IC15]
215	VHiTC7S04FTPR	AC		B	IC (TC7S04FTPR)	[IC16]
216	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC17]
217	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC18]
218	VHiSN74HC238S	AF		B	IC (SN74HC238)	[IC19]
219	VHi74HCT373MF	AH		B	IC (74HCT373MF)	[IC20]
220	VHi80C42G//-1	AT		B	SUB CPU (80C42G)	[IC21]
221	VHiSC9889B/-1	BP		B	IC (SC9889B)	[IC22]
222	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC23]
223	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC24]
224	VHi74AC11238N	AM		B	IC (74AC11238)	[IC25]
225	VHiSN74HC27NS	AC		B	IC (SN74HC27)	[IC26]
226	VHiSN74HC02NS	AC		B	IC (SN74HC02)	[IC27]
227	VHi82C455R4-1	BY		B	IC (82C455R4)	[IC28]
228	VHiSN74HC04NS	AC		B	IC (SN74HC04)	[IC29]
229	QSOCZ1002DCZZ	AK	N	C	IC socket	[IC30]
230	VHiSC9871//-1	BC		B	IC (SC9871)	[IC31]
231	VHiSN74HCT245	AF		B	IC (SC74HCT245)	[IC32]
232	RCNVD1001DCZZ	AT	N	B	Converter (NNSA0505CA)	[IC33]
233	VHiSN74HC08DB	AC		B	IC (SN74HC08)	[IC34]
234	VHiSN74HC08DB	AC		B	IC (SN74HC08)	[IC35]
235	VHiSN74HC08DB	AC		B	IC (SN74HC08)	[IC36]
236	VHiTC7S32FTPR	AC		B	IC (TC7S32FTPR)	[IC100]
237	VHiTC7S08FTPR	AC		B	IC (TC7S08FTPR)	[IC101]
238	VHiSN74HC27NS	AC		B	IC (SN74HC27)	[IC102]
239	VHiSN74HC02NS	AC		B	IC (SN74HC02)	[IC103]
240	VHiALS38ANS//	AE		B	IC (ALS38NS)	[IC104]
241	VHiTC74AC174F	AG		B	IC (TC74AC174)	[IC105]
242	VHiTC74AC541F	AL		B	IC (TC74AC541)	[IC106]
243	VHiSN74HC30NS	AC		B	IC (SN74HC30)	[IC107]
244	VHiSN74HCT244	AF		B	IC (SN74HCT244)	[IC108]
245	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC109]
246	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC110]
247	VHiSN74HCT245	AF		B	IC (SN74HCT245)	[IC111]
248	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC112]
249	VHi518128AFL8	BC		B	IC (518128AFL8)	[IC113]
250	VHiSN74HCT244	AF		B	IC (SN74HCT244)	[IC115]
251	VHiUPD4714GT1	AW		B	IC (UPD4714)	[IC116]
252	VHiTC7S32FTPR	AC		B	IC (TC7S32FTPR)	[IC117]
253	RCiLZ1003DCZZ	AC		B	Coil	[L100]
254	VHPGL3ED8//-1	AC		B	Photo transistor (GL3ED8)	[LED1]
255	VHPGL3HD44/-1	AB		B	Photo transistor (GL3HD44)	[LED2]
256	VHPGL3EG44/-1	AA		B	Photo transistor (GL3EG44)	[LED3]
257	VHPGL3EG44/-1	AA		B	Photo transistor (GL3EG44)	[LED4]
258	VHPGL3EG44/-1	AA		B	Photo transistor (GL3EG44)	[LED5]
259	VHPGL3EG44/-1	AA		B	Photo transistor (GL3EG44)	[LED6]
260	VHPGL3EG44/-1	AA		B	Photo transistor (GL3EG44)	[LED7]
261	VHPGL3EG44/-1	AA		B	Photo transistor (GL3EG44)	[LED8]
262	VS2SC2021-RSC	AF		B	Transistor (2SC2021-RSC)	[Q1]
263	VSDTC114YK/-1	AC		B	Transistor (DTC114YK)	[Q100]
264	VSDTA114YK/-1	AC		B	Transistor (DTA114YK)	[Q101]
265	VSDTA114YK/-1	AC		B	Transistor (DTA114YK)	[Q103]
266	VSDTA144EK/-1	AC		B	Transistor (DTA144EK)	[Q104]
267	VSDTC114YK/-1	AC		B	Transistor (DTC114YK)	[Q105]
268	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R100]
269	VRS-TS2AD565J	AA		C	Resistor (1/10W 5.6MΩ ±5%)	[R101]
270	VRS-TS2AD154J	AA		C	Resistor (1/10W 150KΩ ±5%)	[R102]
271	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R103]
272	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R104]
273	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R105]
274	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R106]
275	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R107]
276	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R108]
277	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R109]
278	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R110]

13 PC-6220 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
279	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R111]
280	VRS-TS2AD332J	AA		C	Resistor (1/10W 3.3KΩ ±5%)	[R112]
281	VRS-TS2AD332J	AA		C	Resistor (1/10W 3.3KΩ ±5%)	[R113]
282	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R114]
283	RCiLZ2087SCZZ	AB		C	Coil (BLM41A04)	[R115]
284	RCiLZ2087SCZZ	AB		C	Coil (BLM41A04)	[R116]
285	VRS-TS2AD470J	AA		C	Resistor (1/10W 47Ω ±5%)	[R117]
286	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R118]
287	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R119]
288	VRS-TS2AD470J	AA		C	Resistor (1/10W 47Ω ±5%)	[R120]
289	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R121]
290	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R122]
291	VRS-TS2AD331J	AA		C	Resistor (1/10W 330Ω ±5%)	[R123]
292	VRS-TS2AD562J	AA		C	Resistor (1/10W 5.6KΩ ±5%)	[R124]
293	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R125]
294	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%)	[R126]
295	VRS-TS2AD273J	AA		C	Resistor (1/10W 27KΩ ±5%)	[R127]
296	VRS-TS2AD152J	AA		C	Resistor (1/10W 1.5KΩ ±5%)	[R128]
297	VRS-TS2AD332J	AA		C	Resistor (1/10W 3.3KΩ ±5%)	[R129]
298	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%)	[R131]
299	VRS-TS2AD153J	AA		C	Resistor (1/10W 15KΩ ±5%)	[R132]
300	VRS-TS2AD473J	AA		C	Resistor (1/10W 47KΩ ±5%)	[R134]
301	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%)	[R135]
302	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R136]
303	QSW-S1005DCZZ	AD	N	B	Slide switch	[SW1]
304	QTANZ6632RCZZ	AA	N	C	Pin	[TPGND]
305	QTANZ6632RCZZ	AA	N	C	Pin	[TPTP]
306	RCRSP1003CCZZ	AT		B	Crystal (32KHz)	[X1]
307	RCRSZ1001DCZZ	AP	N	B	Crystal (14.318MHz)	[X2]
308	RCRSZ1002DCZZ	AP	N	B	Crystal (23.9616MHz)	[X3]
309	RCRSZ1004DCZZ	AP	N	B	Crystal (28.322MHz)	[X4]
310	RCRSZ1003DCZZ	AP	N	B	Crystal (25.175MHz)	[X5]
311	PSHEZ1037ACZZ	AA		C	Sheet	
312	LHLDZ1001DCZZ	AD		C	LED holder	
313	XBBSD20P06000	AA		C	Screw (2×6)	
314	VRD-HT2EY102J	AA		C	Resistor (1/4W 1KΩ ±5%)	
	(Unit)					
901	CPWBY1007DC01	**	N	E	Main PWB unit	

14 PC-6220 VR PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C]
2	QCNW-1009DCZZ	AF		C	VR cable	[CNA]
3	QCNW-1010DCZZ	AD		C	INV cable	[CNB]
4	VRD-RC2EY104G	AA		C	Resistor (1/4W 100KΩ ±2%)	[R1]
5	VRD-RC2EY183G	AA		C	Resistor (1/4W 18KΩ ±2%)	[R2]
6	QSW-S1444CCZZ	AD		B	Slide switch	[SW]
7	VHSDTND104J4M	AC		B	Thyristor	[TH]
8	RVR-B5400QCZZ	AE		B	Variable resistor (50KΩ)	[VR1]
9	RVR-B2300QCZZ	AE		B	Variable resistor (2KΩ)	[VR2]
10	VHERD30EL1/-1	AA		B	Zener diode (RD30EL1)	[ZD]
	(Unit)					
901	CPWBF1019DC01	AZ	N	E	VR PWB unit	

15 PC-6220 Power suply unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	0BR2717CN3///	AY	N	C	Wire harness	[CN3]
2	0BR2717CN1///	AT	N	C	Wire harness	[CN1]
3	0BR2717J101//	AK	N	C	Harness	[J101]
4	0BR2717S1////	AT	N	B	Switch	[S1]
5	0BR2717P1////	AK	N	C	Jack	[P1]
6	0BR2717ALPWB/	BS	N	E	PWB ass'y	
7	0BR2717GLPWB/	BP	N	E	PWB ass'y	
	(Unit)					
901	RDENC1002DCZZ	BV	N	E	Power supply unit	

16 PC-6220 ROM board unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C300]
2	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C400]
3	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C401]
4	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C402]
5	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C403]
6	QCNCW1013DC5J	AR		C	Connector (50pin)	[CNR1]
7	VHiLH5380MY-1	BB		B	IC (LH5380MY)	[IC300]
8	VHiC102FDAB1C	BF	N	B	ROM (C102FDAB1C)	[IC400] (Except G,H,Q)
9	VHiC102FDAC1C	BF	N	B	ROM (C102FDAC1C)	[IC400] (G,H,Q)
	(Unit)					
901	DUNTK1090DC01	BG	N	E	ROM board unit	

17 CE-621A CRT I/F PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	VCCCTS1HH331J	AA		C	Capacitor (50WV 330PF)	[C1]
2	VCCCTS1HH331J	AA		C	Capacitor (50WV 330PF)	[C2]
3	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10μF)	[C3]
4	VCKYTV1EF104Z	AA		C	Capacitor (10WV 0.01μF)	[C4]
5	VCKYTV1EB103K	AA		C	Capacitor (25WV 0.01μF)	[C5]
6	VCKYTV1EF104Z	AA		C	Capacitor (10WV 0.01μF)	[C6]
7	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C7]
8	RC-SZ1001DCZZ	AD		C	Capacitor (16WV 33μF)	[C8]
9	QCNCW1148AC6H	AN		C	Connector (68pin)	[CN1]
10	QCNCW1152AC1E	AQ		C	D-SUB female (15pin)	[CN2]
11	VHDDA204K//-1	AC		B	Diode (DA204K)	[D1]
12	RCiLZ2087SCZZ	AB		C	Coil	[FB1]
13	RCiLZ2087SCZZ	AB		C	Coil	[FB2]
14	RCiLZ2087SCZZ	AB		C	Coil	[FB4]
15	RCiLZ2087SCZZ	AB		C	Coil	[FB6]
16	RFiLN1005DCZZ	AR	N	C	Noise filter (D-45C)	[FL1]
17	VHiSN74HC32NS	AK		B	IC (SN74HC32)	[IC1]
18	VHiAM81EC176/	BA		B	IC (AM81EC176)	[IC2]
19	VHiLM334Z//-1	AL		B	IC (LM334Z)	[IC3]
20	RCiLZ1003DCZZ	AC	N	C	Coil (47μF)	[L1]
21	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R1]
22	VRS-TS2AD563J	AA		C	Resistor (1/10W 56KΩ ±5%)	[R2]
23	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R3]
24	VRS-TS2AD750J	AA		C	Resistor (1/10W 75Ω ±5%)	[R4]
25	VRS-TS2AD750J	AA		C	Resistor (1/10W 75Ω ±5%)	[R5]
26	VRS-TS2AD750J	AA		C	Resistor (1/10W 75Ω ±5%)	[R6]
27	VRS-TS2AD563J	AA		C	Resistor (1/10W 56KΩ ±5%)	[R7]
28	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R8]
29	VRS-TS2AD150J	AA		C	Resistor (1/10W 15Ω ±5%)	[R9]
30	VRS-TS2AD151J	AA		C	Resistor (1/10W 150Ω ±5%)	[R10]
31	LANGT1016DCZZ	AF	N	C	Connector angle	
32	LX-BZ1008DCZZ	AC		C	Screw	
33	LX-BZ1141CCZZ	AA		C	Screw	
34	XBPSD30P06000	AA		C	Screw (3×6)	
35	XRESJ25-04000	AA		C	E type ring (2.5mm)	
36	RC-K1E104SCZZ	AA		C	Capacitor (25WV 0.1μF)	
37	VRD-HT2EY332J	AA		C	Resistor (1/4W 3.3KΩ ±5%)	
38	MSPRP1006DCZZ	AQ	N	C	Connector earth spring	

18 CE-621B RAM PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C1]
2	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C2]
3	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C3]
4	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C4]
5	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C5]
6	VCSAPJ1AE106M	AE		C	Capacitor (10WV 10μF)	[C6]
7	QCNCW1013DC5J	AR		C	Connector (50pin)	[CN1]
8	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC1]
9	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC2]
10	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC3]
11	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC4]
12	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC5]
13	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC6]
14	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC7]
15	VHi518128AFL8	BC	N	B	IC (518128AFL8)	[IC8]

19 CE-621F FDD I/F PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	RR-DZ4102ACZZ	AB		B	Black resistor (1KΩ×4)	[BR1]
2	RR-DZ4102ACZZ	AB		B	Black resistor (1KΩ×4)	[BR2]
3	VCKYTV1HB221K	AA		C	Capacitor (50WV 220PF)	[C1]
4	VCKYTV1HB221K	AA		C	Capacitor (50WV 220PF)	[C2]
5	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C3]
6	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C6]
7	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C7]
8	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C8]
9	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C9]
10	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C10]
11	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C11]
12	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C12]
13	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C13]
14	VCSAPJ1CE336M	AF		C	Capacitor (16WV 33μF)	[C14]
15	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C15]
16	VCKYTV1HB103K	AB		C	Capacitor (50WV 0.01μF)	[C16]
17	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C17]
18	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C18]
19	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C19]
20	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C20]
21	VCCCTV1HH470J	AA		C	Capacitor (50WV 47ρF)	[C21]
22	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C22]
23	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C23]
24	VCCCTV1HH470J	AA		C	Capacitor (50WV 47ρF)	[C24]
25	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C25]
26	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C26]
27	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C27]
28	VCKYTV1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C28]
29	VCSAPJ1CE336M	AF		C	Capacitor (16WV 33μF)	[C29]
30	VCSAPJ1CE336M	AF		C	Capacitor (16WV 33μF)	[C30]
31	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C31]
32	VCCSPU1HL101J	AA		C	Capacitor (50WV 100ρF)	[C32]
33	VCCSPU1HL101J	AA		C	Capacitor (50WV 100ρF)	[C33]
34	QCNCM1012DCCJ	BA		C	Connector (120pin)	[CN1]
35	QCNCM2346SC2F	AH		C	Connector (26pin)	[CN2]
36	QCNCW1115AC2E	AK		C	D-SUB female (25pin)	[CN3]
37	QCNCW5054SC0F	AG		C	Mini DIN connector (6pin)	[CN4]
38	VHiSN74LS07-1	AK		B	IC (SN74LS07)	[IC1]
39	VHiSN74LS14-1	AM		B	IC (SN74LS14F)	[IC2]
40	VHiSN74LS07-1	AK		B	IC (SN74LS07)	[IC3]
41	VHiTC8566AF-1	AZ		B	IC (TC8566AF)	[IC4]
42	VHiTC74HC74FN	AF		B	IC (TC74HC74F)	[IC5]
43	VHiTC74HC04FN	AD		B	IC (TC74HC04FN)	[IC6]
44	VHiTC74HC74FN	AF		B	IC (TC74HC74F)	[IC7]
45	VHiTC74HC10FN	AD		B	IC (TC74HC10FN)	[IC8]
46	VHiTC74HC157F	AE		B	IC (TC74HC157F)	[IC9]
47	VHiTC74HC32AF	AE		B	IC (TC74HC32AF)	[IC10]
48	VHiTC74AC32FN	AD		B	IC (TC74AC32FN)	[IC11]
49	VHiTC74HC138F	AL		B	IC (TC74HC138F)	[IC12]
50	VHiTC74AC11FN	AD		B	IC (TC74AC11FN)	[IC13]
51	VHiTC74AC11FN	AD		B	IC (TC74AC11FN)	[IC14]
52	VHiTC74AC02FN	AD		B	IC (TC74AC02FN)	[IC15]
53	VHiTC74AC74FN	AE		B	IC (TC74AC74FN)	[IC16]
54	VHiTC74HC02FN	AD		B	Ic (TC74HC02FN)	[IC17]
55	VHiTC74HC74FN	AF		B	IC (TC74HC74)	[IC18]
56	VHiTC74HC125F	AH		B	IC (TC74HC125F)	[IC19]
57	VHiTC74HC04FN	AD		B	IC (TC74HC04FN)	[IC20]
58	VHiTC74HC04FN	AD		B	IC (TC74HC04FN)	[IC21]
59	VHiTC74HC32AF	AE		B	IC (TC74HC32AF)	[IC22]
60	VHiTC74AC11FN	AD		B	IC (TC74AC11FN)	[IC23]
61	VHiTC74AC20FN	AD		B	IC (TC74AC20FN)	[IC24]
62	VHiSN74LS06-1	AE		B	IC (SN74LS06)	[IC25]
63	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L1]
64	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L4]
65	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L5]
66	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L14]
67	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L15]
68	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L16]
69	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L17]
70	RCŌRF1003ACZZ	AB		C	Core (BLM41)	[L18]
71	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R1]
72	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%)	[R2]
73	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%)	[R3]
74	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R4]
75	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R5]
76	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R6]
77	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R7]
78	VRS-TS2AD683J	AA		C	Resistor (1/10W 68KΩ ±5%)	[R8]
79	VRS-TS2AD153J	AA		C	Resistor (1/10W 15KΩ ±5%)	[R9]
80	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R10]

19 CE-621F FDD I/F PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
81	RCRSZ1006DCZZ	AP	N	B	Crystal (19.2MHz)	[X1]
82	RCRSZ1053ACZZ	AP		B	Crystal (16MHz)	[X2]
	(Unit)					
901	CPWBX1016DC01		N	E	FDD I/F PWB unit	

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PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
[C]					
CCADZ1003DC01	3- 2	AM	N	D	
CCNW-2814SC01	3- 15	AX		B	
CPWBF1019DC01	4- 29	AZ	N	E	
//	14- 901	AZ	N	E	
CPWBX1016DC01	5- 4		N	E	
//	19- 901		N	E	
CPWBY1007DC01	1- 15	**	N	E	
//	13- 901	**	N	E	
[D]					
DUNT-1020DCZZ	1- 1	BG	N	E	
DUNT-1021DCZZ	1- 1	BH	N	E	
DUNT-1022DCZZ	1- 1	BH	N	E	
DUNT-1033DCZZ	4- 18	AW		E	
DUNT-1038DCZZ	2- 11	CQ	N	E	
DUNT-1060DCZZ	3- 9	BD	N	E	
DUNTK1036DCZZ	4- 28	BA		E	
DUNTK1037DCZZ	1- 11	**	N	E	
DUNTK1062DCZZ	5- 14	BW	N	E	
//	6- 901	BW	N	E	
DUNTK1090DC01	1- 45	BG	N	E	
//	16- 901	BG	N	E	
DUNTM1034DCZZ	4- 2	BC		E	
[G]					
GCABA1003DCZZ	1- 28	BB	N	D	
GCABA1012DCZZ	5- 16	AX	N	D	
GCABB1004DCZZ	2- 7	BB	N	D	
GCABB1013DCZZ	5- 22	AY	N	D	
GCABC1009DCZZ	4- 1	BB		D	
GCABD1011DCZZ	4- 20	AL		D	
GCOVA1008DCZZ	2- 10	AP	N	D	
GCOVH1002DCZZ	1- 40	AD	N	D	
GCOVH1003DCZZ	1- 44	AE	N	C	
GCOVH1004DCZZ	1- 27	AD	N	C	
GCOVH1005DCZZ	1- 33	AD	N	C	
GCOVH1006DCZZ	1- 39	AN	N	D	
GLEGG1002DCZZ	1- 35	AA	N	D	
//	5- 20	AA		D	
[J]					
JBTN-1001DCZZ	4- 16	AB		C	
JBTN-1002DCZZ	4- 25	AB		C	
JBTN-1003DCZZ	4- 35	AB		C	
JHNDP2008SCZZ	3- 7	AB		C	
[L]					
LANGQ1012DCZZ	5- 7	AE	N	C	
LANGQ1013DCZZ	5- 2	AE	N	C	
LANGT1001DCZZ	4- 9	AF		C	
LANGT1002DCZZ	4- 6	AE		C	
LANGT1003DCZZ	4- 33	AD		C	
LANGT1004DCZZ	4- 34	AD		C	
LANGT1005DCZZ	1- 25	AF	N	C	
LANGT1006DCZZ	1- 24	AF	N	C	
LANGT1007DCZZ	1- 12	AE	N	C	
LANGT1008DCZZ	1- 22	AH	N	C	
LANGT1009DCZZ	1- 6	AH	N	C	
LANGT1010DCZZ	1- 41	AE	N	C	
LANGT1014DCZZ	5- 15	AF	N	C	
LANGT1015DCZZ	5- 13	AF	N	C	
LANGT1016DCZZ	17- 31	AF	N	C	
LHLDW5023NCZZ	4- 21	AB		C	
LHLDZ1001DCZZ	13- 312	AD		C	
LPLTP1004DCZZ	3- 10	AF	N	C	
LSTPF1001DCZZ	4- 17	AD		C	
LX-BZ1003DCZZ	4- 27	AA		C	
LX-BZ1004DCZZ	4- 37	AA		C	
LX-BZ1007DCZZ	5- 21	AG		C	
LX-BZ1008DCZZ	17- 32	AC		C	
LX-BZ1011DCZZ	5- 10	AB		C	
LX-BZ1018ECZZ	1- 2	AA		C	
LX-BZ1141CCZZ	1- 23	AA		C	
//	5- 9	AA		C	
//	17- 33	AA		C	
LX-BZ1147CCZZ	1- 14	AA		C	
//	2- 1	AA		C	
LX-BZ1155CCZZ	1- 7	AA		C	
LX-BZ1187CCZZ	1- 5	AA		C	
LX-BZ1199CCZZ	1- 42	AA		C	
[M]					
MSPRC1001DCZZ	4- 15	AA		C	
MSPRC1005DCZZ	5- 24	AA	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
MSPRP1006DCZZ	17- 38	AQ	N	C	
[P]					
PCAPH1016ACZZ	5- 8	AD		C	
PCAPZ1001DCZZ	4- 24	AB		C	
PCUSS1007DCZZ	4- 8	AD		C	
PCUSS1008DCZZ	4- 12	AD		C	
PDMP-1001DCZZ	2- 5	AL	N	C	
PGUMM1562CCZA	5- 11	AD		C	
PHOG-1023CCZZ	3- 15	AB		C	
PSHEZ1005DCZZ	4- 30	AZ		C	
PSHEZ1007DCZZ	4- 36	AA		C	
PSHEZ1008DCZZ	4- 19	AE		C	
PSHEZ1009DCZZ	1- 32	AF	N	C	
PSHEZ1010DCZZ	1- 31	AA	N	C	
PSHEZ1012DCZZ	5- 23	AF	N	C	
PSHEZ1037ACZZ	13- 311	AA		C	
PSLDM1001DCZZ	1- 4	AF	N	C	
PTPEH1323CCZZ	4- 22	AA		C	
PTPEZ1001DCZZ	4- 39	AD		D	
PTPEZ1002DCZZ	4- 4	AA		D	
PZETZ1001DCZZ	4- 10	AC		C	
PZETZ1002DCZZ	4- 7	AC		C	
PZETZ1004DCZZ	2- 9	AB	N	C	
[Q]					
QACCB7521QCZZ	3- 15	AS		B	
QACCB7621QCZZ	3- 15	AN		B	
QACCD7611QCZZ	3- 15	AT		B	
QACCF7622QCZZ	3- 15	AX	N	B	
QACCL7620QCZZ	3- 15	AW		B	
QACCV6620QCZZ	3- 15	AV		B	
QCNCM1012DCCJ	19- 34	BA		C	
QCNCM1013DC5J	13- 135	AR		C	
//	13- 136	AR		C	
//	13- 138	AR		C	
QCNCM1015DC0B	13- 142	AB		B	
QCNCM1022DC0I	13- 140	AK		C	
QCNCM1023DC0C	13- 145	AB		B	
QCNCM1148AC6H	13- 130	AN		C	
QCNCM2346SC2F	19- 35	AH		C	
QCNCM2354SC1D	13- 133	AF		C	
QCNCM2572RC0B	13- 143	AB		B	
QCNCM2572RC1E	13- 141	AD		C	
QCNCW1004DC2B	13- 131	AG		C	
//	13- 132	AG		C	
QCNCW1012DCCJ	13- 129	AW		C	
QCNCW1012DC2F	13- 139	AT		C	
QCNCW1013DC5J	16- 6	AR		C	
//	18- 7	AR		C	
QCNCW1014DC2D	13- 137	AG		C	
QCNCW1115AC2E	19- 36	AK		C	
QCNCW1148AC6H	17- 9	AN		C	
QCNCW1152AC1E	17- 10	AQ		C	
QCNCW2370SC0I	13- 134	AD		C	
QCNCW2370SC1J	13- 144	AE		C	
QCNCW5054SC0F	19- 37	AG		C	
QCNW-1009DCZZ	4- 14	AF		C	
//	14- 2	AF		C	
QCNW-1010DCZZ	4- 38	AD		C	
//	14- 3	AD		C	
QCNW-1011DCZZ	1- 3	AW		C	
//	4- 13	AW		C	
QCNW-1012DCZZ	4- 26	AD		C	
QCNW-1013DCZZ	1- 43	AV	N	C	
QCNW-1014DCZZ	2- 3	AD	N	C	
QCNW-1016DCZZ	3- 13	BB	N	C	
QCNW-1017DCZZ	5- 6	AS	N	C	
QCNW-1018DCZZ	1- 13	AX	N	C	
QPLGA0010UCZZ	3- 15	AM		C	
QPLGA0018WRE0	3- 15	AN		C	
QPWBM1031DCZZ	1- 9	AK	N	C	
QSOCZ1002DCZZ	13- 229	AK	N	C	
QSW-P1004DCZZ	2- 2	AE	N	B	
QSW-S1005DCZZ	13- 303	AD	N	B	
QSW-S1444CCZZ	14- 6	AD		B	
QSW-Z1008DCZZ	13- 156	AH		B	
QTANZ6632RCZZ	13- 304	AA	N	C	
//	13- 305	AA	N	C	
[R]					
RADPA1003DCZZ	3- 11	BQ	N	B	
RADPA1004DCZZ	3- 11	BS	N	B	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
RALMB1002DCZZ	1- 30	AM	N	B
RC-EZ1001DCZZ	13- 30	AD		C
〃	13- 31	AD		C
〃	13- 33	AD		C
〃	13- 34	AD		C
〃	13- 35	AD		C
〃	13- 36	AD		C
〃	13- 37	AD		C
〃	13- 38	AD		C
RC-EZ1003DCZZ	13- 32	AK		C
RC-KIE104SCZZ	17- 36	AA		C
RC-SZ1001DCZZ	13- 108	AD		C
〃	13- 109	AD		C
〃	13- 110	AD		C
〃	13- 111	AD		C
〃	14- 1	AD		C
〃	16- 1	AD		C
〃	17- 7	AD		C
〃	17- 8	AD		C
RCiLZ1003DCZZ	13- 253	AC		B
〃	17- 20	AC	N	C
RCiLZ2087SCZZ	13- 283	AB		C
〃	13- 284	AB		C
〃	17- 12	AB		C
〃	17- 13	AB		C
〃	17- 14	AB		C
〃	17- 15	AB		C
RCNVD1001DCZZ	13- 232	AT	N	B
RCŌRF1003ACZZ	13- 157	AB		C
〃	13- 158	AB		C
〃	13- 159	AB		C
〃	13- 160	AB		C
〃	13- 161	AB		C
〃	13- 162	AB		C
〃	13- 163	AB		C
〃	13- 164	AB		C
〃	13- 165	AB		C
〃	13- 166	AB		C
〃	13- 167	AB		C
〃	13- 168	AB		C
〃	13- 169	AB		C
〃	13- 170	AB		C
〃	13- 171	AB		C
〃	13- 172	AB		C
〃	13- 173	AB		C
〃	13- 174	AB		C
〃	13- 175	AB		C
〃	13- 176	AB		C
〃	13- 177	AB		C
〃	13- 178	AB		C
〃	13- 179	AB		C
〃	13- 180	AB		C
〃	13- 181	AB		C
〃	13- 182	AB		C
〃	13- 183	AB		C
〃	13- 184	AB		C
〃	13- 185	AB		C
〃	13- 186	AB		C
〃	13- 187	AB		C
〃	13- 188	AB		C
〃	13- 189	AB		C
〃	13- 190	AB		C
〃	13- 191	AB		C
〃	13- 192	AB		C
〃	13- 193	AB		C
〃	13- 194	AB		C
〃	13- 195	AB		C
〃	13- 196	AB		C
〃	13- 197	AB		C
〃	13- 198	AB		C
〃	13- 199	AB		C
〃	19- 63	AB		C
〃	19- 64	AB		C
〃	19- 65	AB		C
〃	19- 66	AB		C
〃	19- 67	AB		C
〃	19- 68	AB		C
〃	19- 69	AB		C
〃	19- 70	AB		C
RCRSP1003CCZZ	13- 306	AT		B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
RCRSZ1001DCZZ	13- 307	AP	N	B
RCRSZ1002DCZZ	13- 308	AP	N	B
RCRSZ1003DCZZ	13- 310	AP	N	B
RCRSZ1004DCZZ	13- 309	AP	N	B
RCRSZ1006DCZZ	19- 81	AP	N	B
RCRSZ1053ACZZ	19- 82	AP		B
RDENC1002DCZZ	1- 8	BV	N	E
〃	15- 901	BV	N	E
RFiLN1005DCZZ	17- 16	AR	N	C
RR-DZ2101ACZZ	13- 12	AA		B
RR-DZ2102ACZZ	13- 16	AA		B
RR-DZ2103ACZZ	13- 19	AA		B
RR-DZ2223ACZZ	13- 6	AA		B
〃	13- 11	AA		B
〃	13- 15	AA		B
RR-DZ2333ACZZ	13- 5	AA		B
RR-DZ4101ACZZ	13- 23	AB		B
〃	13- 25	AB		B
RR-DZ4102ACZZ	13- 26	AB		B
〃	19- 1	AB		B
〃	19- 2	AB		B
RR-DZ4223ACZZ	13- 3	AB		B
RR-DZ4333ACZZ	13- 4	AB		B
〃	13- 8	AB		B
〃	13- 10	AB		B
〃	13- 14	AB		B
RR-DZ4472ACZZ	13- 2	AB		B
RR-DZ8101ACZZ	13- 1	AC		B
〃	13- 13	AC		B
〃	13- 17	AC		B
〃	13- 20	AC		B
〃	13- 21	AC		B
〃	13- 24	AC		B
RR-DZ8102ACZZ	13- 27	AC		B
RR-DZ8103ACZZ	13- 9	AC		B
〃	13- 18	AC		B
RR-DZ8333ACZZ	13- 7	AC		B
〃	13- 28	AC		B
RR-DZ8821ACZZ	13- 22	AC		B
RTŌ-R1001ACZZ	13- 29	AE		C
RVR-B2300QCZZ	14- 9	AE		B
RVR-B5400QCZZ	14- 8	AE		B
【S】				
SPAKA1011DCZZ	3- 3	AM	N	D
SPAKA1012DCZZ	3- 14	AG	N	D
SPAKA1013DCZZ	3- 20	AE	N	D
SPAKA1014DCZZ	3- 12	AC	N	D
SPAKA1027DCZZ	11- 2	AV	N	D
SPAKA1043DCZZ	10- 4	AK	N	D
SPAKA1044DCZZ	9- 4	AH	N	D
SPAKA1056DCZZ	10- 3	AC	N	D
SPAKA1057DCZZ	9- 3	AD	N	D
SPAKA1058DCZZ	3- 1	AF	N	D
SPAKA1059DCZZ	3- 5	AG		D
SPAKA1060DCZZ	3- 21	AE	N	D
SPAKA5416SCZZ	3- 6	AB		D
SPAKC1015DCZZ	3- 8	AU	N	D
SPAKC1025DCZZ	11- 4	AM	N	D
SPAKC1032DCZZ	9- 6	AG	N	D
〃	10- 6	AG	N	D
SPAKP1031DCZZ	10- 1	AA	N	D
SPAKP1038DCZZ	9- 1	AB	N	D
SSAKA0330QCZZ	3- 18	AA		D
SSAKA3001CCZZ	3- 17	AA		D
SSAKH1028CCZZ	3- 4	AA		D
SSAKH3010CCZZ	11- 3	AA		D
SSAKH3015CCZZ	3- 22	AA		D
【T】				
TCADZ1075ACZZ	3- 2	AF		D
TCAUS1001DCZZ	1- 46	AC	N	D
TCAUS1054CCZZ	3- 24	AB		C
TGANE2002HCZZ	3- 2	AN		C
TiNSE1005DCZZ	3- 2	AX	N	D
TiNSE1006DCZZ	3- 2	AX	N	D
TiNSE1007DCZZ	3- 2	AX	N	D
TiNSE1008DCZZ	3- 2	AU	N	D
TiNSM1011DCZZ	11- 1	AF	N	D
TiNSM1021HCZZ	9- 5	AD		D
〃	10- 5	AD		D
〃	11- 1	AD		D

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
TiNSM1024DCZZ	9- 5	AF	N	D	
TLABB1381ACZZ	3- 25	AC		D	
TLABG1025DCZZ	5- 19	AC	N	D	
TLABH1065DCZZ	4- 3	AA	N	D	
TLABM1004DCZZ	1- 49	AF	N	D	
TLABM1466ACZZ	9- 8	AC		D	
〃	10- 8	AC		C	
〃	11- 6	AC		C	
TLABM2121HCZZ	9- 8	AD		D	
〃	10- 8	AD		D	
〃	11- 6	AD		D	
TLABM2270SCZZ	3- 23	AB		D	
TLABP1019DCZZ	11- 5	AA	N	D	
TLABP1022DCZZ	10- 7	AA	N	D	
TLABP1023DCZZ	9- 7	AA	N	D	
TLABS1009DCZZ	1- 47	AC	N	D	
TLABS1026DCZZ	5- 19	AC	N	D	
TLABZ1546ACSA	1- 48	AC		D	
〔U〕					
UBATN1002DCZZ	1- 38	BU		B	
〃	3- 19	BU		B	
UBNDA1008CCZZ	3- 16	AA		C	
〔V〕					
VCCCTS1HH331J	17- 1	AA		C	
〃	17- 2	AA		C	
VCCCTV1HH101J	13- 87	AA		C	
〃	13- 88	AA		C	
〃	13- 89	AA		C	
〃	13- 90	AA		C	
〃	13- 91	AA		C	
〃	13- 92	AA		C	
〃	13- 93	AA		C	
〃	13- 94	AA		C	
〃	13- 95	AA		C	
〃	13- 96	AA		C	
〃	19- 31	AA		C	
VCCCTV1HH220J	13- 61	AA		C	
〃	13- 62	AA		C	
VCCCTV1HH221J	13- 115	AA		C	
〃	13- 117	AA		C	
〃	13- 118	AA		C	
〃	13- 119	AA		C	
〃	13- 120	AA		C	
〃	13- 121	AA		C	
〃	13- 122	AA		C	
〃	13- 123	AA		C	
〃	13- 124	AA		C	
〃	13- 125	AA		C	
〃	13- 126	AA		C	
VCCCTV1HH470J	13- 39	AA		C	
〃	13- 41	AA		C	
〃	13- 65	AA		C	
〃	13- 66	AA		C	
〃	13- 67	AA		C	
〃	13- 83	AA		C	
〃	13- 97	AA		C	
〃	13- 98	AA		C	
〃	13- 99	AA		C	
〃	13- 101	AA		C	
〃	19- 21	AA		C	
〃	19- 24	AA		C	
VCCSPU1HL101J	19- 32	AA		C	
〃	19- 33	AA		C	
VCKYTQ1EF474Z	13- 128	AB		C	
VCKYTV1EB103K	17- 5	AA		C	
VCKYTV1EF104Z	13- 40	AA		C	
〃	13- 43	AA		C	
〃	13- 44	AA		C	
〃	13- 45	AA		C	
〃	13- 46	AA		C	
〃	13- 47	AA		C	
〃	13- 49	AA		C	
〃	13- 50	AA		C	
〃	13- 51	AA		C	
〃	13- 52	AA		C	
〃	13- 56	AA		C	
〃	13- 57	AA		C	
〃	13- 58	AA		C	
〃	13- 60	AA		C	
〃	13- 68	AA		C	

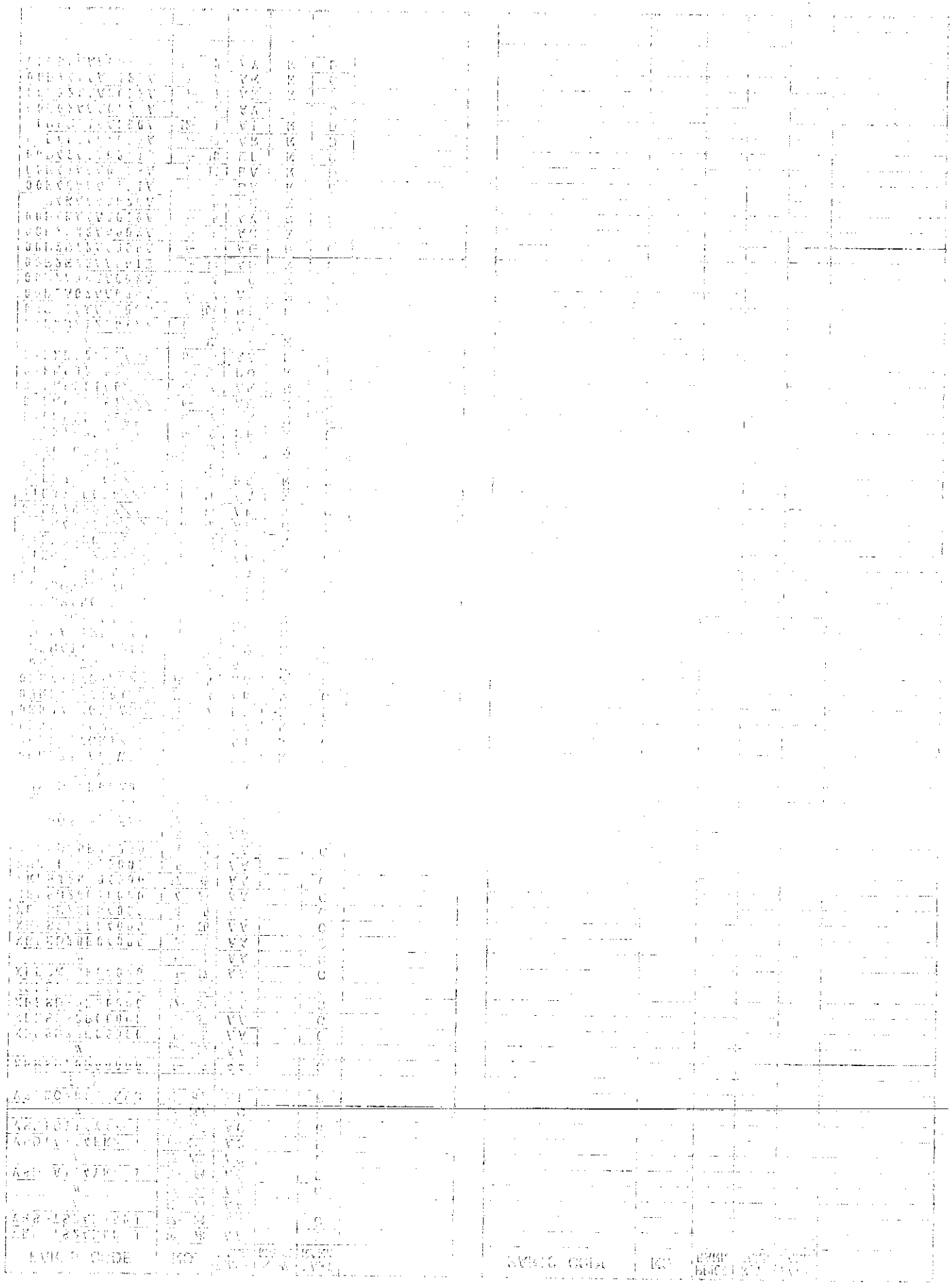
PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VCKYTV1EF104Z	13- 70	AA		C	
〃	13- 71	AA		C	
〃	13- 74	AA		C	
〃	13- 75	AA		C	
〃	13- 76	AA		C	
〃	13- 77	AA		C	
〃	13- 79	AA		C	
〃	13- 84	AA		C	
〃	13- 85	AA		C	
〃	13- 86	AA		C	
〃	13- 100	AA		C	
〃	13- 103	AA		C	
〃	13- 106	AA		C	
〃	13- 107	AA		C	
〃	13- 114	AA		C	
〃	13- 127	AA		C	
〃	16- 2	AA		C	
〃	16- 5	AA		C	
〃	17- 4	AA		C	
〃	17- 6	AA		C	
〃	18- 3	AA		C	
〃	18- 4	AA		C	
〃	18- 5	AA		C	
〃	19- 5	AA		C	
〃	19- 6	AA		C	
〃	19- 7	AA		C	
〃	19- 8	AA		C	
〃	19- 9	AA		C	
〃	19- 10	AA		C	
〃	19- 11	AA		C	
〃	19- 12	AA		C	
〃	19- 13	AA		C	
〃	19- 17	AA		C	
〃	19- 18	AA		C	
〃	19- 19	AA		C	
〃	19- 20	AA		C	
〃	19- 23	AA		C	
〃	19- 26	AA		C	
〃	19- 27	AA		C	
〃	19- 28	AA		C	
VCKYTV1EF223Z	13- 112	AA		C	
VCKYTV1EF473Z	13- 48	AA		C	
VCKYTV1HB102K	13- 42	AA		C	
〃	13- 53	AA		C	
〃	13- 54	AA		C	
〃	13- 55	AA		C	
〃	13- 63	AA		C	
〃	13- 64	AA		C	
〃	13- 69	AA		C	
〃	13- 72	AA		C	
〃	13- 73	AA		C	
〃	13- 78	AA		C	
〃	13- 80	AA		C	
〃	13- 81	AA		C	
〃	13- 82	AA		C	
〃	13- 102	AA		C	
〃	13- 104	AA		C	
〃	13- 105	AA		C	
〃	13- 113	AA		C	
〃	13- 116	AA		C	
〃	16- 3	AA		C	
〃	16- 4	AA		C	
〃	18- 1	AA		C	
〃	18- 2	AA		C	
〃	19- 15	AA		C	
〃	19- 22	AA		C	
〃	19- 25	AA		C	
VCKYTV1HB103K	19- 16	AB		C	
VCKYTV1HB221K	19- 3	AA		C	
〃	19- 4	AA		C	
VCSAPJ1AE106M	13- 59	AE		C	
〃	17- 3	AE		C	
〃	18- 6	AE		C	
VCSAPJ1CE336M	19- 14	AF		C	
〃	19- 29	AF		C	
〃	19- 30	AF		C	
VHDDA204K//-1	17- 11	AC		B	
VHDMA721///-1	13- 146	AC		B	
〃	13- 148	AC		B	
VHDMA724///-1	13- 149	AD		B	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
VHDMA724///-1	13- 150	AD		B
〃	13- 151	AD		B
〃	13- 152	AD		B
〃	13- 153	AD		B
〃	13- 154	AD		B
〃	13- 155	AD		B
VHD1SS332//-1	13- 147	AB		B
VHERD30EL1/-1	14- 10	AA		B
VHiALS38ANS//	13- 240	AE		B
VHiAM81EC176/	17- 18	BA		B
VHiC102FDAB1C	16- 8	BF	N	B
VHiC102FDAC1C	16- 9	BF	N	B
VHiKM41C464-1	13- 200	AQ		B
〃	13- 201	AQ		B
〃	13- 204	AQ		B
〃	13- 205	AQ		B
〃	13- 208	AQ		B
〃	13- 209	AQ		B
〃	13- 212	AQ		B
〃	13- 213	AQ		B
VHiLH5380MY-1	16- 7	BB		B
VHiLM334Z//-1	17- 19	AL		B
VHiLZ95H22/-1	13- 210	AZ		B
VHiSC146818P1	13- 202	AW		B
VHiSC9871//-1	13- 230	BC		B
VHiSC9889B/-1	13- 221	BP		B
VHiSN74HCT244	13- 244	AF		B
〃	13- 250	AF		B
VHiSN74HCT245	13- 231	AF		B
〃	13- 247	AF		B
VHiSN74HC02NS	13- 226	AC		B
〃	13- 239	AC		B
VHiSN74HC04NS	13- 228	AC		B
VHiSN74HC08DB	13- 233	AC		B
〃	13- 234	AC		B
〃	13- 235	AC		B
VHiSN74HC238S	13- 218	AF		B
VHiSN74HC27NS	13- 225	AC		B
〃	13- 238	AC		B
VHiSN74HC30NS	13- 243	AC		B
VHiSN74HC32NS	17- 17	AK		B
VHiSN74LS06-1	19- 62	AE		B
VHiSN74LS07-1	19- 38	AK		B
〃	19- 40	AK		B
VHiSN74LS14-1	19- 39	AM		B
VHiTC7S04FTPR	13- 215	AC		B
VHiTC7S08FTPR	13- 237	AC		B
VHiTC7S32FTPR	13- 236	AC		B
〃	13- 252	AC		B
VHiTC74AC02FN	19- 52	AD		B
VHiTC74AC10FN	13- 203	AD		B
VHiTC74AC11FN	19- 50	AD		B
〃	19- 51	AD		B
〃	19- 60	AD		B
VHiTC74AC174F	13- 241	AG		B
VHiTC74AC20FN	19- 61	AD		B
VHiTC74AC32FN	19- 48	AD		B
VHiTC74AC374F	13- 214	AK		B
VHiTC74AC541F	13- 242	AL		B
VHiTC74AC74FN	19- 53	AE		B
VHiTC74HC02FN	19- 54	AD		B
VHiTC74HC04FN	19- 43	AD		B
〃	19- 57	AD		B
〃	19- 58	AD		B
VHiTC74HC10FN	19- 45	AD		B
VHiTC74HC125F	19- 56	AH		B
VHiTC74HC138F	19- 49	AL		B
VHiTC74HC157F	19- 46	AE		B
VHiTC74HC32AF	19- 47	AE		B
〃	19- 59	AE		B
VHiTC74HC74FN	19- 42	AF		B
〃	19- 44	AF		B
〃	19- 55	AF		B
VHiTC8566AF-1	19- 41	AZ		B
VHiUPD4714GT1	13- 251	AW		B
VHi3JD2CA1A-1	13- 206	AU		B
VHi518128AFL8	13- 216	BC		B
〃	13- 217	BC		B
〃	13- 222	BC		B
〃	13- 223	BC		B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
VHi518128AFL8	13- 245	BC		B
〃	13- 246	BC		B
〃	13- 248	BC		B
〃	13- 249	BC		B
〃	18- 8	BC	N	B
〃	18- 9	BC	N	B
〃	18- 10	BC	N	B
〃	18- 11	BC	N	B
〃	18- 12	BC	N	B
〃	18- 13	BC	N	B
〃	18- 14	BC	N	B
〃	18- 15	BC	N	B
VHi74AC11238N	13- 224	AM		B
VHi74HCT373MF	13- 219	AH		B
VHi80C286/-12	13- 211	BP		B
VHi80C42G//-1	13- 220	AT		B
VHi80C52N//-1	13- 207	AZ		B
VHi82C455R4-1	13- 227	BY		B
VHPGL3ED8//-1	13- 254	AC		B
VHPGL3EG44/-1	13- 256	AA		B
〃	13- 257	AA		B
〃	13- 258	AA		B
〃	13- 259	AA		B
〃	13- 260	AA		B
〃	13- 261	AA		B
VHPGL3HD44/-1	13- 255	AB		B
VHSDTND104J4M	14- 7	AC		B
VRD-HT2EY102J	13- 314	AA		C
VRD-HT2EY332J	17- 37	AA		C
VRD-RC2EY104G	14- 4	AA		C
VRD-RC2EY183G	14- 5	AA		C
VRS-TS2AD101J	13- 286	AA		C
〃	13- 287	AA		C
〃	13- 302	AA		C
〃	17- 28	AA		C
〃	19- 74	AA		C
〃	19- 75	AA		C
VRS-TS2AD102J	13- 271	AA		C
〃	13- 293	AA		C
〃	19- 71	AA		C
〃	19- 76	AA		C
〃	19- 77	AA		C
〃	19- 80	AA		C
VRS-TS2AD103J	13- 282	AA		C
〃	13- 289	AA		C
〃	13- 290	AA		C
〃	17- 21	AA		C
〃	17- 23	AA		C
VRS-TS2AD104J	13- 294	AA		C
VRS-TS2AD150J	17- 29	AA		C
VRS-TS2AD151J	17- 30	AA		C
VRS-TS2AD152J	13- 296	AA		C
VRS-TS2AD153J	13- 299	AA		C
〃	19- 79	AA		C
VRS-TS2AD154J	13- 270	AA		C
VRS-TS2AD223J	13- 268	AA		C
〃	13- 272	AA		C
〃	13- 273	AA		C
〃	13- 274	AA		C
〃	13- 275	AA		C
〃	13- 276	AA		C
〃	13- 277	AA		C
〃	13- 278	AA		C
〃	13- 279	AA		C
VRS-TS2AD273J	13- 295	AA		C
VRS-TS2AD331J	13- 291	AA		C
VRS-TS2AD332J	13- 280	AA		C
〃	13- 281	AA		C
〃	13- 297	AA		C
VRS-TS2AD470J	13- 285	AA		C
〃	13- 288	AA		C
VRS-TS2AD472J	13- 298	AA		C
〃	13- 301	AA		C
〃	19- 72	AA		C
〃	19- 73	AA		C
VRS-TS2AD473J	13- 300	AA		C
VRS-TS2AD562J	13- 292	AA		C
VRS-TS2AD563J	17- 22	AA		C
〃	17- 27	AA		C
VRS-TS2AD565J	13- 269	AA		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VRS-TS2AD683J	19- 78	AA		C	
VRS-TS2AD750J	17- 24	AA		C	
〃	17- 25	AA		C	
〃	17- 26	AA		C	
VSDTA114YK/-1	13- 264	AC		B	
〃	13- 265	AC		B	
VSDTA144EK/-1	13- 266	AC		B	
VSDTC114YK/-1	13- 263	AC		B	
〃	13- 267	AC		B	
VS2SC2021-RSC	13- 262	AF		B	
〔X〕					
XBBSD20P06000	5- 3	AA		C	
〃	13- 313	AA		C	
XBBSD30P06000	5- 5	AA		C	
XBBSF30P06000	1- 37	AA		C	
XBPSD30P06000	17- 34	AA		C	
XBPSF30P06000	5- 17	AA		C	
XBPSN20P04000	1- 17	AA		C	
〃	5- 1	AA		C	
XBSSD20P04000	2- 4	AA		C	
XBSSF26P04000	1- 26	AA		C	
XEBSD26P04000	4- 5	AA		C	
XESSD26P10000	4- 23	AA		C	
XRESJ25-04000	17- 35	AA		C	
XUBSF30P10000	5- 18	AA		C	
XUPSD30P08000	1- 34	AA		C	
〃	5- 12	AA		C	
XUSSD26P06000	4- 32	AA		C	
XUSSD26P07000	4- 31	AA		C	
XUSSD30P06000	2- 6	AA		C	
〔0〕					
0BR2717ALPWB/	15- 6	BS	N	E	
0BR2717CN1///	15- 2	AT	N	C	
0BR2717CN3///	15- 1	AY	N	C	
0BR2717GLPWB/	15- 7	BP	N	E	
0BR2717J101//	15- 3	AK	N	C	
0BR2717P1////	15- 5	AK	N	C	
0BR2717S1////	15- 4	AT	N	B	
0DBBATT8-2200	8- 2	BQ	N	B	
0DBCABiNET-AU	8- 1	BH	N	D	
0DBCABiNET-B/	8- 3	BH	N	D	
0DBCHARGER-UT	8- 5	CF	N	E	
0DBCONNECTOR/	8- 4	BF	N	C	
0iEE16200026/	6- 16	AA	N	C	
0iEK160205///	6- 7	AG	N	C	
0iEK32003403/	6- 3	AD	N	C	
0iEK410793///	6- 12	AB	N	C	
0iEK790677///	6- 10	AK	N	C	
0iEK790678///	6- 11	AA	N	C	
0iEK790700///	6- 6	BR	N	B	
0iEK790740///	6- 9	BB	N	B	
0iEK790741///	6- 10	AK	N	C	
0iEK790742///	6- 9	BB	N	B	
0iEK90215603/	6- 2	AN	N	D	
0iEK902157///	6- 1	AM	N	D	
0iEK902160///	6- 4	AN	N	S	
0iEK902193///	6- 14	BQ	N	E	
0iEXB12260405	6- 5	AA	N	C	
〃	6- 13	AA	N	C	
0iEXD21200122	6- 8	AA	N	C	
00PJ1AAA2006B	7- 101	BL	N	C	
00P2A02AA005A	7- 7	AG	N	C	
00P2A09AA002A	7- 4	AG	N	C	
00P2B72AA001B	7- 13	AG	N	C	
00P2B72AA005A	7- 3	AG	N	C	
00P2C02AA002A	7- 9	AG	N	C	
00P4KA4AA019A	7- 5	AV	N	C	
00P4KA4AA020A	7- 8	BH	N	C	
00P40AAA0131A	7- 1	BA	N	D	
00P41AAA0103A	7- 14	BA	N	D	
00P42AAA0271C	7- 10	BF	N	C	
00P49AAA2002A	7- 12	AR	N	D	
00P5B115A090A	12- 1	AT	N	D	
00P62AAA0271A	7- 6	AV	N	C	
00P72AAA0052A	7- 11	AN	N	C	
00P74AAA0123A	7- 2	AN	N	C	
00P98AAA0020A	12- 2	AY	N	D	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	



SHARP

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