TEAC FD-55AV / GV
MINI FLEXIBLE DISK DRIVE
MAINTENANCE MANUAL

TEAC®

TEAC FD-55AV ~ GV

MINI FLEXIBLE DISK DRIVE

MAINTENANCE MANUAL

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THEORY OF OPERATION

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3-1-1. General Block Diagram
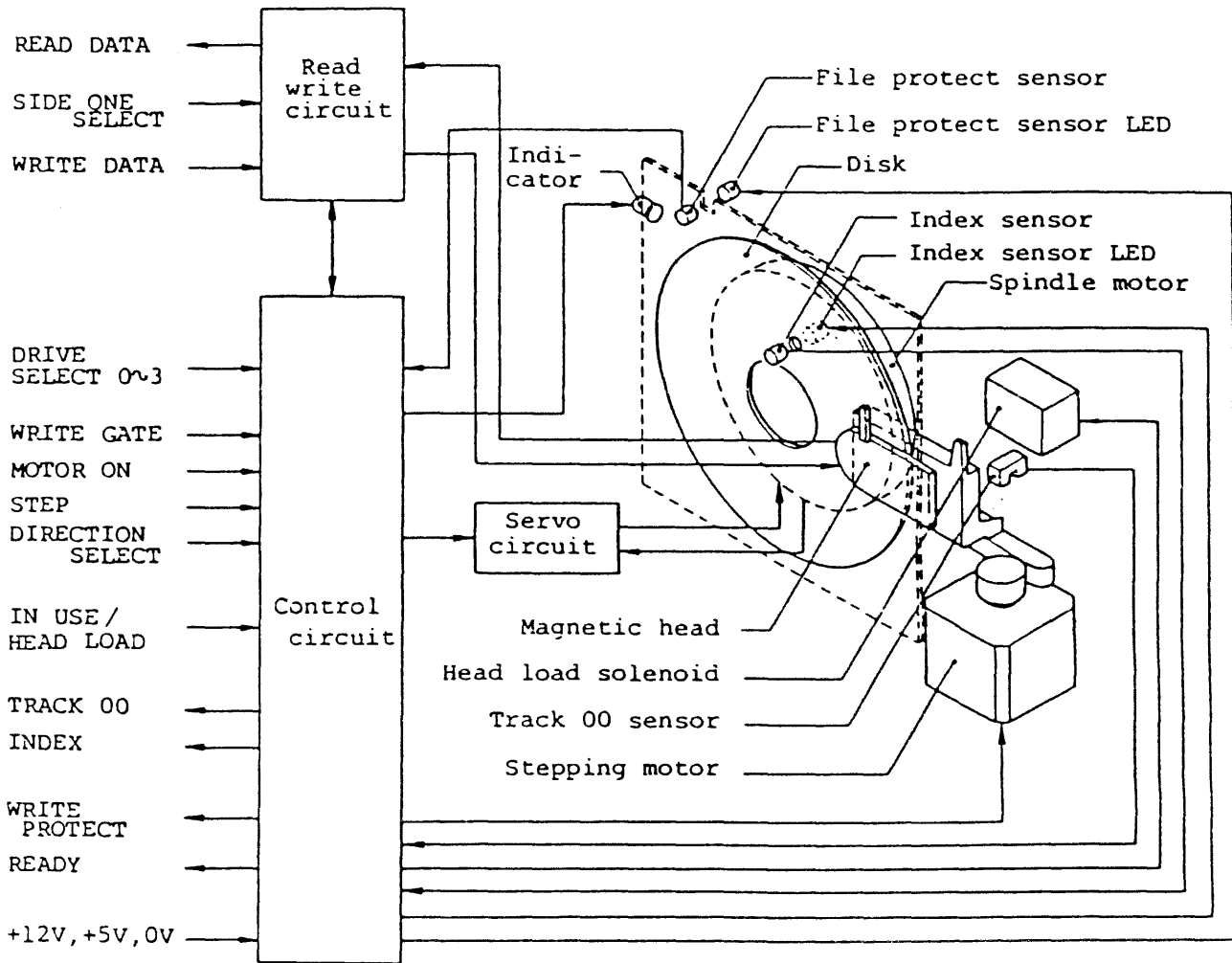
(Fig.301) General block diagram

3-1-2. Mechanical Section

Since the disk is a flexible recording media made of mylar film base and data interchangeability between disks and FDDs is required, the mechanical section of the FDD uses precision parts and it is also assembled carefully and precisely. For this reason, only trained technicians can handle the internal mechanism. Never apply excessive impact nor drop the FDD down on the desk.

The mechanical section is constructed with frame, door mechanism, disk clamp mechanism, disk rotation mechanism, magnetic head and carriage, head load mechanism (or CSS mechanism), head seek mechanism, various detection mechanisms, etc.

(1) Frame

The main structure for mounting the various mechanisms and printed circuit boards. The frame is made of aluminum diecast to maintain the stability of the FDD in strength, precision, durability, and expansion coefficient.

(2) Door mechanism and disk clamp mechanism

The door mechanism is constructed with the main parts of set arm which forms the structure for installing the disk on the spindle; other parts of front lever, clamp arm, etc. The set arm is attached to the rear of the frame with leaf spring and on the tip of the set arm a collet, which forms the disk clamp mechanism, is attached.

When a disk is inserted and the door is closed, the collet is inserted into the center hole of the disk and the disk is clamped in the correct position along the outer circumference of the collet.

(3) Disk rotation mechanism

The disk rotation mechanism comprises DD motor Ass'y which includes

spindle.

The DD motor is an outor-rotor type DC brushless motor which has the
long life of 30,000 hours or more in continuous rotation.

The rotation speed is 300rpm for A ∿ F models or 360rpm for G model
and is maintained at a stable condition against load variations and
environmental changes. This is achieved by a feedback signal from the
internal AC tachometer.

The collet and the spindle are combined precisely to maintain the
center position correctly without damaging the center hole of a disk
and so as to make the head be in contact with the disk at a correct
position.

(4) Magnetic head and carriage
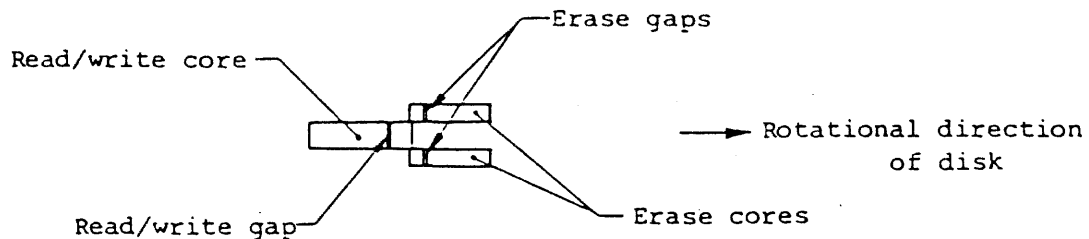
(Fig.302) External view of magnetic head core

The magnetic head assembly (head carriage Ass'y) of a single sided
model (A or E model) is button type, which is mounted on the carriage
to be in contact with the head window area of the side 0 surface of a
disk (down surface when the FDD is situated horizontally). For a
double sided model (B, F, or G model), both of the side 1 head and
the side 0 head are special flat type supported with the gimbaled
mechanisms. The two magnetic heads are mounted accross the disk on one
carriage (head carriage).

In both types of head, the surface is designed for minimum disk wear
and maximum read output. The head itself is a long life type for
improved head wear. Each head is constructed with a read/write gap

used for data reading and data writing and two erase gaps to erase the recorded track edge immediately after the recording (tunnel erase). The magnetic ehad and the carriage form the core section of the FDD and is specially assembled with high precision.

(5) Head load mechanism or CSS mechanism

The head load mechanism is used for models with head load solenoid and the CSS mechanism is used for double sided CSS model without head load solenoid.

The head load mechanism functions to make the head in contact with a disk when only required so as to reduce disk and magnetic head wear. This mechanism is constructed with head load solenoid, arm lifter, etc. If the head loading is executed for a single sided model, the head pad attached to the pad arm of the carriage is depressed lightly against the side 1 surface of a disk.
For a double sided model, the side 1 head attached to the upper arm of the carriage is depressed against the side 1 surface of a disk with an appropriate pressure.
The side 0 surfaces of the head and the disk are set to the same height and the depression of the side 1 head produces the stable contact between the heads and the disk.

In the CSS model, the magnetic heads are always in contact with a disk as far as the disk is installed. In order to elongate the disk and head leves, it is required to make the disk rotate only when it is necessary.
The CSS mechanism is constructed with a CSS Ass'y which is designed to protect the contact of side 0 and side 1 heads directly when the front lever is closed without disk. For the purpose os protecting the head being caught and damaged by the head window edge during disk insertion and ejection, head protector is also equipped to the CSS mechanism to lift up the disk jacket. The head protector is also used

in models with head load solenoid.

(6) Head seek mechanism

The head seek mechanism consists mainly of stepping motor with a capstan
(pooly), steel belt (band), and guide shafts. The head carriage is
connected to the capstan of the stepping motor through the steel belt
and is slided along the guide shafts.
The stepping motor rotates 2 steps (3.6°) in 48tpi models and 1 step
(1.8°) in 96tpi models for one track space. In some 48tpi models,
the stepping motor rotates 3.6° for one steps. For all models, hybrid
type 4-phase stepping motor is adopted to improve speed of the head
seek operation and precision of the head positioning. This special
motor is driven in a unique manner which brought a success in reducing
the heat radiation and to obtain a highly precise positioning.
The parallelism and the distance between the shafts and the center
line of a disk, and shafts and capstan themselves are precisely machined.
Also the thermal expansion of the frame, steel belt, carriage, etc. are
taken into consideration in the process of design so that they are
mutually offset with the expansion of the disk.

(7) Detection mechanisms

  (a) File protect detection mechanism

    This mechanism is constructed with an LED and a photo-transistor to
    detect the existence of the write enable notch of the disk jacket.
    When a disk with the notch covered is installed and the light pass
    for detection is disturbed, no write or erase current will be supplied
    to the read/write and erase heads and the recorded information on the
    disk is protected from an erroneous input of a write command.
    The LED is mounted on the PCBA DD motor servo and the photo-transistor
    on the PCBA front OPT #H.

(b) Track 00 detection mechanism

This mechanism is constructed with a photo-interrupter for detecting
the outermost track position (track 00) of the head and with a track
00 stopper which are attached to the rear side of the head carriage.
Inside tracks from the track 00 on the disk are used. Even if an
erroneous step out command is input from the track 00 position, the
command will be ignored by the internal circuit of the FDD.
If the head moves out from the track 00 by some reason (such as
impact during transportation), the head carriage strikes the track 00
stopper to protect the head from moving out of the returnable range
at a next power on. If V-type carriage is used (refer to Note 12 of
item 5-2-1 and Table 505), the frame edge functions like a track 00
stopper. And if L-type carriage (refer to Table 504) is used, a
screwed small parts functions as a track 00 stopper.

When step-in commands are input from the innermost track, the head
moves toward inward with an appropriate space left against
the head window edge of the disk. In order to recalibrate the track
from this position (returning operation to the track 00), it is
required to input the step-out commands with several additional steps
to the maximum track number.

(c) Index detection mechanism

LED and photo-transistor for detecting the index hole are located
at the index window area of the disk jacket.
The LED is mounted on the PCBA DD motor servo (in the rotor of spindle
motor) and the photo-transistor on the PCBA front OPT #H. The index
hole will be detected along the rotation of the disk.

3-2. CIRCUIT DESCRIPTIONS

The electronics of the FDD is constructed with three sections which are read write circuit, control circuit, and servo circuit.   Read write circuit and control circuit are mounted on the PCBA MFD control #H, and servo circuit is on the PCBA DD motor servo.

3-2-1. Read Write Circuit

The read write circuit is constructed with mode selector, read circuit, write circuit, low voltage sensor.   They are mostly packed in a read write LSI (bipolar LSI, U5).

Fig.303 shows the block diagram.

(Fig.303) Block diagram of read write circuit

LOW PASS FILTER
L4. L5. RA11. C18. C29

SWITCH FILTER
C30. C31. Q7. Q8. U1

TRACK SWITCH. SF

GAIN SELECTOR
S4/S5

TP4 TP5
A5V
C17 C20

DIFFERENTIATOR
R22. C32. L3. C35

GSC GSO GS1 AVGG PRED PRED DIFI DIFI DIFC DIFC DIFO

11 10 9 8 7 6 5 4 3 2 1

LSI
U5

C25
TP8

READ WRITE COIL
ERASE COIL
COMMON(CENTER TAP)

SIDE0
HEAD

J9-12

RW00 12
RW10 13   HEAD   PRE.
RW01 14   SWITCH   AMP
RW11 15   MATRIX

ACTIVE
DIFFERENTIATOR

PEAK
DETECTOR

44 DIFO
43 CI
42 CI

C24
TP7
5V

AGND 16
WT 17
WT 18

LOW VOLTAGE SENSOR
DVGG
EVCC   LVS0   LVS1

TIME
DOMAIN
FILTER

41 DVGG
40 TDCR
39 RDCR

TIME CONSTANT
C21. C22. RA8

WRITE
DRIVER

38 DGND
37 LVGG

SIDE1
HEAD

COM1 19

12V
EVCC 20

COM0 21

COMMON
DRIVER

C23
36 CD   0V

CR3 R12 ED1 22

ERASE
DRIVER

WRITE
CURRENT
SOURCE

WRITE CONTROL
LOGIC

35 OINV
34 DS

RD DRIVER

HIGH/APS /APS OPEN/RDY0 LOW HIGH PCB A~E RD OUTPUT CONTROL
HIGH/APS OPEN/RDY0 OPEN/RDY0 HIGH HIGH/APS PCB F~
HIGH HIGH

23 24 25 26 27 28 29 30 31 32 33

R11

0V EGND   EDO WCS1 WCS0 CS WD WG EG S1 LVS RD

ASYMMETRY ADJUSTOR
R1

WRITE CURRENT
SWITCH
R8. R9. Q1

OUTPUT
DRIVER

TP2

J1-22
WRITE
DATA

WG
EG

J1-32
SIDE ONE
SELECT

J1-30
READ
DATA

LVS DRIVE
SELECT

TRACK
SWITCH

- 308 -

3-2-1-1. Mode selector

Mode selector is constructed with the switch filter and write current
switch, which are used only for 96tpi models.
Table 301 shows the switching condition of the read write circuit by
the track switch signal (SF signal in the schematic diagram) from the
control circuit.

(1) Switch filter

Switch filter is used only in G model and in optional F model for
eliminating the influence of saddle waveform (refer to Fig.304) at the
outer tracks. When the SF signal is HIGH level, the output of the NPN
transistors, Q7 and Q8 (includes resistors internally) becomes LOW
level. Then the switch filter capacitors, C30 and C31 are activated to
increase the capacity of the low pass filter capacitor, C29. This state
is the On-state of the switch filter, and the cut-off frequency of the
low pass filter is set to low.

(2) Write current switch

Write current switch is used only in E, F, and G models and used for
making the write current in outer tracks (track 00 to track 43) higher
than in inner tracks (track 44 to track 79) to improve the over-write
(write 2F after 1F write and measure the residual frequency components
of 1F) and sholder characteristics.

Write current is supplied to the write driver by write current source
in the read write LSI, U5. The supplied value from this current source
can be calculated from the following expression combining the external
resistors R9, R8, and Q1 (ON at outer tracks).

$$\text{Outer tracks: } Iw = \frac{13.2}{R9} + \frac{12.7}{R8} - 0.12 \text{ --- No.1}$$

Inner tracks: $Iw = \dfrac{13.2}{R9} - 0.12$ --- No.2

(Reference)

Erase current is calculated from the following expression. Write
current is not switched depending on the track position.

$Ie = \dfrac{10.8}{R11 \ (or \ R12)}$ --- No.3

Switching item	Models and track position				
	A,B (48tpi) all tracks	E,F (96tpi).		G(96tpi,high density)	
		Tr.00∿43	Tr.44∿79	Tr.00∿43	Tr.44∿79
SF signal	H	H	L	H	L
Switch filter	No circuit	ON	OFF	ON	OFF
Write current sw. (Current exp.)	Constant No.2	No.1	No.2	No.1	No.2
Erase driver (Current exp.)	Constant No.3	←	←	←	←

(Table 301) Switching function of mode selector for read write circuit

3-2-1-2. Read circuit

The read circuit consists of head matrix switch, pre-amplifier, low pass filter, differentiation amplifier, peak detector, time domain filter, and output driver. Main circuits are enclosed in the read write LSI, U5.

The minute voltage induced in read operation by the read/write head is input to pre-amplifier via matrix switch for selecting side 0/1 heads. The pre-amplifier has three gain setting terminals, GS0, GS1 and GSC. In A ~ F models, GS0-GSC is shorted to obtain the gain of 100 times, while GS1-GSC is shorted in G model to obtain the gain of 200 times. The pre-amp. output is supplied to the differentiation amplifier via the low pass filter and the switch filter to eliminate undesirable high frequency noises. The differentiation amplifier phase-shifts the peak position of the reproduced waveform to zero cross point, and at the same time, further amplifies the signal with the most appropriate equalization. The peak detector constructed with a comparator converts the differentiated output after passing through the coupling capacitors, C24 and C25 into a square wave.
The time domain filter eliminates a virtual pulse caused by the saddle in the low frequency area (1F area, 62.5KHz for A ~ F models, 125KHz for G model) at outer tracks. The time domain filter is constructed with two edge detectors, delay single shot, read data latch, and data single shot. Then the signal is output from the FDD through the RD driver and the output driver.

In the RD driver (3-state output) of the read write LSI, U5, there are some gates. To the TDCR terminal for pulse width setting of delay single shot m.v., control signal from the control circuit (OPEN/RDYO/ APS signal) is input in parallel. These control signals are different depending on PCB issue numbers (A ~ D, E, or F ~) and FDD models (PCBA versions). Anyway, the FDD is so set that the RD terminal outputs positive read pulses at read operation. Table 302 shows the control function.

PCB issue No.	Typical PCBA Version	RD output control			No positive pulse outputs on RD terminal at: (RD output: LOW level)
		TDCR	OINV	$\overline{DS}$	
A∿D	-00 A∿C -04 A∿C	OPEN	H	L	During write operation (Internal control of LSI)
	-14,A,B	RDYO	H	L	During write + Drive not-READY (RDYO:LOW)
E	-08,B,C -10A -15A	APS	H	L	During write + During motor start-ting (360∿380ms after MON) + Head seek operation
F∿	-00D∿ -04D∿	OPEN	H	H	The same as -00∿04 of PCB issue A∿D.
	-08D∿ -10B∿ -14C∿ -15B∿	RDYO	H	H	The same as -14 A∿D of PCB issue A∿D.
	Special	RDYO	APS	H	During write + Drive not-READY + Head seek operation.

(Table 302) RD output control of read write LSI

Magnetization
on disk

Pre-amp.output
(TP4)   Shoulder   2.5V,
                                                                                                approx.

Pre-amp.output
(TP5)   2.5V,
                                                                                                approx.

                                                        Saddle

Differentiation
amp.output(TP7)   2.5V,
                                                                                                approx.

                                                        Zero corss point

Differentiation
amp.output(TP8)   2.5V,
                                                                                                approx.

Peak detector
output in U5
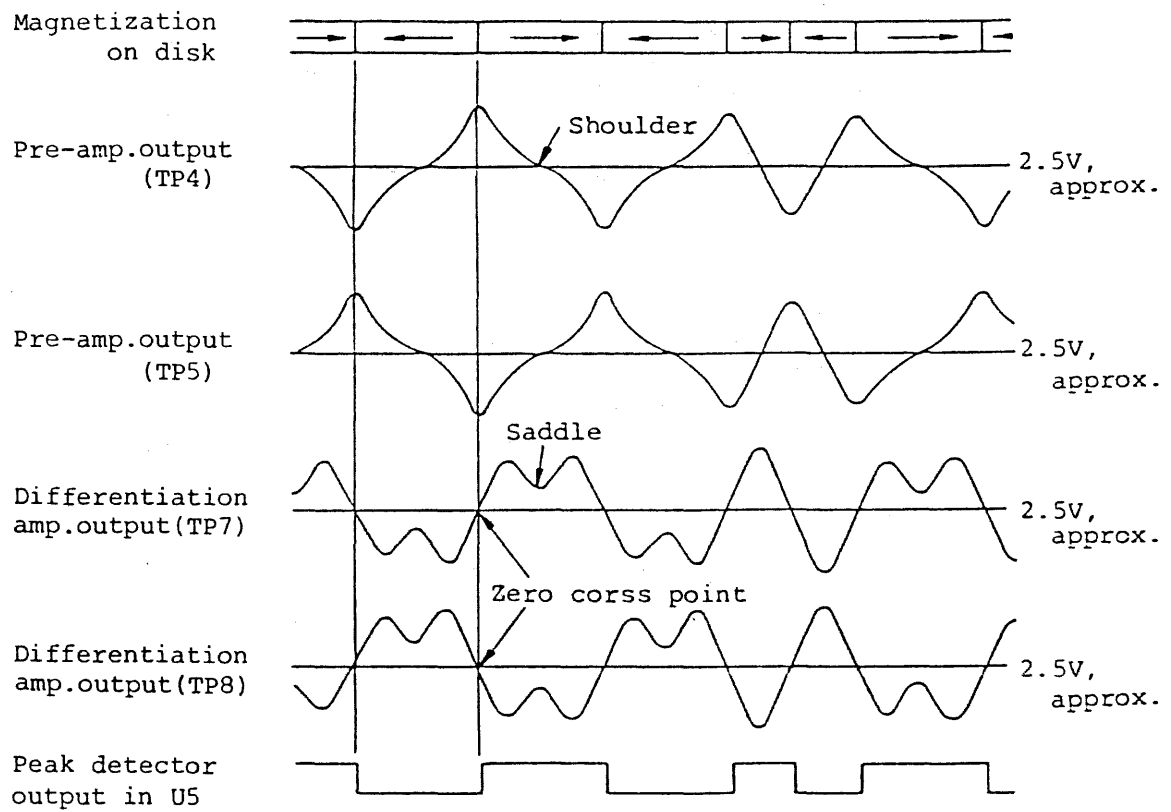
(Fig.304) Read amplifier and peak detector waveforms
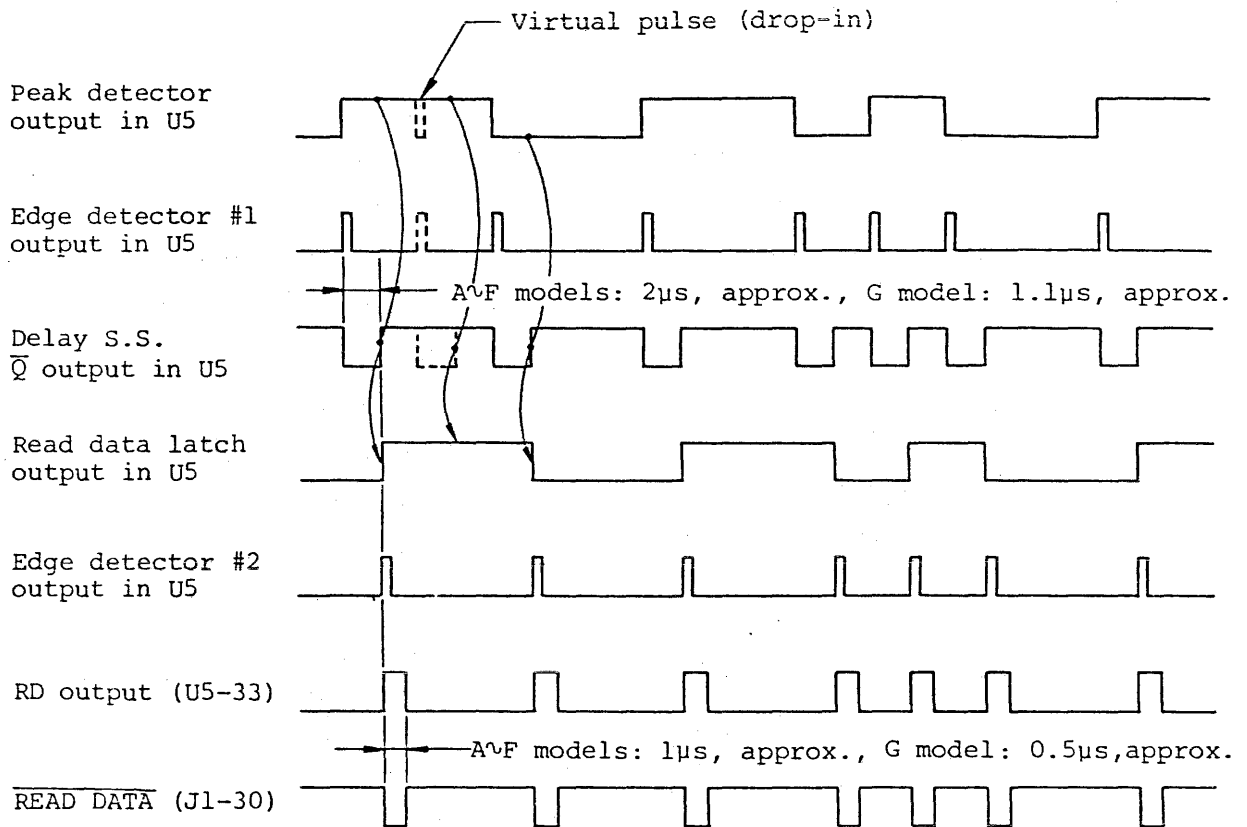
(Fig.305) Time domain filter and read gate waveforms

3-2-1-3. Write circuit

The write circuit consists of write control logic, write current source, write driver, erase driver, common driver, and etc. Most of the circuits are enclosed in the read write LSI, U5.
Common driver output terminals, COM0 and COM1 are connected to the common terminals (center taps) of the side 0 and side 1 heads, respectively. The outputs of the common driver are controlled by the SIDE ONE SELECT (S1) input signal, and write gate (WG)/erase gate (EG) signals supplied through the write control logic. When the COM0 or the COM1 is HIGH level (11.5V, approx.), the power to the read circuit is cut off in the read write LSI to inhibit the read operation.

Input signals			FDD operation	Output voltage (approx.)	
S1	WG	EG		COM0	COM1
H	H	H	SIDE 0 read operation	2.7V	0V
H	L	—	SIDE 0 write operation	11.5V	0V
H	—	L	SIDE 0 write operation	11.5V	0V
L	H	H	SIDE 1 read operation	0V	2.7V
L	L	—	SIDE 1 write operation	0V	11.5V
L	—	L	SIDE 1 write operation	0V	11.5V

(Table 303) Common driver output

The EG signal supplied from the erase timer in the control circuit changes to HIGH or LOW level with an appropriate time delay against the WG signal (refer to Fig.306). Since the erase gaps locate about 0.85mm (A ∿ F models) or 0.585mm (G model) backward and across the read/write gap, it is necessary for the erase driver to delay the WG signal so that the written data is completely trimmed by the erase head (tunnel erase). The tunnel erase produces a guard band between the tracks preventing deterioration of the S/N ratio resulting from a off-track (positioning error). It also ensures disk interchangeability.

The WRITE DATA input pulse is latched by the write data latch in the
write control logic. And appropriate write current from the write
current source is supplied to the read/write head by turning on and off
the two write drivers alternately.

WRITE GATE (J1-24)

Erase-on
delay   Erase-off
                            delay

WG (U5-29)

EG (TP2)

SIDE ONE SELECT
(J1-32)

WRITE DATA (J1-22)

Write data latch
in U5

Write driver output
(U5-17,18,12∿15)

Write current

Magnetization on
disk

Previous magnetization
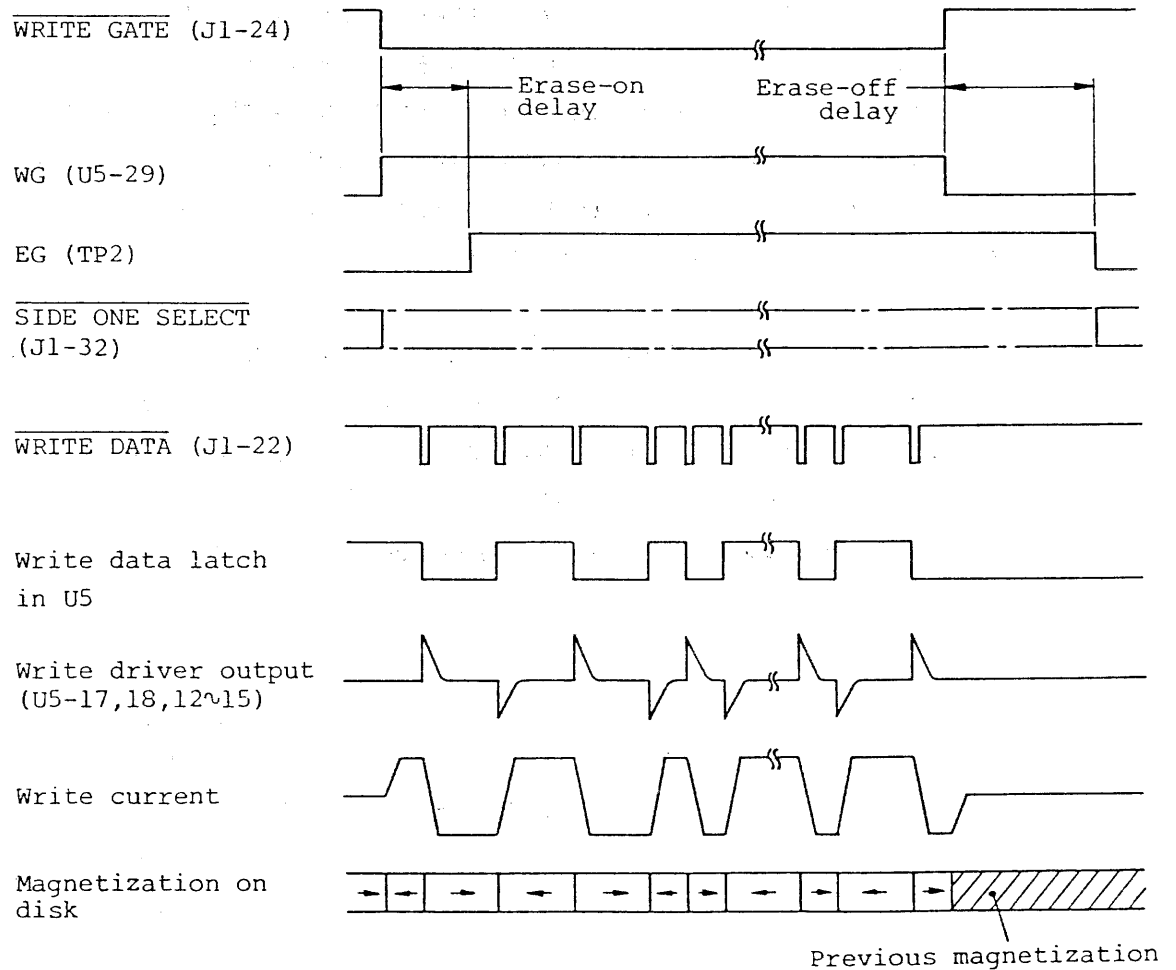
(Fig.306) Typical waveform of write circuit operation

3-2-1-4. Low voltage sensor

The low voltage sensor is equipped to protect the FDD from erroneous
operation due to the internal circuit construction of the FDD during
unstable state of the power voltage such as at power on or off. Two
sensors of LVS0 and LVS1 are equipped in the read write LSI, U5.
LVS0 monitors the +5V and +12V voltage supplied to the internal circuit
of the read write LSI. If the voltage is lower than 3.5V through 4.4V,
it supplies signals to inhibit the operation of the common driver,
write driver, erase driver, and write control logic in the LSI, which
protect the disk from an erroneous write or erroneous erase during
unstable state of the power voltage.

LVS1 is equipped to generate $\overline{LVS}$ signal to be supplied to the control
circuit in item 3-2-2. As well as LVS0, it is activated in the range
of 3.5V through 4.4V. The monitored voltage by the LVS1 is only +5V
connected to the LVGG terminal (pin 37) of the read write LSI. While
the $\overline{LVS}$ signal is LOW level, all the control circuits (mainly control
LSI, U3) are reset.
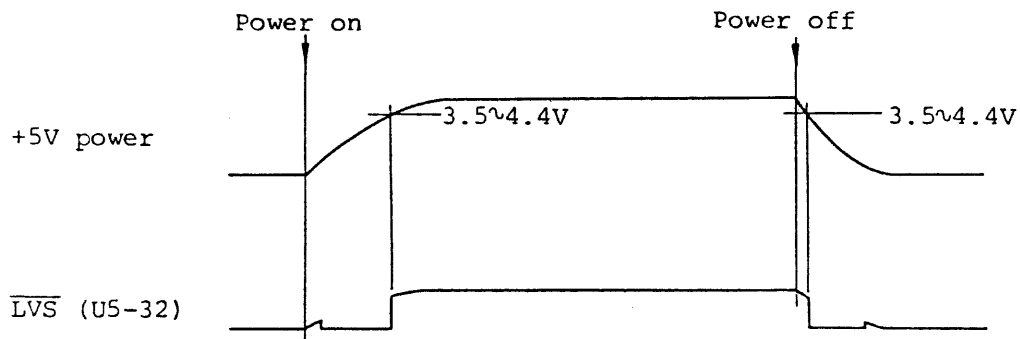
(Fig.307) Typical waveform of low voltage sensor

3-2-1-5. Function and operating waveform of read write LSI terminals

Following shows the function of the read write LSI, U5 and typical
operation waveforms.

(1) Pre-amplifier

(a) RW00 (pin 12), RW01 (pin 14)

Terminals for side 0 head connection.

Side 0 write

11.5V,approx.

WRITE DATA interval

Side 0 read: 2.7V, approx.

Side 1 write: 0V, approx.

Side 1 read: 0V, approx.
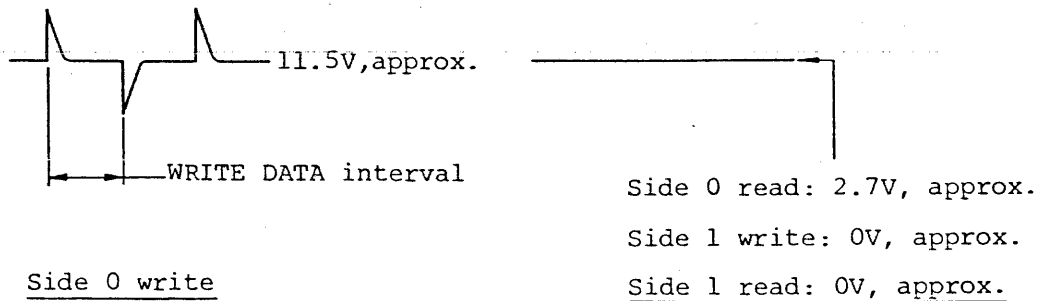
(b) RW01 (pin 13), RW11 (pin 15)

Terminals for side 1 head connection.

Side 1 write

11.5V,approx.

WRITE DATA interval

Side 1 read: 2.7V, approx.

Side 0 write: 0V, approx.

Side 0 read: 0V, approx.
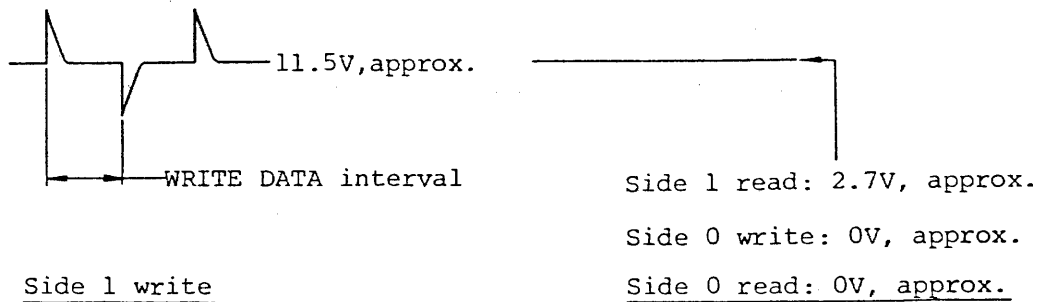
(c) GSC (pin 11), GS0 (pin 10), GS1 (pin 9)

Setting terminals of pre-amplifier gain.
If GSC-GS0 is shorted or connected with a capacitor, the differential

voltage gain of the pre-amplifier is increased to 100 times. Also
if GSC-GS1 is shorted or connected with a capacitor, it becomes 200
times.

(d) PREO (pin 7, pin 6)

Differential output terminals of the pre-amplifier. The phase of
pins 6 and 7 are opposite each other. (Refer to Fig.304).

2.7V,approx.   2.7V,approx.

      Read   Write
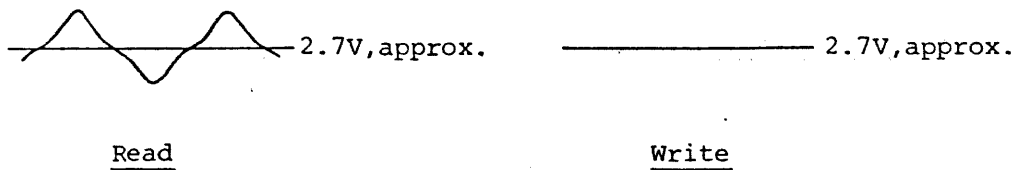
(2) Differentiation amplifier

(a) DIFI (pin 5, pin 4)

Differential input terminals to the differentiation amplifier.
The phase of pin 5 and 4 are opposite each other.

2.5V,approx.   2.5V,approx.

      Read   Write
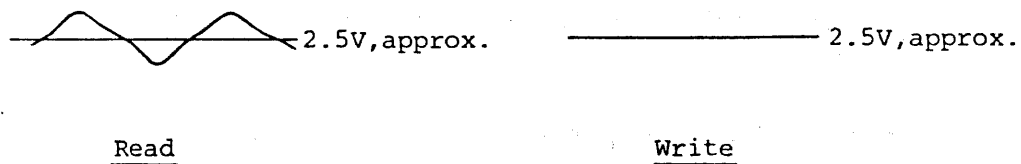
(b) DIFC (pin 3, pin 2)

Time constant setting terminals of the differentiation amplifier.
The phase of pin 3 and 2 are opposite each other.

— 1.1V,approx.   ————————— 1.1V,approx.

            Read   Write
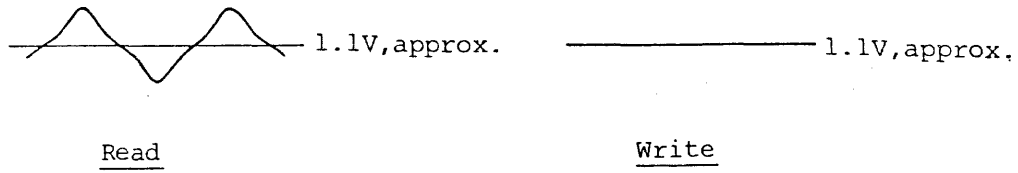
(c) DIFO (pin 1, pin 44)

Differential output terminals of the differentiation amplifier.
The phase of pin 1 and 44 are opposite each other.

—2.7V,approx.   ———————— 2.7V,approx.

            Read   Write
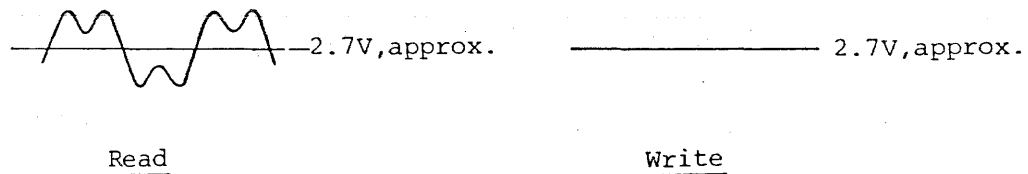
(d) CI (pin 43, pin 42)

Differential input terminal of the comparator (peak detector). The
phase of pin 43 and 42 are opposite each other.

— 2.5V,approx.   ————————2.5V,approx.

            Read   Write
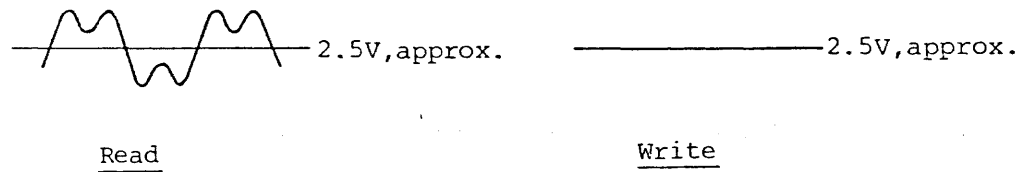
(3) Time domain filter

(a) TDCR (pin 40)

    Pulse width setting terminal of the delay single shot m.v.   Some
    models use this terminal for the inhibit gate of the RD pulse output.
    While this terminal is forced to be LOW level, the delay single shot

do not operate and no RD pulse is output. Refer to Table 302.

```
 ─┐ /│─┐ /─┐ /─┐ /─ 1.5V,approx.        ────────────────────┐
  │/ │/  │/  │/                                              │
  │ │                                                        │
 ─┤ ├──Delay single shot          Write: 1.5V,approx.        │
  │ │    pulse width
                                  Read inhibit: 0.7V,approx.
```

   Read
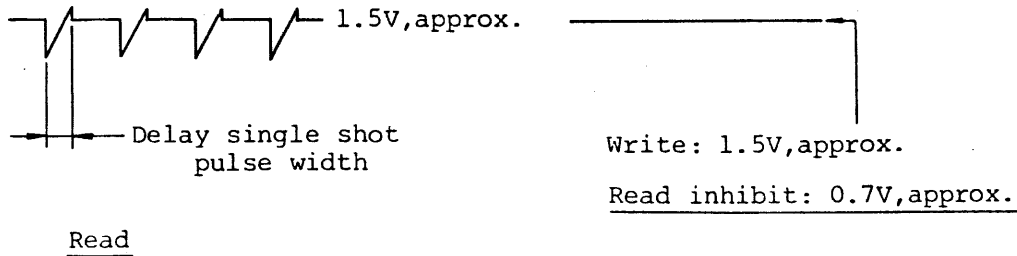
(b) RDCR (pin 39)

   Pulse width setting terminal for the RD output pulse.

```
 ─┐ /│─┐ /─┐ /─┐ /─ 2V,approx.      ───────────── 2V,approx.
  │/ │/  │/  │/
  │ │
 ─┤ ├──RD pulse width              Write & read inhibit
```

   Read
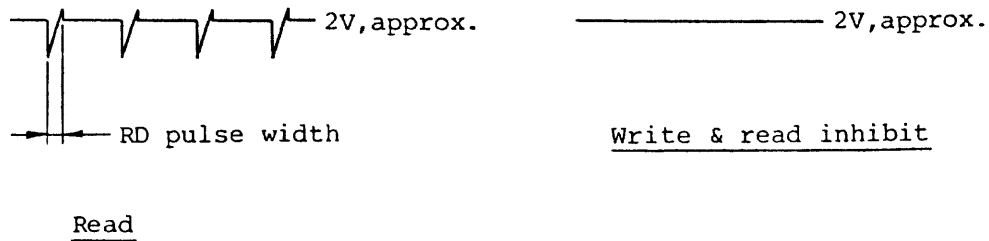
(4) Write circuit

(a) COM0 (pin 21), COM1 (pin 19)

   Output terminals of the common driver. Two terminals are equipped
   for the side 0 and side 1 heads respectively.
   Refer to tables 303 and 304 as to the output voltage at each
   operating condition.

(b) EO0 (pin 24), EO1 (pin 22)

   Output terminals of the erase driver which is constructed with open
   collector NPN transistors. Two terminals are equipped. While the EG
   input terminal is HIGH level, one of the drivers which is selected

by the CS input terminal turns on (becomes LOW).
Refer to Table 304.

(c) WCS0 (pin 26), WCS1 (pin 25)

External resistor terminals for setting the write current. Following
shows the circuit diagram of the terminal. By the pull up resistors
for the WCS0 and WCS1, the write current is determined. The current
is calculated by the expression in item 3-2-1-1 (2).
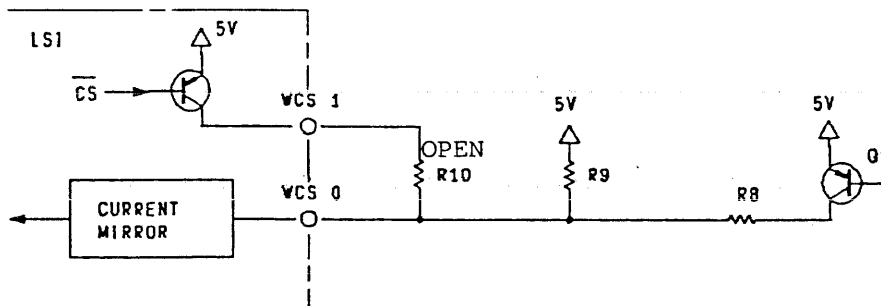
(d) WT (pin 17), pin 18)

External resistor terminals for the head termination in write operat-
ion. An appropriate value of resistor is connected externally not
to occur the abnormal overshoot nor undershoot at write operation.
These terminals are also used for the asymmetry adjustment at read
operation

11V,approx.   ─────────────────12V,approx.

WRITE DATA interval   Read
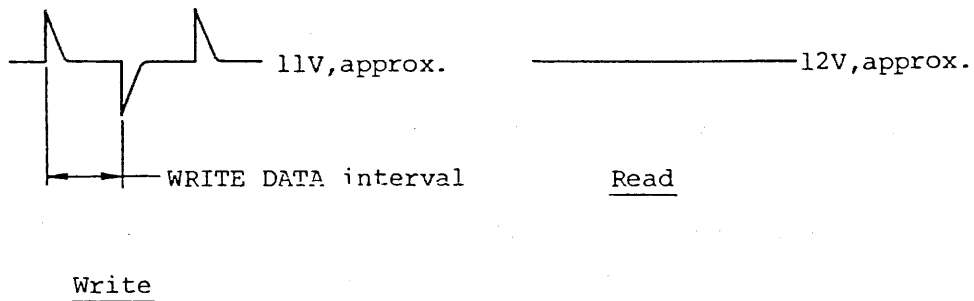
Write

(e) CD (pin 36)

In order to protect the head from undersirable magnetization, this terminal is used to set the delay time to keep the write current flow at a determined direction for 1 through 5μs, approx., after the completion of a write operation (WG turns off).
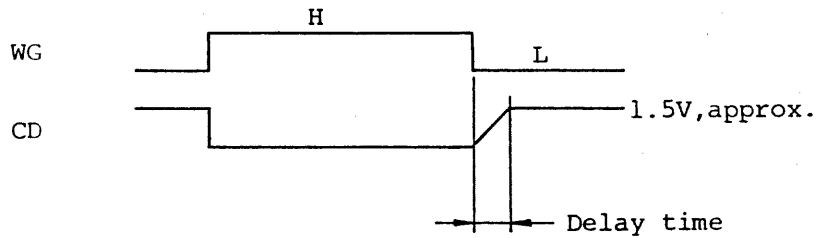
(f) $\overline{CS}$ (pin 27) --- Schmitt TTL input

Control input terminal having following two functions. (Refer to Table 304).

i) ON/OFF control of write current setting terminal WCS1.
ii) Selection of erase driver output terminals EO0 and EO1.

(g) $\overline{WD}$ (pin 28) --- Schmitt TTL input

WRITE DATA input terminal from the host controller.

Write   Read

(h) WG (pin 29), EG (pin 30) --- Schmitt TTL input

Control input terminals for write permit (WG) and erase permit (EG) from the control circuit in the FDD. Refer to Tables 304 and 305.

(5) Others

(a) $\overline{\text{S1}}$ (pin 31) --- Schmitt TTL input

SIDE ONE SELECT input terminal from the host controller.
The terminal functions as the selector for common driver outputs
COM0/COM1 and for head switch matrix of RW00,01/RW 10,11 terminals.
Refer to Table 304.

(b) $\overline{\text{LVS}}$ (pin 32) --- Open collector TTL output

$\overline{\text{LVS}}$ signal output terminal to the control circuit of the FDD. Refer
to item 3-2-1-4.

(c) OINV (pin 35), $\overline{\text{DS}}$ (pin 34) --- TTL input

Control input terminal of RD output. Refer to Tables 302 and 304.

(d) AGND (pin 16), EGND (pin 23), and DGND (pin 38)

0V power terminals mainly for the following circuits in the LSI.

AGND: Analog operation circuits such as pre-amplifier.
EGND: Erase driver.
DGND: Digital operation circuits such as write control logic.

(e) AVGG (pin 8), DVGG (pin 41), LVGG (pin 37)

+5V power terminals mainly for the following circuits in the LSI.

AVGG: Analog operation circuits such as pre-amplifier.
AVGG: Digital operation circuits such as write control logic.
LVGG: Low voltage sensor (LVS1).

(f) EVCC (pin 20)

+12V power terminal.

	Inputs						Outputs						Write
	WG	EG	$\overline{S1}$	$\overline{CS}$	$\overline{DS}$	OINV	$\overline{LVS}$	COM0	COM1	EO0	EO1	RD	current
R	L	L	H	–	L	L	H	R	0	Z	Z	N	0
e	L	L	L	–	L	L	H	0	R	Z	Z	N	0
a	L	L	–	–	H	L	H			Z	Z	Z	0
d	L	L	H	–	–	H	H	R	0	Z	Z	P	0
	L	L	L	–	–	H	H	0	R	Z	Z	P	0
W	H	L	H	H	–	–	H	Hi	0	Z	Z	F	WCS 0
r	L	H	H	H	–	–	H	Hi	0	0	Z	F	0
i	H	H	H	H	–	–	H	Hi	0	0	Z	F	WCS 0
t	H	L	L	H	–	–	H	0	Hi	Z	Z	F	WCS 0
e	L	H	L	H	–	–	H	0	Hi	0	Z	F	0
/	H	H	L	H	–	–	H	0	Hi	0	Z	F	WCS 0
E	H	L	H	L	–	–	H	Hi	0	Z	Z	F	WCS 0+1
r	L	H	H	L	–	–	H	Hi	0	Z	0	F	0
a	H	H	H	L	–	–	H	Hi	0	Z	0	F	WCS 0+1
s	H	L	L	L	–	–	H	0	Hi	Z	Z	F	WCS 0+1
e	L	H	L	L	–	–	H	0	Hi	Z	0	F	0
	H	H	L	L	–	–	H	0	Hi	Z	0	F	WCS 0+1
LV	–	–	–	–	–	–	L	0	0	Z	Z	Z	0

L: Logic level 0 (LOW)   R: COM voltage, 2.7V, approx.

H: Logic level 1 (HIGH)   P: Positive pulse

Z: High impedance (OPEN)   N: Negative pulse

Hi: COM voltage, 11.5V, approx. F: FALSE (No pulse output)

LV: Low voltage

(Table 304) Read write LSI control table

3-2-2. Control Circuit

The control circuit consists of strap circuit, LED & head load control circuit, write/erase control circuit, motor on gate, ready detector, stepping motor control circuit, track counter, disk change circuit, interface driver, etc.

Almost all the circuits except for drivers are enclosed in the control LSI, U3. Since the LSI is a CMOS type, input current is very small (less than ±1µA) and a protective register is serially inserted in the input terminal.

Fig.308 shows the block diagram.

(Fig.308) Block diagram of control circuit

3-2-2-1. Strap circuit

    In order to select the various function by users, various strap
    posts are available. Refer to the Specification items 1-11 and 1-12
    as to the details of strap function.
    Some models have not strap posts. These models have soldered jumping
    wires instead of the strap posts, and the function is fixed. (Refer
    to the version table in the schematic diagram).

3-2-2-2. LED and head load control circuit

    The circuits consists of LED/Head load gate, overdrive timer 1, LED
    driver, solenoid driver, and overdrive circuit 1.

(1) LED/Head load gate

    To the LED/Head load gate in the control LSI, U3, DRIVE SELECT ($\overline{\text{DSEL}}$)
    and IN USE ($\overline{\text{IU}}$)/HEAD LOAD ($\overline{\text{IHL}}$) signals are input.
    According to the selected function designated by the straps U1 (US1
    signal) and U2 (US2 signal), these input signals are gated to output
    to the LED driver and the solenoid driver as $\overline{\text{DLED}}$ and HLC signals.

(a) $\overline{\text{DLED}}$ signal

    A signal to turn on the front bezel indicator (LED).
    While this signal is LOW level, the LED turns on.

Strap setting		U3 input		LED on condition ($\overline{\text{DLED}}$ LOW)
U1	U2	US1	US2	(No relation to HL strap & $\overline{\text{IHL}}$ input)
OFF	OFF	L	L	$\overline{\text{IU}}$ (L) + $\overline{\text{DSEL}}$ (L)
OFF	ON	L	H	$\overline{\text{IU}}$ (L) + $\overline{\text{DSEL}}$ (L)
ON	OFF	H	L	$\overline{\text{IU}}$ (L)
ON	ON	H	H	$\overline{\text{IU}}$ (L) + $\overline{\text{DSEL}}$ (L) x RDYO (H)

        RDYO: U3, Ready detector output signal. HIGH in ready.

        (Table 305) LED turn-on condition

(b) HLC signal

    A signal to activate the solenoid for the models with head load
    solenoid. While this signal is LOW level, the solenoid is activated.

Strap setting			U3 input			Solenoid on condition (HLS $\overline{\text{HIGH}}$)
U1	U2	HL	US1	US2	$\overline{\text{IHL}}$	(No relation to IU strap & $\overline{\text{IU}}$ input)
OFF	OFF	OFF	L	L	L	$\overline{\text{DSEL}}$ (L) x PRDY --- No.1
OFF	OFF	ON	L	L	L/H	$\overline{\text{DSEL}}$ (L) x $\overline{\text{IHL}}$ (L) x PRDY --- No.2
OFF	ON	OFF	L	H	L	PRDY --- No.3
OFF	ON	ON	L	H	L/H	$\overline{\text{IHL}}$ (L) x PRDY --- No.4
ON	OFF	OFF	H	L	L	The same as No.1
ON	OFF	ON	H	L	L/H	The same as No.2
ON	ON	OFF	H	H	L	The same as No.1
ON	ON	ON	H	H	L/H	The same as No.2

Note: PRDY= RDYO (see Table 305) + Pre-ready

Pre-ready: Internal signal of LSI. It becomes TRUE before
one rotation of the disk (one INDEX pulse)

(Table 306) Solenoid drive condition

(2) LED driver

$\overline{\text{DLED}}$ signal from the control LSI, U3 is inverted and is input to the
driver IC, U7. U7 is constructed with NPN transistor array (open
collector output). Refer to Fig.309.

(3) Solenoid driver

The HLC signal from the control LSI, U3 with a pull up resistor of
1KΩ is supplied to the driver IC, U7. Refer to Fig.309 as to the
construction of U7.

(4) Overdrive timer 1

The HLC signal is also supplied to the overdrive timer in the control
LSI. The overdrive timer is constructed with a retriggerable counter.
For the initial 26msec of the solenoid activation, it maintains the $\overline{\text{HOD}}$
output (open drain) LOW level.
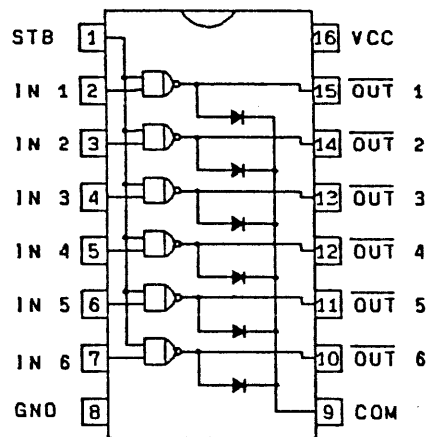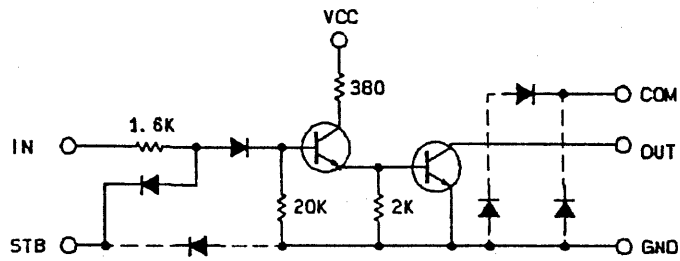
(Fig.309) Construction of driver IC, U7

(5) Overdrive circuit 1

The $\overline{HOD}$ signal is input to the PNP transistor Q5 which constructs the overdrive circuit 1 and it makes Q5 turn on while the signal is LOW level. +12V power is applied to the solenoid at that time to execute the drawing-in action of the solenoid securely.

After the overdrive period, the solenoid maintains its situation with +5V power through the diode CR1 to save the power.

In some models, overdrive function is not equipped with shorting the emitter-collector of Q5. In such a model, +12V is always supplied to the solenoid.

HLC input

$\overline{\text{HOD}}$ output ———————————————————— 12V,approx.

Applied voltage
to solenoid coil ——————————— 11V,approx.
                                          ————— 4V,approx.
                                          ———— 0V

|—26ms—|
  approx. |——Overdrive period
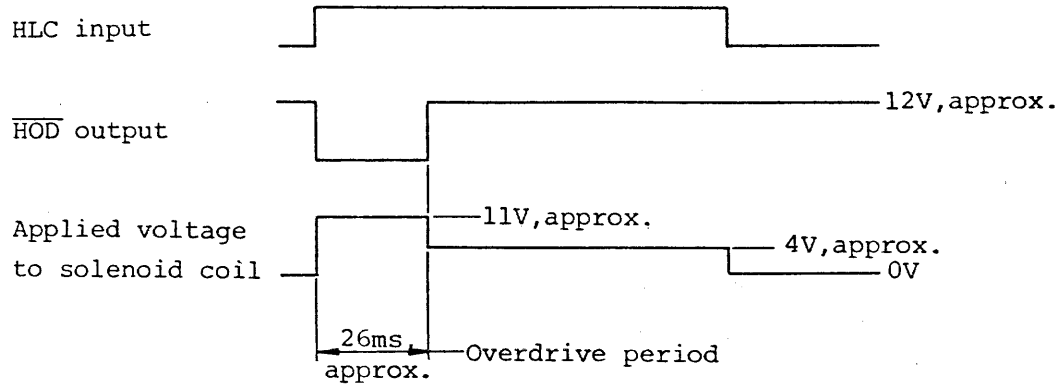
(Fig.310) Overdrive timing of head load solenoid

3-2-2-3. Write/erase control circuit

The circuit consists of write/erase gate and erase timer. Most of the parts of the circuit are enclosed in the control LSI, U3.

(1) Write/erase gate

The gate judges whether new data can be written on an installed disk. If it can be, the circuit supplies the WG signal for the read write LSI and erase timer.
The WG signal becomes TRUE in the following condition. The conditions are different depending on each LSI No.

(a) Control LSI No.: 2206-00 LH5060 or LH5060A

$WG = \overline{DSEL}(L) \times \overline{IWG}(L) \times \overline{FPT}(L) \times \overline{MON\ delay\ 1} \times \overline{SEEK}$

(b) Control LSI: 2206-00 LH5060B

$WG = \overline{DSEL}(L) \times \overline{IWG}(L) \times \overline{FPT}(L)$

Notes   WG: Write operation at HIGH

$\overline{DSEL}$: DRIVE SELECT input signal LOW.

$\overline{IWG}$: WRITE GATE input signal LOW.

$\overline{FPT}$: File protect sensor output (FPT input of LSI) LOW.
The same as that the file protect sensor detects the write enable notch (light passing condition) of a disk which is equivalent to that the WPO output of LSI is HIGH.

$\overline{MON\ delay\ 1}$: Internal signal of LSI. 360 ∿ 380msec after a motor-on command. Refer to Fig.311.

$\overline{SEEK}$: Internal signal of LSI. The ehad is not under seek operation (not in 10 ∿ 12msec for 96tpi and 13 ∿ 15msec for 48tpi after the last step pulse).

(2) Erase timer

The circuit to make the WG signal delay from the write/erase gate as in Fig.306 to output the EG signal for the read write LSI. Refer to item 3-2-1-3.

Various delay time can be set by ER0 ∿ ER3 and SPED input terminals of the control LSI. Only the SPED terminal is used for selection of the FDD here.

FDD model	U3 input terminals				Erase delay	
	ER0	ER1	ER2	SPED	On-delay	Off-delay
A∿F model (300rpm)	H	L	L	L	250∿267μs	883∿900μs
G model (360rpm)	H	L	L	H	191∿200μs	541∿550μs

   Note: The figure in the above table is the calculated value
         excluding the tolerance of the oscillator.

   (Table 307) Erase delay control table

3-2-2-4. Motor on gate

The circuit, receiving a spindle motor-on command from the host
controller, supply the MC (motor control) signal to the spindle motor
servo circuit. The circuit consists of OR-gate, 123μs delay circuit
and auto-turn circuit which are enclosed in the control LSI, U3.

A motor-on command input to the $\overline{\text{MONO}}$ or $\overline{\text{MON1}}$ terminal is supplied to
123μs delay circuit via the OR-gate to be delayed for 123 ∿ 267μs.
The delay circuit eliminates the noises mixed onto the interface line
and protects the control circuit from erroneous operation.
The MC signal becomes TRUE in the following conditions.

MC=($\overline{\text{MONO}}$(L) + $\overline{\text{MON1}}$(L)) x 123μs delay x DISK

Notes   MC: Motor rotation at HIGH

$\overline{\text{MONO}}$: MOTOR ON input signal LOW

$\overline{\text{MON1}}$: Differs depending on PCB issue.

Issue A ∿ E: Fixed at FALSE (HIGH)

Issue F ∿ : $\overline{\text{DLED}}$ is low at ML strap is ON.

(Front bezel indicator is ON).

DISK: Normally fixed to TRUE (HIGH).

For optional FDDs with disk sensor, it becomes HIGH when
a disk is inserted.

The auto-turn circuit makes the spindle motor rotates automatically at
a disk insertion to improve the chucking accuracy. The circuit is set
by the information of a disk insertion from the disk sensor and file
protect sensor, and is reset at the detection of a ready state or more
than 10 seconds after the insertion. Even though the FDD becomes ready
state by a command from this circuit, the RDYO signal in item 3-2-2-5
maintains FALSE (LOW level).

3-2-2-5. Ready detector

Ready detector consists of 50% speed detector, ±6% speed detector, pre-ready latch, ready latch, MON delay circuit which are enclosed in the LSI, U3. In the block diagram, these circuits are shown as one block of ready detector.

The MC signal for controlling the spindle motor is input to the ready detector which enables the operation of all the above five circuits. As the motor speed increases, 50% speed detector operates first, and then pre-ready latch is set when the pulse interval becomes less than twice of the nominal condition (i.e., 50% of disk speed). Then ±6% speed detector starts its operation and sets the ready latch when the pulse interval at the $\overline{IDXS}$ terminal becomes within ±6% of the nominal condition. The ready latch is set when more than three index pulses are detected after the motor start. In the typical case, the motor speed reaches within ±6% of the rated speed when the next pulse is detected after the pre-ready state. The ready latch will be set at that time.

Operation modes of the two speed detectors are changed by the SPED signal and the index pulse interval will be detected appropriately for 360rpm (A ∿ F models) or 300rpm (G model).

On the other hand, the MON delay circuit generates two delay signals after the MC signal becomes TRUE. One of them is the MON delay 1 signal to be supplied to write/erase gate (360 ∿ 380msec delay) and the other is the MON delay 2 signal (380 ∿ 400msec delay). The MON delay 2 signal and the ready latch output coinciding through AND gate are output from the control LSI as the RDYO signal which indicates that the FDD is read/write ready state. Fig.311 shows the timing chart of ready detector. The RDYO signal goes TRUE in the following conditions.

RDYO = MC x ±6% speed x $\overline{MON\ delay\ 2}$

Notes   RDYO: Ready at HIGH

MC: MC signal to the spindle motor HIGH (motor rotates).

±6% speed: $\overline{\text{IDXS}}$ pulse interval is within ±6% of nominal value.

$\overline{\text{MON delay 2}}$: 380 ∿ 400ms after MC signal becomes HIGH.

MC(Motor on command)

400ms, Max.

Constant speed

Disk rotation speed

360rpm: 166.7ms
300rpm: 200ms   t

$\overline{\text{IDXS}}$(TP1)
(Index detection)

50% speed detection
in U3

2t, Max.

Pre-ready latch
in U3

Pre-ready

t±6%

Ready latch in U3

360∿380ms

MON delay 1 in U3

MON delay 2 in U3

380∿400ms

RDYO output

Ready

360rpm: 730ms, Max.
300rpm: 800ms, Max.

IDXO output

Motor on

Head load enable
(with solenoid model)
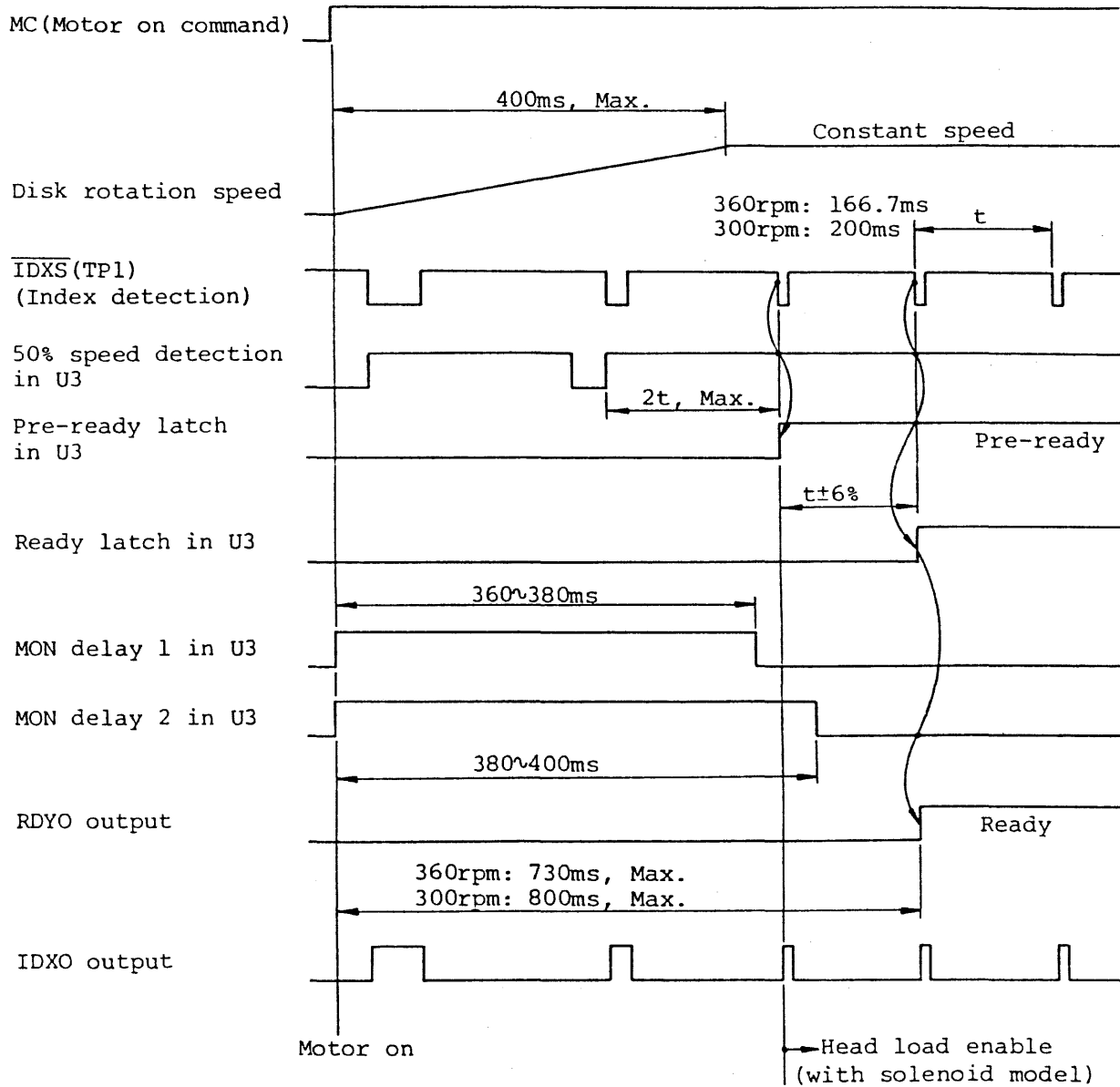
Note: 300rpm: A∿F models, 360rpm: G model

(Fig.311) Ready detector waveforms

All the five parts of ready detector are reset by the MC signal going
FALSE (LOW level).

3-2-2-6. Stepping motor control circuit

Stepping motor control circuit consists of direction latch, internal
step generator, shift register, phase drive selector, overdrive timer,
coil driver, and overdrive circuit.
All the above circuits except for the coil driver and overdrive circuit
are enclosed in the control LSI, U3. In the block diagram, all the
enclosed circuit in the control LSI except for the overdrive timer are
shown as one block of the stepper control circuit.

(1) Direction latch

At every input of the STEP ($\overline{ISTP}$) pulse from the host controller, the
direction latch samples and holds the head seek direction designated
by the DIRECTION SELECT ($\overline{IDIR}$) signal. The latched output is supplied
to the bi-directional shift register and changes the activating order
of the stepping motor coil as shown in Fig.312.

(2) Internal step generator

The circuit has following purposes.

(a) The circuit generates an internal step pulse 3msec approx. later from
    the STEP ($\overline{ISTP}$) input pulse. This function is executed only when
    the signal level at the TRK terminal is LOW (48tpi mode). When the
    TRK is HIGH (96tpi mode or 48tpi mode with a stepping motor of 3.6°
    for one step), it is not executed.
    When the TRK is HIGH level, the stepping motor rotates for one step
    space in response to one STEP pulse. When it is LOW level, the stepping
    motor rotates for two step space (3.6°) in response to one STEP pulse.

(b) When the RE strap for auto-recalibration is ON (PCB issue F and later)
    and the control LSI No. is 2206-00 LH5060A or 5060B, step pulses for

auto-recalibration are generated at every 3msec, approx.

The auto-recalibration starts when the FDD is powered on and the $\overline{\text{LVS}}$ signal from the read write LSI is changed from LOW to HIGH, and continues until the detection of the track 00.

The maximum time required for auto-recalibration is 255msec.

During the execution of the auto-recalibration, the FDD maintains NOT-ready state (RDYO output LOW) and the STEP ($\overline{\text{ISTP}}$) pulse input from the host controller is ignored.

(3) Shift register and phase drive selector

Step pulse and the output of the direction latch are supplied to the shift register and the phase drive selector to be converted to the appropriate timing signals for the uni-polar 1-2 phase drive of the 4-phase stepping motor. These phase drive signals are output from the control LSI and supplied to the coil driver.

In order to improve the torque margin in the seek operation, partial 2-phase drive period is provided by the phase drive selector only in the initial stage when the drive phase is changed. Refer to Fig.312 for timing chart.

(4) Coil driver

Four outputs, PA, PB, PNA, PNB from the control LSI, U3 are input to the coil driver which consists of a driver IC, U7. Refer to Fig.309 as to the construction of U7.

(5) Overdrive timer 2

External and internal step pulses are also supplied to the overdrive timer 2 in the LSI. The overdrive timer 2 is constructed with a retriggerable counter. During on-state of the timer (50msec, approx.), $\overline{\text{SOD}}$ output (open drain) from the LSI becomes LOW level. Refer to Fig.313.

DIRECTION SELECT (J1-18, $\overline{\text{IDIR}}$)   Step-out   Step-in

$\overline{\text{STEP}}$ (J1-20, $\overline{\text{ISTP}}$)

Direction latch in U3

96tpi (or 48tpi, 3.6°):

    Internal step gen. in U3   50ms, approx.

    $\overline{\text{SOD}}$ (Overdrive timer 2)   Overdrive operation
    output

    Coil driver input

        PA

        PB

        PNA

        PNB

        t1   t2

48tpi: 50ms, approx.

                Internal step
                delay (3ms, approx)
    Internal step gen. in U3

    $\overline{\text{SOD}}$ (Overdrive timer 2)
    output

    Coil driver input

        PA

        PB

        PNB

        PNB

        t1   t1

           t2   t2
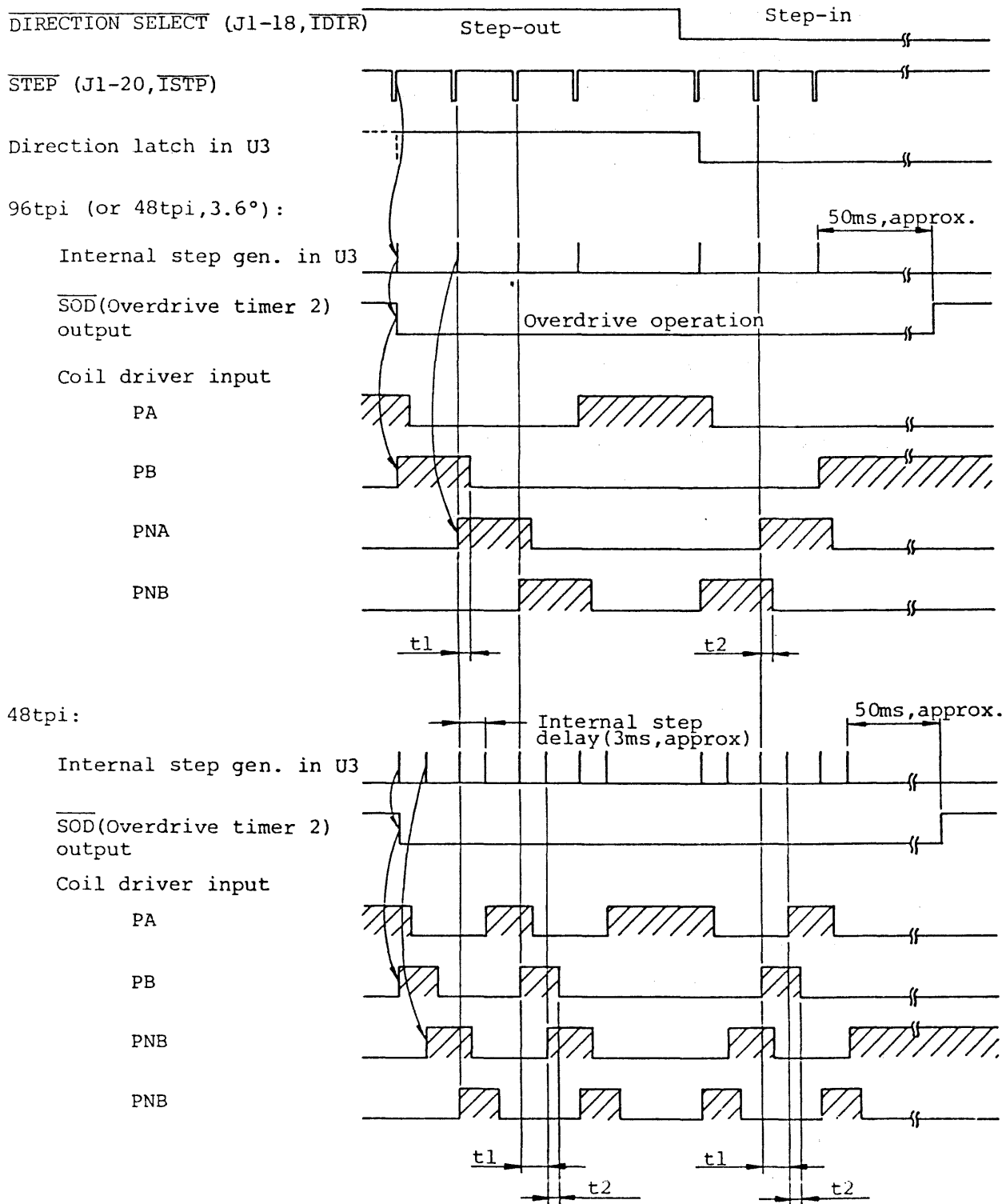
t1: Internal step delay (3msec, approx.)
t2: Partial 2-phase activating period (0.6ms, approx.)

(Fig.312) Stepping motor control circuit waveform

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Final internal step pulse      ⎍
in  U3                     ___⎏ ⎏_____

___                        ___        _____ 12V,approx.
SOD output                    ⎏_____⎰
                           ____⎏

                               _____
Applied voltage to motor   ___⎰           ⎏_____ 11V,approx.
coils                        ⎸             ⎸⎏_____ 4V,approx.
                           __⎸__-__-__-__⎸_⎸___-__-__-__ 0V
                             ⎸  50ms, approx. ⎸
                             ⎸←─────────────→⎸
                                Overdrive period
```
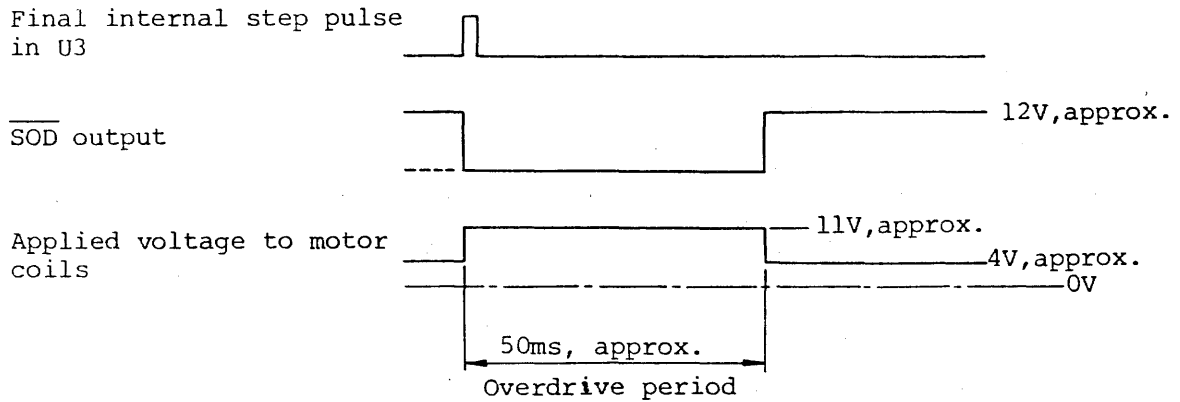
(Fig.313) Stepping motor overdrive timing

(6) Overdrive circuit 2

The $\overline{SOD}$ signal is input to the PNP transistor Q6 which constructs the
overdrive circuit 2 and it makes Q6 turn on during LOW level. At that
time +12V power is applied to the stepping motor coils to execute
the seek and settling operations securely with high torque.
After the completion of the settling, only +5V power is supplied to the
coils through the diode, CR3 which minimize the power loss by supplying
only the required torque for holding the stop position. By the above
design, heat radiation is decreased to the minimum level and the power
consumption of the stepping motor in seek stop is only 0.25W, approx.

3-2-2-7. Track counter

Track counter memorizes the track position and outputs track switch (SP) signal for the read write circuit. It also outputs TOO (TRACK 00) signal to the host controller. All the circuits are enclosed in the control LSI, U3. The function of this circuit is used only in 96tpi models. Refer to item 3-2-1-1.

The output signal from the track 00 sensor (TP3) is supplied to TOS terminal of the LSI and is output as the TOO signal through the gate in the track counter. The TOO signal becomes TRUE in the following conditions.

TOO= TOS x Step out x PA

Notes   TOO: Track 00 detected at HIGH.

            TOS: Track 00 sensor output at TP3 (TOS input of LSI) is HIGH. Track 00 sensor detects the light disturbing wing of the head carriage (track 00 position).

            Step out: Direction latch output in item 3-2-2-6 is step-out direction.

            PA: PA output from stepping motor control circuit is HIGH. Phase A coil of the motor is activated.

When the TOO signal becomes TRUE (HIGH level), the track counters constructed from up-down counters are reset. If a step-in operation is executed, the counter steps up and the SF output changes to LOW at 44th track. Refer to item 3-2-1-1 as to the function of the SF signal.

    Track 00 ∿ 43: SF signal HIGH.
    Track 44 ∿ 79: SF signal LOW.

3-2-2-8. Other terminals and function of control LSI

Following explains other terminals and function of the control LSI, U3.

(1) APS output terminal

APS signal becomes TRUE (HIGH level) in the following conditions.
The signal is used to inhibit the RD output pulse in some optional
models.

APS= MON delay 1 + SEEK
Notes   MON delay 1: Internal signal of LSI. Spindle motor is under
                     starting operation. (See Fig.311).
         SEEK: Internal signal of LSI. The head is under seek operation
               (10 ∿ 12msec for 96tpi and 13 ∿ 15msec for 48tpi after
               the last step pulse).

(2) OSCI, OSCO terminals and clock generator

It supplies clocks for operation to all the circuits in the LSI by
external ceramic oscillator.

(3) $\overline{LVS}$ input terminal

$\overline{LVS}$ signal input terminal from the read write LSI.
When it is LOW, all the circuits in the control LSI are reset.

(4) OINV input terminal

Terminal to invert the level of the control LSI output signals which
are used as output signals to the host controller. The terminal is
fixed to HIGH level in this FDD and HIGH output is TRUE.

(5) PSE 1 input terminal

Input terminal for power save control.

This function is not used in this FDD and it is fixed to HIGH level.

(6) SPC output terminal

Output terminal for power save control.

This function is not used in this FDD (open condition).

(7) MCK output/RE input terminal

  (a) LSI No. 2206-00 LH5060: MCK output terminal. Not used, open.

  (b) LSI No. 2206-00 LH5060A or 5060B: RE input terminal

                         Execute auto-recalibration at LOW level.

(8) $\overline{\text{DCR}}$, DCDO terminals and disk change circuit

Disk change circuit generates DISK CHANGE signal which indicates that the disk is removed from the FDD. It is used only in some optional models with disk sensor.

When a disk is removed, the DISK signal from the disk sensor becomes LOW level and sets the flip-flop in the disk change circuit. This is the disk change state and the DCDO output becomes HIGH. If a disk is inserted again and the $\overline{\text{DCR}}$ terminal is pulsed during the LOW level of the DSEL (DRIVE SELECT) signal, the flip-flop is reset to make the DCDO output return to LOW level. Since $\overline{\text{DCR}}$ terminal is connected with $\overline{\text{ISTP}}$ terminal on the PCB, it is reset by the STEP pulse from the host controller.

3-2-2-9. Interface driver

Output signals from the read write LSI and control LSI are supplied to
the host controller via the interface driver. AND gates of the inter-
face driver makes these output signals to the host controller valid
only when the DRIVE SELECT input signal is TRUE (LOW level).
As to the INDEX and the READ DATA interface signals, there are some
types of output condition. In one of the types, signals from the LSI
are output as they are. In another type, they are output only when the
FDD is in ready state by means of ANDing with RDYO signal.

The interface driver used in this FDD differs as follows depending on
the PCB issue No. There are no difference in the construction of
open collector, sink current capability, and electric characteristics.

(a) PCB issue A ∿ E: TTL7438
(b) PCB issue F and later: M52803 (Refer to Fig.314)

(Fig.314) Construction of interface driver, M52803

3-2-3. Servo Circuit

There are two types of rotational speed which are 300rpm for A ∿ F models and 360rpm for G model. The start and stop of the rotation is controlled by the MC signal through the motor on gate in the control LSI.

The servo circuit aims to maintain the rotational speed of the spindle motor at a determined constant speed, and the circuit is mounted on the PCBA assembled with the spindle motor.
The spindle motor is a long life DC brushless motor having 3-phase coils and bi-polar drive system. The coils are driven by the exclusive servo IC. Energization and magnetized direction of the coils are controlled by the signal from the hall elements mounted on the servo PCBA around the rotor so that they are changed corresponding to the designated rotational direction.
The rotational speed is maintained stably and precisely. The feedback signal from the AC tacho-meter in the rotor is converted into the drive voltage (F-V conversion) by servo IC, and applied to the drive coils through the phase compensation circuit.

Several manufacturers' spindle motors are sued in FD-55V series for the stable supply of the motor. Though these motors are almost the same in the function and performance, they are different in external view because of a little difference in the servo circuit, etc.

3-3. FUNCTION OF TEST POINTS AND VARIABLE RESISTORS

Following shows the mounting position of the test points and variable
resistors.
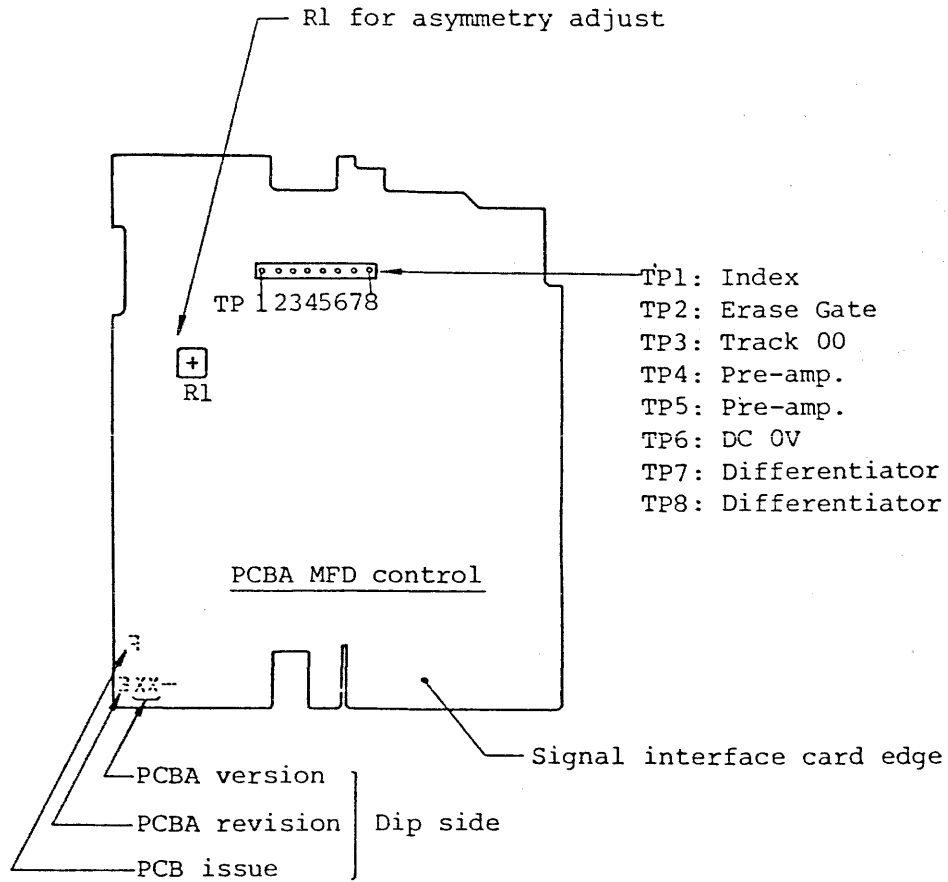
(Fig.315) Location of test points and variable resistors

3-3-1. Function of Test Points

Eight test points (one for ground) are equipped on the PCBA MFD control #H for the check and adjustment of the waveforms of the FDD.

(1) TP1 (Index)

Test point to observe the output of the index detection photo-transistor. When the index hole is detected, LOW going pulse is observed. The photo-transistor is mounted on the PCBA front OPT #H and the LED is mounted on the DD motor (spindle motor) Ass'y.

The test point is used for the following purposes.

(a) Confirmation of the disk rotational speed.

(b) Rough confirmation and adjustment of the index burst detection timing. Burst timing is adjusted by the fixing screws of the PCBA front OPT #H. (Use INDEX interface signal for precise confirmation and adjustment).

TP1 (Index)

Index interval   Pulse width
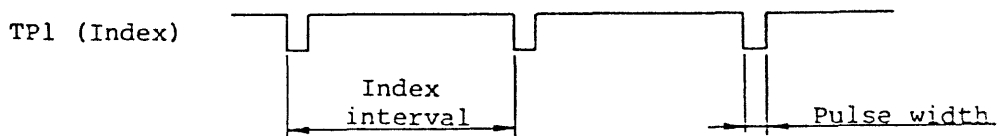
(Fig.316) Typical waveform of TP1 (Speed observation)

TP1 (Index)

TP4 or 5
(Pre-amp. output)
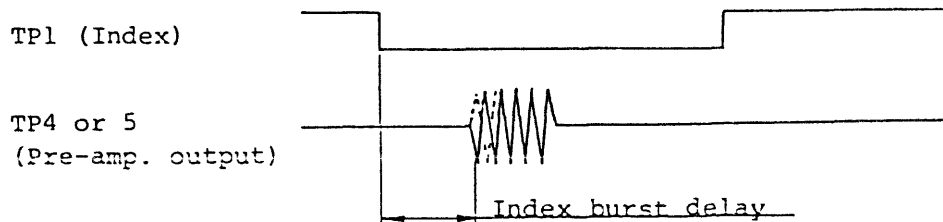
Index burst delay

(Fig.317) Typical waveform of TP1
(Rough observation of burst timing)

Items	Models	
	A~F models	G model
Index interval	200 ± 3ms	166.7 ± 2.5ms
Pulse width	2 ~ 5.5ms	1 ~ 8ms
Burst delay	200 ± 200μs	165 ± 165μs

(Table 308) Index timing

(2) TP2 (Erase gate)

Test point to observe the output of the erase gate.

When TP2 is HIGH level, erase current flows through the erase head.

This TP is used for the check of the required delay time of the erase

gate signal against the WRITE GATE input signal.
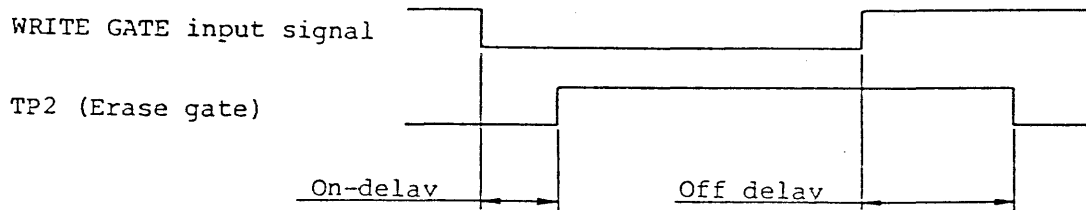
(Fig.318) Typical waveform of TP2

Delay	Models	
	A~F models	G model
On-delay	200 ~ 320μs	175 ~ 210μs
Off-delay	860 ~ 950μs	500 ~ 560μs

(Table 309) Erase gate delay

(3) TP3 (Track 00 sensor)

Test point to observe the output of the track 00 detection photo-

transistor.

The signal level at this TP is opposite to that of the TRACK 00 output
signal. When the head is on track 00 or around track 00 position, TP3
becomes HIGH level.

The voltage of TP3 should be more than 4V at track 00 and less than 0.5V
at track 04 (96tpi) or at track 02 (48tpi).

TP3 (Track 00 sensor)

4.0V, Min.

0.5V, Max.

Track 04 (96tpi)
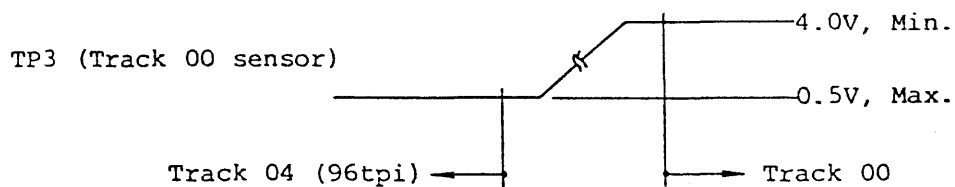
Track 00

(Fig.319) Typical waveform of TP3

Note: The TRACK 00 output signal goes TRUE (LOW level) only when the
phase A coil of the stepping motor is energized and the direction
latch is set to the step-out direction. Therefore, the level
change timing of the TRACK 00 signal is not consistent with that
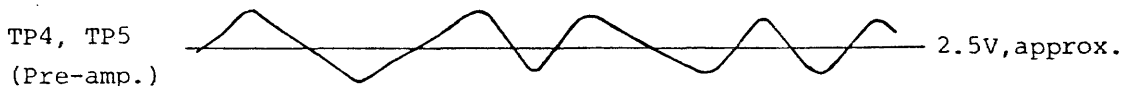of the TP3 signal.

(4) TP4, TP5 (Pre-amplifier)

Test point to observe the read pre-amplifier output signals.
The pre-amplifier has two outputs of the order of several dozen to
several hundred mVp-p, and they differ in phase by 180° (opposite phase).
Both outputs are observed at TP4 and TP5 respectively.
For an accurate observation of the read waveforms, use two channels of
an oscilloscope with one channel set to Invert mode and Add both
channels. Use TP6 (0V) test point for the oscilloscope ground.
TP4 and TP5 are used for checking various characteristics of the
read/write head and also for the check and adjustment of the head seek
mechanism such as track alignment.

TP4, TP5
(Pre-amp.) ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 2.5V, approx.

(Fig.320) Typical waveform of TP4 and TP5

(5) TP7, TP8 (Differentiation amplifier)

Test points to observe the differentiation amplifier output signals.

Like the pre-amplifier, the differentiation amplifier also has two

outputs of the order of several hundred mVp-p to several Vp-p which

differ in phase by 180°. Both outputs are observed at TP7 and TP8

respectively.

For an accurate observation of the waveforms, use two channels of the

oscilloscope with one channel set to Invert mode and Add both channels.

Use TP6 (0V) test point for the oscilloscope ground.

TP7 and TP8 are used for checking the total operation of the read/write

head and the read amplifier and for the check and adjustment of the head

seek mechanism such as track alignment.

TP7, TP8
(Differentiator) ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 2.5V,
approx.
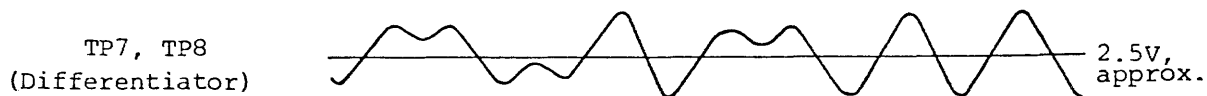
(Fig.321) Typical waveform of TP7 and TP8

(6) TP6 (0V)

It is used as the ground terminal for measurement equipment. Be sure

to use a small size clip to obtain a probe ground of the equipment.

3-3-2. Function of Variable Resistor

On the PCBA MFD control #H, following variable resistor is mounted. The variable resistor is correctly adjusted before the shipment of the FDD and fundamentally it shall not be readjusted except for by a trained technicians.

(1) R1 (for asymmetry adjustment)

Variable resistor for adjusting the asymmetry of the read data pulse. Write 1F data and observe the pulse intervals at the READ DATA output line. Then adjust the variable resistor so that the read data asymmetry takes the minimum value. Repeat each adjustment alternately for side 0 and side 1 heads to obtain the minimum asymmetry for both sides.
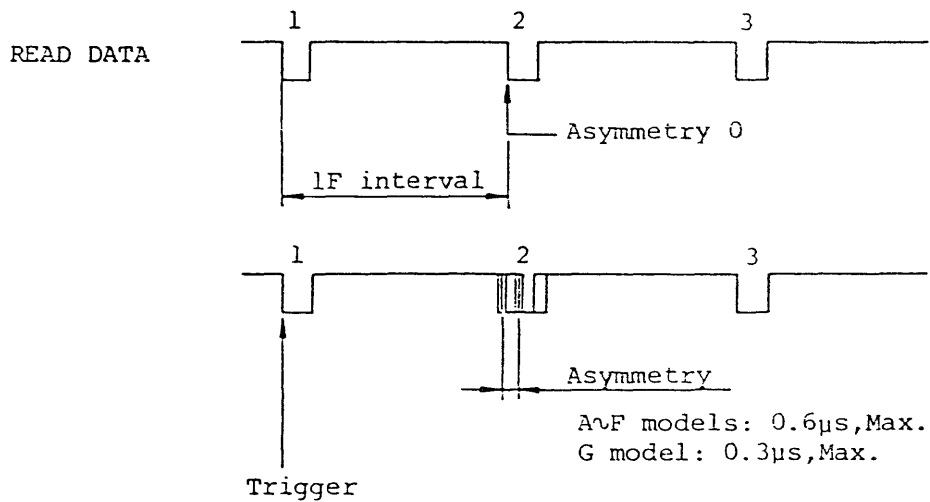
Note: When the READ DATA waveform is observed at the DOUT terminal of the SKA, positive going pulse is observed.

(Fig.322) Read data asymmetry

SECTION 4

MAINTENANCE

4-1. GENERAL

4-1-1. Periodic Maintenance

The FDD is designed to be free from periodic maintenance such as replacement of parts, grease-up, etc. when it is operated at a normal operation duty.

However, cleaning of the magnetic head using a cleaning disk is recommended since it is effective to improve the reliability of the data. If some of the parts in the FDD are operated at a specially heavy duty condition, or if the FDD is operated over 5 years, it is recommended to replace the wear parts according to Table 510 in item 5-5.

Periodic maintenance items	Recommended cycle	Required time	Referred items
Cleaning of magnetic head	Refer to 4-3	5 min.	4-3-1
Replacement of wear parts	Refer to 5-5 and 4-5.		

(Table 401) Periodic maintenance items

4-1-2. Check and Adjustment

.Table 402 shows all of the check and adjustment items.

Following items do not require periodic maintenance. Check and
adjustment should be done when required during replacement of the
maintenance parts or during trouble shooting referring to items 4-2
and 4-4.

The numbered procedure in Table 402 shows a typical procedure of the
general check and adjustment all over the FDD. After mechanical items
(steps 1 ∿ 4), electric performance items (steps 5 ∿ 15) should be
done.

Steps	Check and adjustment items	Required time	Referred items
1	Adjustment of set arm position	5 minutes	4-4-1
2	Check and adjustment of holder position	5 minutes	4-4-2
3	Check and adjustment of arm lifter (Model with head load solenoid)	5 minutes	4-4-3
4	Check of CSS Ass'y (CSS model)	5 minutes	4-4-4
5	Check of file protect sensor	5 minutes	4-4-5·
6	Check of disk rotational speed	5 minutes	4-4-6
7	Check of erase gate delay	5 minutes	4-4-7
8	Check and adjustment of head touch	5 minutes	4-4-8
9	Check and adjustment of asymmetry	5 minutes	4-4-9
10	Check of read level	5 minutes	4-4-10
11	Check of resolution	5 minutes	4-4-11
12	Check and adjustment of track alignment	10 minutes	4-4-12
13	Check and adjustment of track 00 sensor	5 minutes	4-4-13
14	Check and adjustment of track 00 stopper	5 minutes	4-4-14
15	Check and adjustment of index burst timing	5 minutes	4-4-15

(Table 402) Check and adjustment items

4-1-3. Maintenance Jigs and Tools

The following are the jigs and tools required for adequate maintenance of the FDD.

(1) Equipment

(A) When the Simulator KA (off-line exerciser, abbreviated to SKA) is used:

(a) SKA

SKA	Applied models
SKA-A ∿ F	FD-55AV ∿ FV
SKA-G (or SKA-GFII, G mode)	FD-55GV

(Table 403) SKA and applied models

Notes: 1. Though SKA-A ∿ F was simply called as SKA conventionally, they are distinguished as SKA A ∿ F here for convenience' sake. However, when the identification of each SKA model is not so important, all SKAs in table 403 are generally called as SKA in the following explanation.
2. SKAs in Table 403 can be used also for FD-55(L) series.

(b) Accessories for SKA

SKA needs the following accessories for operating the FD-55V series. The following accessories are common for all the V-series except for special models.

i) SKA/FDD interface cable #0 (P/N 15922337-00)
ii) Check cable #5 (P/N 15922611-00)
   SKA/FDD power cable is included in the check cable #5.

Note: SKAs for FD-55(L) series differ from those for FD-55V series only in the check cable.

(c) Oscilloscope (two channels)

(d) DC power supply (+12V, 1.2A and +5V, 2A) or SKA power supply. The following accessory is required for the power supply (The accessory is supplied with the SKA power supply).

    i) Power cable (4P)

(e) Thermometer and hygrometer

(B) When SKA is not used:

    (a) FDD controller and DC power supply (user's system)

    (b) Oscilloscope (two channels)

    (c) Frequency counter

    (d) DC clip-on ammeter

    (e) Thermometer and hygrometer

(2) Tools

    (a) Cross-point screwdrivers, M2.6 and M3

    (b) Common screwdriver, small size

    (c) Hexagon wrench key, 1.5mm

    (d) A pair of tweezers

    (e) Round nose pliers

    (f) Cutting pliers

    (g) Solder and soldering iron

    (h) Cutter knife

(3) Special jigs

(a) Max. media jig for adjustment (Jig C, P/N 17890746-00)

(b) Max. media jig for check (Jig E, P/N 17890746-02)

(c) Alignment adjustment jig (P/N 17851100-00)

(4) Disks

(a) Work disk (commercially available disk)

    i) For Normal density (FD-55AV ∿ FV)

   ii) For High density (FD-55GV)

(b) Cleaning disk (commercially available cleaning disk)

    i) For single sided (FD-55AV, EV)

   ii) For double sided (FD-55BV, FV, GV)

(c) Level disk

    i) For Normal density (FD-55AV ∿ FV), P/N 14900015-00

   ii) For High density (FD-55GV), P/N 14900015-01

Note: Commercially available disks may be used if there is no doubt.

(d) Alignment disk

    i) For single sided, 48tpi (FD-55AV), P/N 14900016-00

   ii) For double sided, 48tpi (FD-55BV), P/N 14900016-21

  iii) For single sided, 96tpi (FD-55EV), P/N 14900016-23

  iv) For double sided, 96tpi (FD-55FV), P/N 14900016-24

   v) For High density, double sided, 96tpi (FD-55GV), P/N 14900016-25

(5) Other articles used during maintenance

(a) Absolute alcohol (Ethanol)

(b) Cotton swab or gauze

(c) Locking paint (Three Bond, 1401B)

(d) Screws and washers (Refer to item 5-2-2)

(e) Oil (Kantoh Kasei, FLOIL 464P, TEAC P/N 10854022)

(f) Grease (Kyodo Yushi, Multemp P2B, TEAC P/N 10857031)

Note: Be sure to use well calibrated equipment and disks.

4-2. PRECAUTIONS

4-2-1. Torque Applied to Screws and Locking Paint

  (1) The following torque should be applied to screws, unless otherwise specified.

Size of screws	Application	Torque
M2.6	Installation of track 00 sensor #H	3Kg.cm
M3	For general usage	6Kg.cm
M3	Installation of steel belt, PCBA front OPT #H, PCBA disk sensor	4.5Kg.cm
M3	Installation of air damper (option)	3Kg.cm
M3 setscrew	Installation of L-type front lever Ass'y (option)	4.5Kg.cm

(Table 404) Torque applied to screws

  (2) Apply fresh locking paint to the following designated points after tightening or adjusting the screw.

    (a) Installation screws of stepping motor: M3, 2 points
    (b) Adjustment screw of arm lifter
           (Only for models with head load solenoid): M3 setscrew
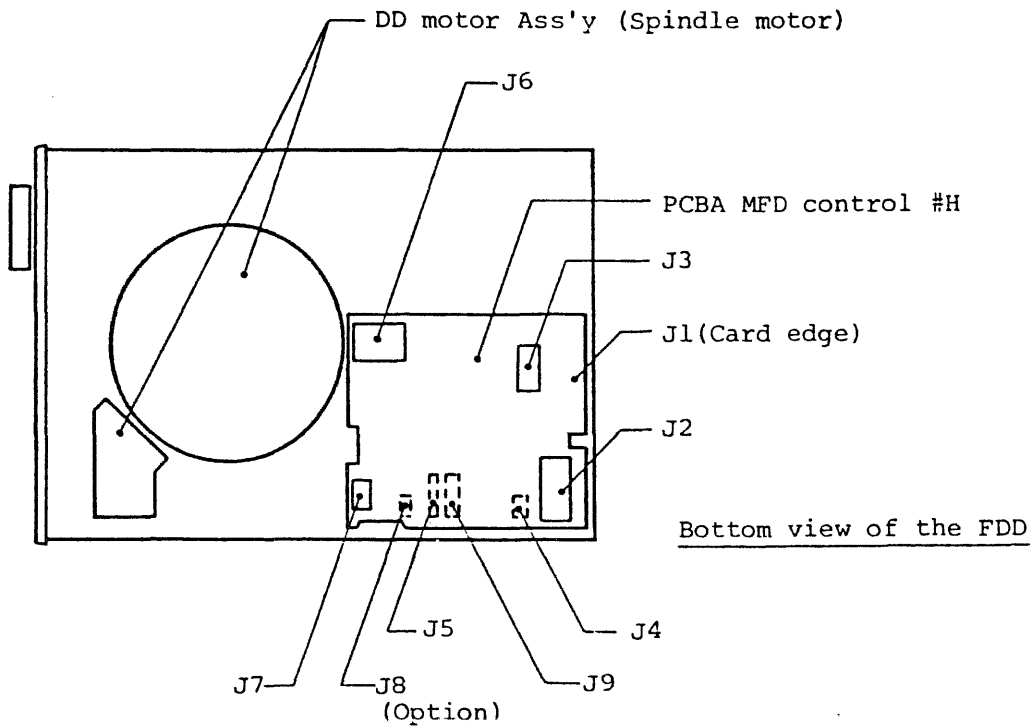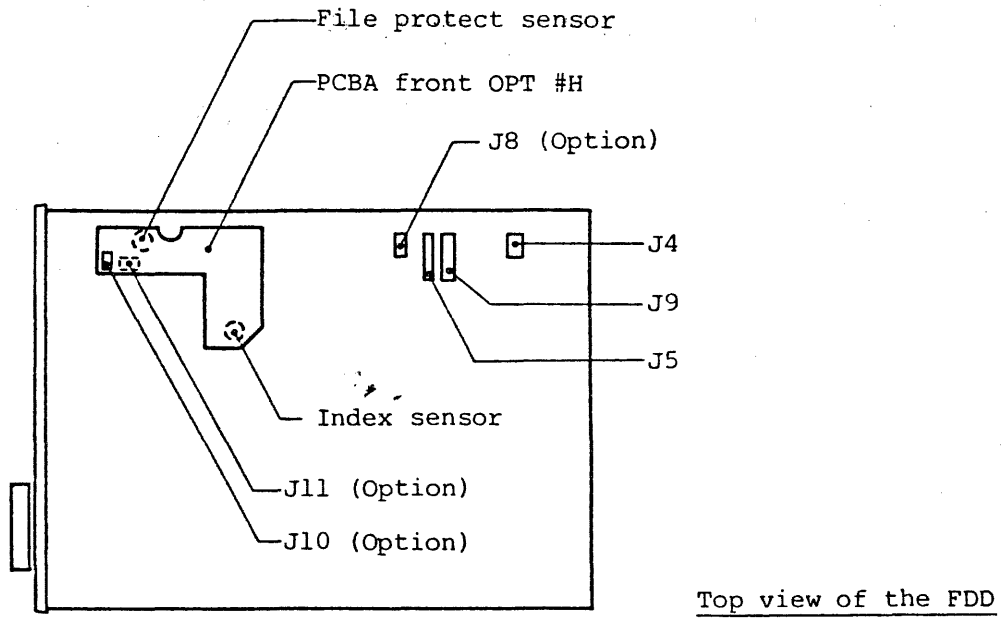   (c) Steel belt of V-type carriage: 4 points, refer to item 4-5-1.

  Note: Before applying the locking paint, remove old locking paint on the screw and around it.

4-2-2. Handling of Connectors

(1) Types of connectors

The following connectors are used in the FDD. Fig.401 shows the location.

(a) J1: Interface connector

(b) J2: Power connector

(c) J3: IC socket for terminator network
        (Some models are not equipped).

(d) J4: Head load solenoid & track 00 connector

(e) J5: PCBA front OPT #H connector

(f) J6: Stepping motor connector

(g) J7: Spindle motor (DD motor Ass'y) connector

(h) J8: (Option, Door close Ass'y or PCBA disk sensor connector)

(i) J9: Head connector

(j) J10: (Option, 1/1 size front bezel indicator connector)

(k) J11: (Option, Door lock solenoid connector)

File protect sensor

PCBA front OPT #H

J8 (Option)

J4

J9

J5

Index sensor

J11 (Option)

J10 (Option)

Top view of the FDD

DD motor Ass'y (Spindle motor)

J6

PCBA MFD control #H

J3

J1(Card edge)

J2

Bottom view of the FDD

J5

J7

J8
(Option)

J9

J4

(Fig.401) Types of connectors

(2) Connection and disconnection of the connectors

Be sure to turn the power off before connecting and disconnecting the connectors. Connection or disconnection should be done straightly and correctly without applying excessive force to the cables and the post pins.

(3) Precautions for handling the white or brown connectors (J6, J7, J11)

(a) Disconnection of the connector

As shown in Fig.402, carefully pull up the edges of the upper protruding area of the connector little by little with the finger nails or with a screwdriver.
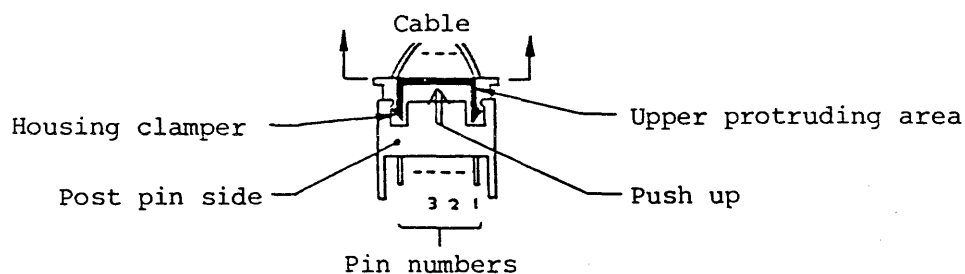
(Fig.402) Disconnection of white connector
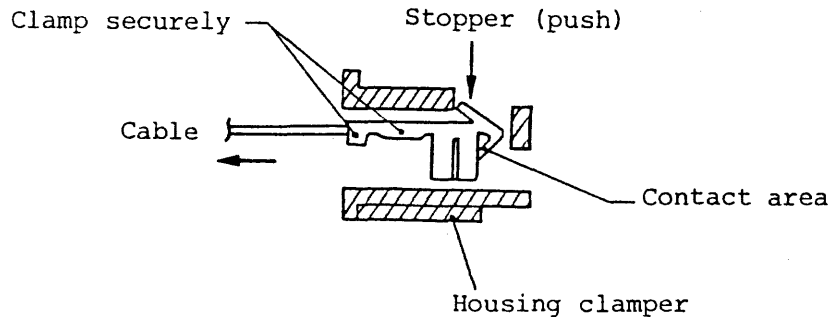
(b) Connection of the connector

Push the connector into the post pin on the PCBA with the housing clamper up.

(c) Removal of the pin (for reference)

Refer to Fig.403.
Depressing the stopper of the pin lightly with a narrow object such as a pair of tweezers, pull the cable in the direction indicated by

the arrow.

(Fig.403) Sectional view of white connectors

(d) Insertion of the pin (for reference)

Before insertion, check the following three points.

   i) Confirm that the sheath and the core of the cable are securely
      clamped.
  ii) Confirm that the stopper is lifted as in Fig.403 and it inhibits
      accidental removal.
 iii) No tarnish or contamination should be on the contact area of the
      pin or the PCB side post pin. If there is, remove it.

   Contact failure may happen if any of these three points is not
   satisfied.
   When you insert the pin, it should be so inserted that the stopper
   faces the opening side of the housing.
   After the insertion, check the connection by pulling the cable lightly.

(4) Precautions for handling the black connectors (J4, J5, J9, J10)

  (a) Disconnection of the connector

   Pull out slowly holding the housing with the fingers or a round nose

pliers. Be sure not to apply tension to the fine cables of the J9
(head connector).

(b) Connection of the connector

Make the polarizing key position of the housing correspond with the
lack of the post pin, and push the housing carefully with the fingers.

(c) Removal of the pin

Lifting up the stopper of the housing with a narrow object such as
cutter knife, pull the cable with a pair of tweezers in the direction
indicated by the arrow. Refer to Fig.404.
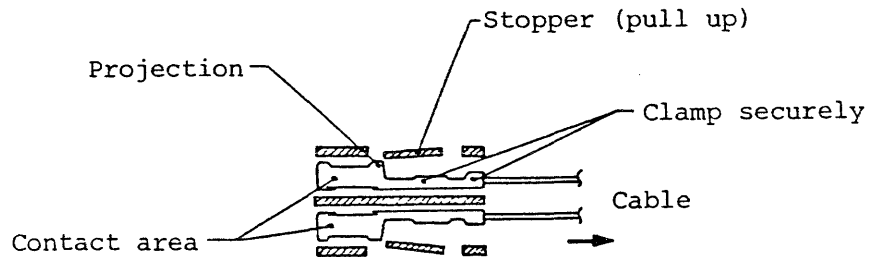
(Fig.404) Sectional view of black connectors

(d) Insertion of the pin

Before insertion, check the pins according to item (3)-(d), i)
through iii).
When you insert the pin, it should be so inserted that the projection
side faces the stopper of the housing. After the insertion, pull the
cable with a pair of tweezers softly in order to confirm whether is
is securely connected.

4-2-3. Head Cable Treatment

Head cable should be arrnaged correctly by the clampers with appropriate margin in length so that the head carriage can move on the guide shafts smoothly.

(1) Clamp the head cable with fixing point of the cable guide so that the cable has appropriate looseness when the head carriage is set to track 00 (rear end of the moving area) and that the cable does not touch the stepping motor and does not strike the bottom of the cable guide. The appropriate length of the head cable from the head carriage output to the fixing point of the cable guide is approximately 85mm.
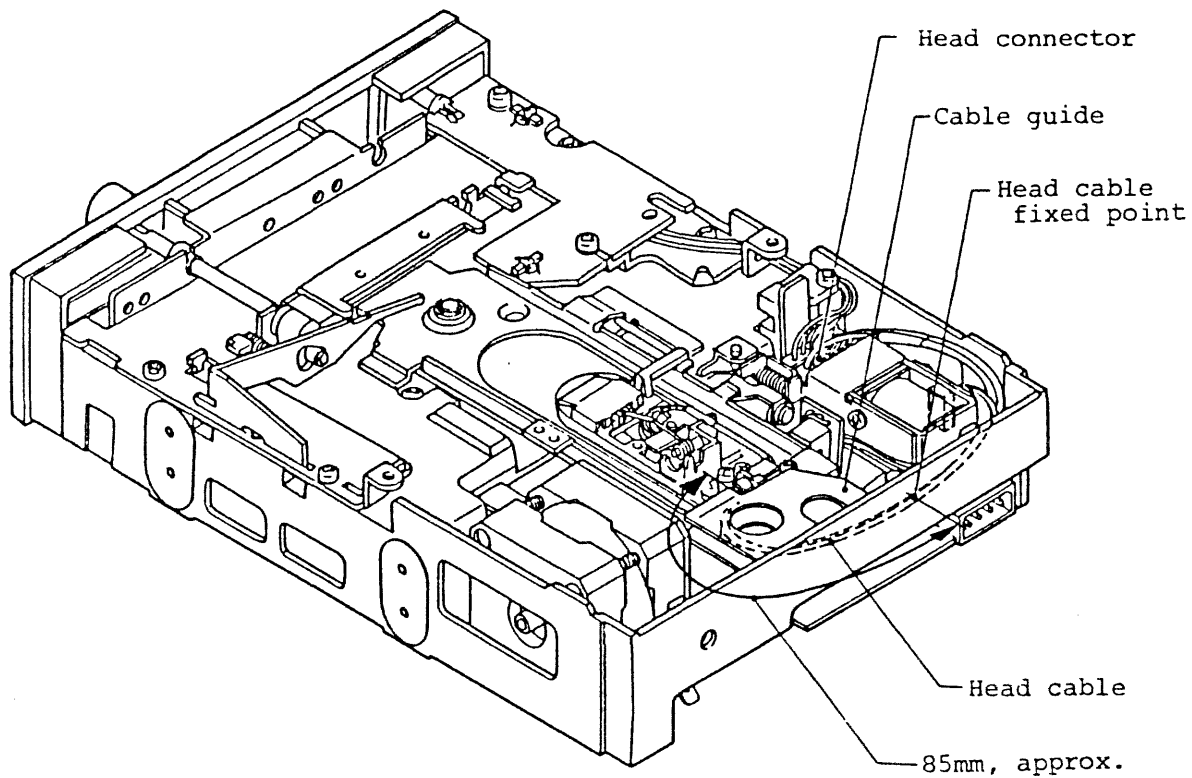
(Fig.405) Head cable arrangement

(2) Form the cable not to have excessive looseness in the area from the head connector to the cable guide.

4-2-4. Initial Setting of SKA-G and SKA

    Following initial setting is required for operating the SKA. Following
    setting is applied to all of the SKA-A ∿ F, SKA-G, and the SKA-GFII
    unless otherwise specified.

4-2-4-1. Cable connection and setting of power supply voltage

    (1) Set the output voltage of DC power supply to +12V and +5V, approx.

    (2) Turn the DC power off and connect the power cable to the PSA (SKA PWR)
        connector of the SKA.

    (3) Set the FD PWR switch of the SKA to the OFF position.
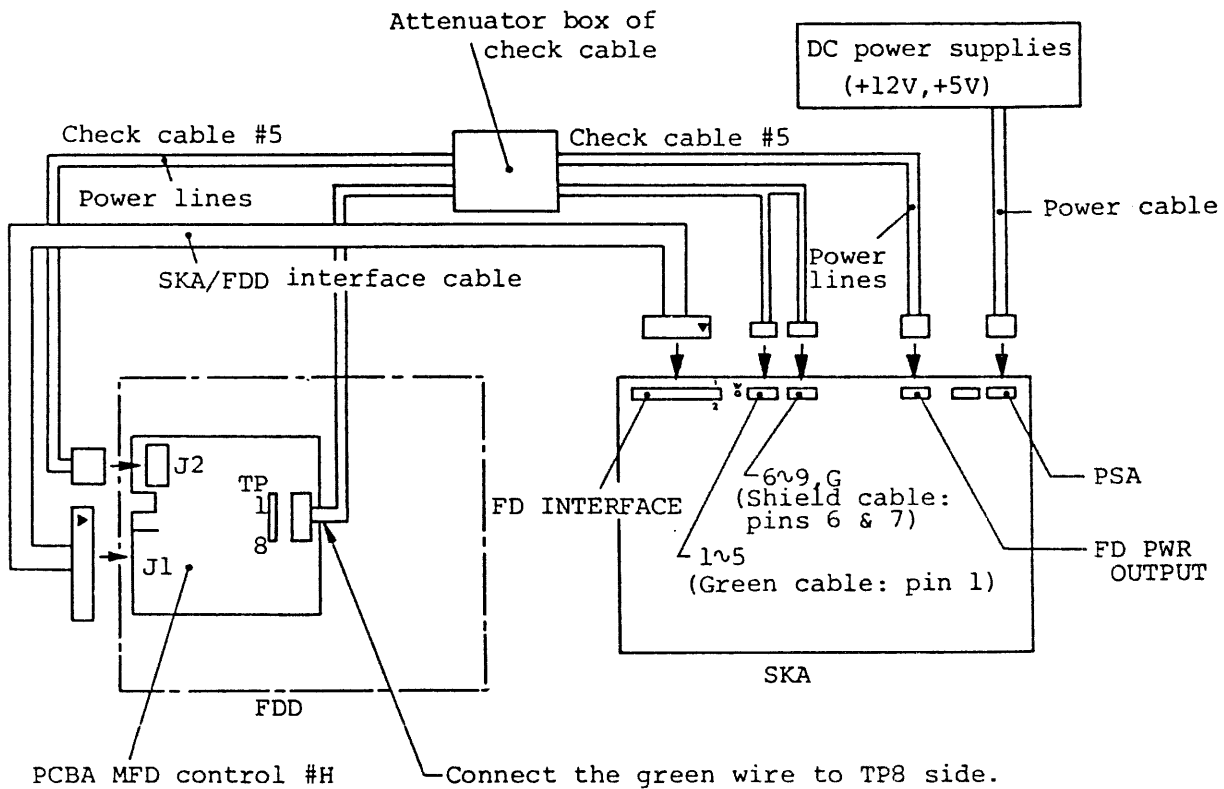
(Fig.406) Connection of SKA cable

(4) Connect the SKA/FDD interface cable. Pay attention to the identification mark of the connector (Δ) so that it locates at the pin 1 and 2 side.

(5) Connect the FD PWR OUTPUT of the SKA and J2 of the FDD with the power line of the check cable #5.

(6) Connect the black connector (8P) of the check cable #5 to TP1 ᷍ TP8 of the FDD. Be sure to connect so that the green wire comes to TP8 side.

(7) Connect the white connector with shielded wire of the check cable #5 to terminals 6 ᷍ 9, G of the SKA. The shielded wire side comes to terminals 6, 7 side of the SKA.

(8) Connect the white connector without shielded wire of the check cable #5 to terminals 1 ᷍ 5 of the SKA. Green wire side comes to terminal 1 side of the SKA.

(9) Turn the DC power on. Set the FD PWR switch of the SKA to the PSA side.

(10) Key in "CB". (+5V VOLTAGE)

(11) Adjust the DC power voltage so that the DATA indicator of the SKA ☐☐.☐☐ (V) indicates the value within the range of 5.00±0.1V.

(12) Key in "F". (STEP)

(13) Key in "CC". (+12V VOLTAGE)

(14) Adjust the DC power voltage so that the DATA indicator ☐☐.☐☐ (V) indicates the value within the range of 12.00±0.24V.

(15) Key in "F". (STOP)

Note: The above items (1), (2), (7), (8), (10) ∿ (15) may be omitted
for replacement of the FDD or a temporary FDD power off. Remain the
DC power on for the SKA and control the FDD power by the SKA PWR
switch.

4-2-4-2. Setting of the maximum track number

      Before the check and the adjustment of the FDD, set the maximum track
number according to the following instructions.
The setting will be maintained until the main DC power (SKA PWR) is
turned off or until the RESET switch of the SKA is depressed. Since
the FD PWR switch is independent of this setting, it is convenient
to maintain the main DC power on for the successive operations.
The initial setting of the following is not required if the maximum
track number is the same as the initial value of the SKA.

(1) Key in "CF". (SET TMAX)

(2) The maximum track number set at that time is indicated with the latter
two digits of the DATA indicator ☐☐☐☐ (track).

Note: If there is no change in the maximum track number in item (2),
      depress "F" key.

(3) Key in the maximum track number used for the FDD in two digits of
decimal notation.

   e.g. 48tpi (FD-55AV, BV): CF 39 (for 40 cylinders)
      96tpi (FD-55EV, FV): CF 79 (for 80 cylinders)
      96tpi, high density (FD-55GV): CF 76 (for 77 cylinders)

Note: If 80 cylinders are used in FD-55GV, key in "CF 79" also for the
      SKA (Key in "CF F" if it is the same as the initial value of the
      SKA).

4-2-4-3. Setting of step rate and settling time

Before check and adjustment of the FDD, set the step rate and the
settling time according to the following instructions.
The setting will be maintained until the main DC power (SKA PWR) is
turned off or until the RESET switch of the SKA is depressed.
If the step rate and the settling time are the same as the initial
values of the SKA, the initial setting of the following is not required.

(1) Key in "DB".   (SET STEP RATE)

(2) Step rate set at that time is indicated by 0.1msec scale on the DATA
    indicator ☐☐▪☐ (ms).

    e.g. DATA indicator ☐☐6̄0̄ indicates 6.0msec.

(3) Key in a new step rate down to one decimal place (unit:msec).

    Note: If there is no change in step rate in item (2), omit item (3) and
          forward to item (4).

(4) Key in "F".   (STOP -- Setting of the step rate completes).

(5) Settling time at that time is indicated by 0.1msec scale on the DATA
    indicator ☐☐▪☐ (ms).

    e.g. DATA indicator ☐1̄5̄0̄ indicates 15.0msec

(6) Key in new settling time down to one decimal place (Unit: msec).

    Note: If there is no change in settling time in item (5), omit item (6)
          and depress "F" key to complete the operation.

(7) Depress "F" key . (STOP -- Setting of the settling time completes).

    e.g. 48tpi (Step rate 6msec, Settling time 15msec): DB 60 F 150 F
         96tpi (Step rate 3msec, Settling time 15msec): DB 30 F 150 F

4-2-4-4. Level disk calibration

 Setting of the following calibration value is required for accurate
 measurement before the check of the read level or the resolution.
 Use a level disk with a calibration value (100% center) written on the
 label. The setting will be maintained until the main DC power (SKA PWR)
 is turned off or until the RESET switch of the SKA is depressed.
 If the calibration value is the same as the initial value (100%) of the
 SKA, the initial setting of the following is not required.

(1) Innermost track read level

 (a) Key in "D0". (CALIBRATION READ LEVEL)

 (b) Calibration value set at that time is indicated in the latter three
     digits of the DATA indicator [   ] (%).

 (c) Key in a new calibration value written on the level disk label
     (three digits, Max.).

 (d) Key in "F". (STOP)

  Note: If there is no calibration change in item (b), omit item (c) and
        depress "F" key.

(2) Innermost track resolution

 (a) Key in "D1". (CALIBRATION RESOLUTION)

 (b) Calibration value set at that time is indicated in the latter three
     digits of the DATA indicator [   ] (%).

 (c) Key in a new calibration value written on the level disk label.
     (three digits, Max.)

(d) Key in "F". (STOP)

Note: If there is no calibration change in item (b), omit item (c) and
      depress "F" key.

e.g. READ LEVEL 103%, RESOLUTION 96%: DO 103 F, Dl 96 F

Note: The setting in this item is not required when the level disk
      is not used (i.e., when it is substituted with a commercially
      available disk and no accurate measurement is required).
      Calibration value should be the same as the initial value (100%).

4-2-4-5. Alignment disk calibration

    Setting of the following calibration value is required for accurate
measurement before the check and adjustment of the track alignment.
Use a correctly calibrated (0% center) alignment disk with a calibration
value written on the label. The setting will be maintained until
the main DC power (SKA PWR) is turned off or until the RESET switch of
the SKA is depressed.
If the calibration value is the same as the initial value (0%) of the
SKA, the initial setting of the following is not required.

(1) SIDE 0 alignment

  (a) Key in "E0". (CALIBRATION SIDE 0 ALIGNMENT)

  (b) The calibration value set at that time is indicated in the latter two
      digits of the DATA indicator ☐☐☐☐ (%), and the polarity is indicated
      in the initial digit. If a "0" is indicated, the polarity is positive.

      Polarity indication: plus /- , minus −

  (c) Key in a polarity and a new calibration value (two digits, Max.)
      written on the alignment disk label.

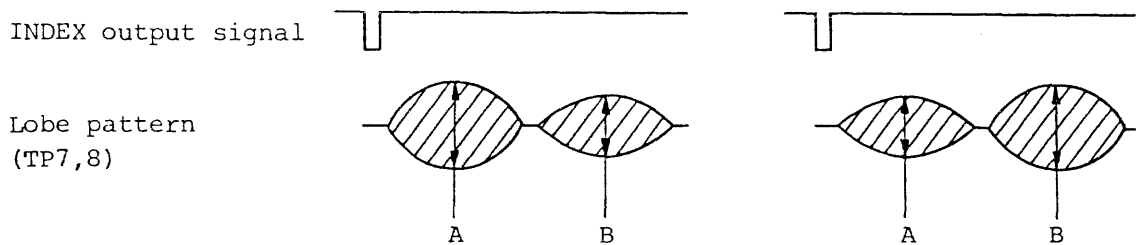   Designation of polarity: Depress "B" key only for minus designation.
                          (No designation is required for plus).

  (d) Key in "F". (STOP)

(2) Side 1 alignment

  (a) Key in "E1". (CALIBRATION SIDE 1 ALIGNMENT)

  (b) The same as in item (1)-(b) ∿ (d).

INDEX output signal

Lobe pattern
(TP7,8)

A   B   A   B

Notes: 1. The lobe pattern ratio is calibrated in the SKA according to the following expression.

$$\text{Lobe pattern ratio after calibration} = \frac{A-B}{\text{Larger one of A \& B}} \times 100 - \text{Calibration value(\%)}$$

2. If the calculated value with the above expression is positive, the polarity is plus, while the polarity is minus when the value is negative.

(Fig.407) Calibration of alignment lobe pattern

(3) Index burst timing

(a) Key in "E5". (CALIBRATION INDEX TIMING)

(b) The calibration value set at that time is indicated in the latter three digits of the DATA indicator ☐☐☐☐ (μs), and the polarity is indicated in the initial digit. (Refer to item (1)-(b)).
   If a "0" is indicated, the polarity is positive.

(c) Key in a polarity and a new calibration value (three digits, Max.) written on the alignment disk label. Refer to item (1)-(c) for the polarity designation.

(d) Key in "F". (STOP)

Note: If there is no change in the calibration value in item (b), omit item (c) and depress "F" key.

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e.g. Double sided FDD, SIDE 0 ALIGNMENT +3%, SIDE 1 ALIGNEMTN -5%,
     INDEX TIMING -25μs:

     E0 3 F, El B 5 F, E5 B 25 F

INDEX output signal

Index burst (TP4,5)

t —— Index burst timing
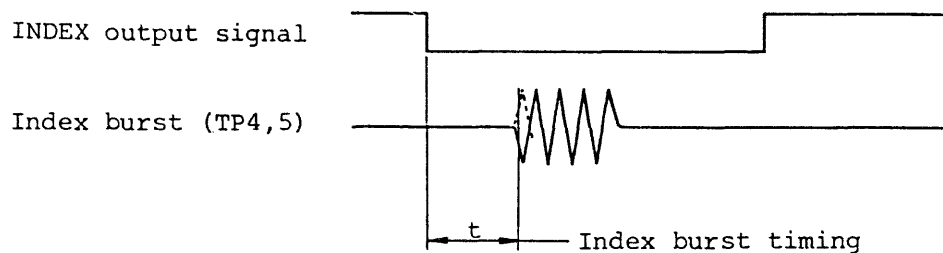
Notes: 1. The index timing is calibrated in the SKA according to the
          following expression.

          Calibrated timing = t - calibration value (μs)

       2. If the calculated value with the above expression is
          positive, the polarity is plus, while the polarity is minus
          when the value is negative.

          (Fig.408) Calibration of index burst timing

4-2-4-6. Humidity setting

For the check and adjustment of the track alignment using an alignment disk, set the environmental relative humidity to the SKA in order to improve the precision of measurement.
This setting is important when the relative humidity is considerably different from 50% at the 96tpi FDD.
The initial setting of the following is not required if the relative humidity is the same as the initial value (50%) of the SKA.

(1) Key in "F2".   (CALIBRATION RH ALIGNMENT)

(2) The relative humidity set at that time is indicated in the latter two digits of the DATA indicator ☐☐☐☐ (%).

(3) Input the relative humidity percentage in the measurement environment (two digits, Max.)

 e.g. Relative humidity 58%: E2 58

4-2-4-7. Gain setting

Following setting is required for the check and adjustment of this FDD.

(1) Track alignment of 96tpi (FD-55EV, FV, GV):

Key in "DD" to confirm that the H GAIN indicator of the SKA is on.

(2) Track alignment of 48tpi (FD-55AV, BV), and other items:

Confirm that H GAIN indicator of the SKA is off. If it is on, depress "DD" key again to turn it off.

4-2-4-8. Setting of FDD straps and SKA special key

(1) Setting of FDD straps

It is required to confirm before the operation that the straps (short
bars) on the PCBA MFD control #H are at the appropriate position for the
system to be used in the check and adjustment.
For the purpose of simplyfying the explanation, it is recommended to
set the following straps on when you use the SKA. However, if you can
set the straps correctly referring to Specification, Schematic Diagrams,
and SKA Instruction Manual, you need not to follow this recommendation.

Strap setting.
(a) DS0 ∿ DS3 block: Make DS0 on.
(b) U1 ∿ IU block: IU may be on or off. Others are off.
(c) FG block: Make FG on.
(d) Other blocks: Initial setting of the FDD.

Note: If the strap position of the FDD is changed from the initial
     setting at the system installation, be sure to change it back
     to the initial position after maintenance.

(2) Setting of SKA special key

(a) The signal level of the interface connector pin No.4 (IN USE/HEAD
    LOAD) changes alternately between TRUE and FALSE by depressing "A"
    (IN USE) key of the SKA. When it is TRUE, "A" indicator turns on.
    Refer to the Specification as to the function of the signal and its
    relation to the straps.

(3) Signal of interface connector pin No.34

When the output signal of interface connector pin No.34 (READY, OPEN,
or other optional signals) is TRUE (LOW level), "RDY" indicator of the

SKA turns on.

Refer to the specification as to the function of the signal and its relation to the straps.

4-2-5. Others

(1) Terminator

When you check each FDD with a maintenance system such as the SKA,
it is necessary to put the terminator network into the IC socket J3 on
the PCBA MFD control #H. The terminator shall be returned to the initial
condition after completion of the maintenance.

For the fixed type terminator without IC socket (soldered on PCB), above
instruction is not applied.

(2) Connection of the probe ground

Connect the probe ground of the equipment as follows:

(a) For the observation at the test points (TP) 4, 5 (Pre-amplifier) and
TPs 7, 8 (Differentiation amplifier):
Connect the probe ground to the TP6 (OV) on the PCBA MFD control #H.

(b) For the observation at the other test point:
Connect the probe ground to the TP6 (OV) on the PCBA MFD control #H,
or GND(OV) terminal of the system power supply unit, or the GND
terminal of the SKA.

(c) For the observation of the SKA test point:
Connect the probe ground to the GND terminal of the SKA.

Note: When you use the SKA, almost all the checks including the read
amp. output level at TPs of the FDD will be done automatically
through the check cable #5 and FDD interface cable.
Also these signals can be observed by an oscilloscope using the
test points on the SKA.

(3) Head load of the CSS model

For the CSS model (without head load solenoid), the FDD is always in head load condition as far as a disk is inserted and the front lever is closed.

(4) Orientation of the FDD

Position the FDD as shown in Fig.409 unless otherwise specified.

Lever
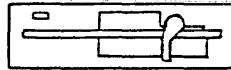
Horizontal setting   Vertical setting
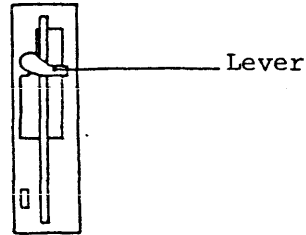
(Fig.409) General orientation of the FDD during maintenance

(5) Maintenance environment

Maintenance of the FDD should be done on a clean bench at room temperature and humidity. It is recommended to execute the check and adjustment of the track alignment after leaving the FDD for at least 2 hours at room temperature and humidity. The magnetic head, disk, steel belt, etc. might suffer from dust and dirt if the maintenance is not undertaken in a clean environment.

(6) Disk

There are two sectoring types in normal density disks which are soft sectored disk and hard sectored disk. Use soft sectored disks when the

SKA is used.

For the check and adjustment of high density FDD (FD-55GV), appropriate high density (HD) disk is required.

(7) Total error test

In the check and adjustment in item 4-4, read/write error test is not included. After the adjustment or the replacement of the maintenance parts, it is recommended to perform a data error test by connecting the FDD to the user's system or the TEAC simulator KB. The window margin test is the most recommended item.

4-3. PREVENTIVE MAINTENANCE

4-3-1. Cleaning of Magnetic Head by Cleaning Disk

When you use the FDD in dusty environment, it is recommended to clean the magnetic head surface periodically (e.g. once a month) with a commercially available cleaning disk. Especially for a double sided FDD, it is difficult to clean the head surface directly, be sure to use the cleaning disk.

For typical usage under typical environmental condition, the cleaning is recommended when data errors often occur.

(A) Equipment

(1) Cleaning disk
(2) SKA or user's system

(B) Cleaning procedure

(1) General method

(a) Install an appropriate cleaning disk and start the spindle motor.

Notes: 1. Do not use a damaged cleaning disk on the surface.
2. For a single sided FDD, be sure to install a single sided cleaning disk. The cleaning surface of the disk shall be in contact with the head surface.
When the FDD is placed horizontally, the magnetic head is located down and it faces the back side of the disk.
If a double sided cleaning disk is installed in a single sided FDD, it may damage the head pad.
3. For a double sided FDD, a double sided cleaning disk should be used. Side 0 (lower side) and side 1 (upper side) heads are cleaned simultaneously.

(b) Execute head loading and clean the head at a suitable track position
    for 10 ∿ 30 seconds, approx. In order to avoid the concentration on
    a specific track, it is a good way to make the head move between
    track 00 and the innermost track during cleaning.

    Note: The most appropriate cleaning time is different for each type of
          cleaning disk used.
          Excessively long cleaning time is not effective but has possibility
          to accelerate the head wear.

(c) Remove the cleaning disk.

(2) SKA method

    (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch
        to the PSA side.

    (b) Execute drive select by key "0". (DS0 indicator turns on).

    (c) Key in "C0" and confirm that the TRACK indication of the SKA
        becomes "00". (RECALIBRATE)

    (d) Install an appropriate cleaning disk. See item (1)-(a), "Notes".

    (e) Start the spindle motor by key "5". (MON indicator turns on).

    (f) Key in "C6". (SEEK TEST)

    (g) After 10 ∿ 30 seconds, depress "F" key.

    (h) Eject the cleaning disk.

4-3-2. Direct Cleaning (Single sided)

This cleaning method is applied only to a single sided FDD.
If this method is applied to a double sided FDD, gimballed mechanism
might be damaged.
If visible dirt is on the head surface when the head pad arm is lifted
up manually during maintenance, perform direct cleaning as follows:

(A) Equipment

(1) Absolute alcohol (Ethanol)
(2) Cotton swab or gauze

(B) Cleaning procedure

(1) Lightly dampen a cotton swab or a gauze with alcohol.

(2) Lift up the pad arm (see Fig.410) and clean the head surface carefully
with the cottom swab or the gauze.
Note: Do not touch the pad surface.

(3) Wipe the head surface with clean dry cloth after the evaporation of the
alcohol.

(4) After confirming that the dirt is cleaned off and no fluff is left on
the head surface, let the pad arm down carefully.

Pad —

— Pad arm

Set arm —

— Arm lifter

Magnetic head
surface

Head carriage Ass'y —
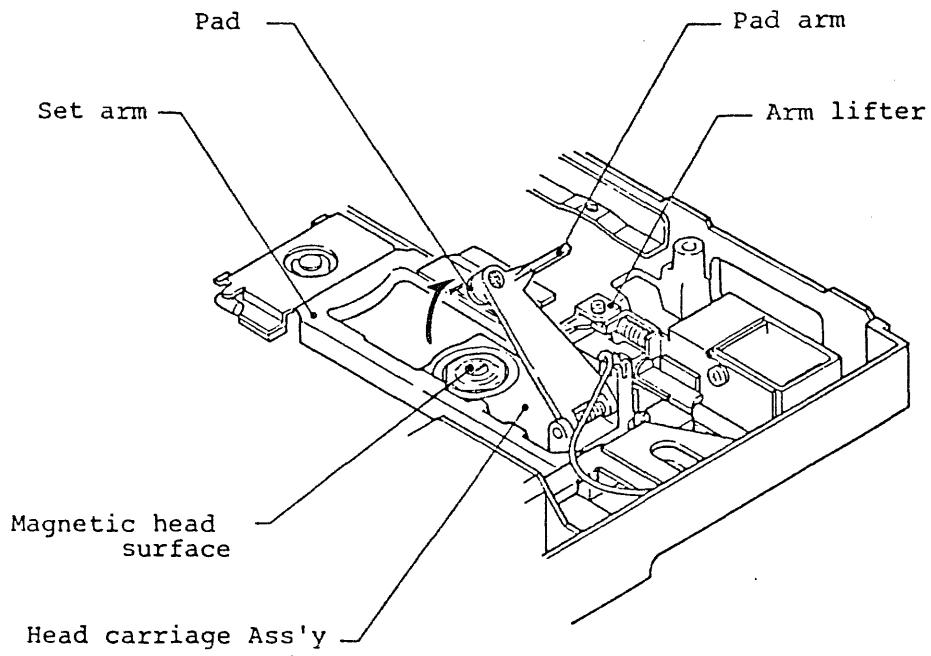
(Fig.410) Direct cleaning of the magnetic head (Single sided only)

4-4. CHECK AND ADJUSTMENT

4-4-1. Adjustment of Set Arm Position

  (A) Equipment

  (1) Cross point screwdriver, M3

  (2) Locking paint

  (B) Adjustment procedure

  (1) Loosen two fixing screws of the set arm (see Fig.411) so that the set
      arm can be moved manually without getting out of place.

  (2) Close the set arm by turning the front lever.

  (3) In this condition (item (2)), adjust the set arm so that the visial
      distance of the gap between the collet shaft and the set arm hole
      becomes even.

  (4) Tighten the installing screws of the set arm with the specified torque.

  (5) Open and close the set arm by turning the front lever and confirm that
      it does so smoothly.

Collect shaft

Set arm

2-Set arm fixing
screws

Gap between collet shaft and set arm hole

Front lever
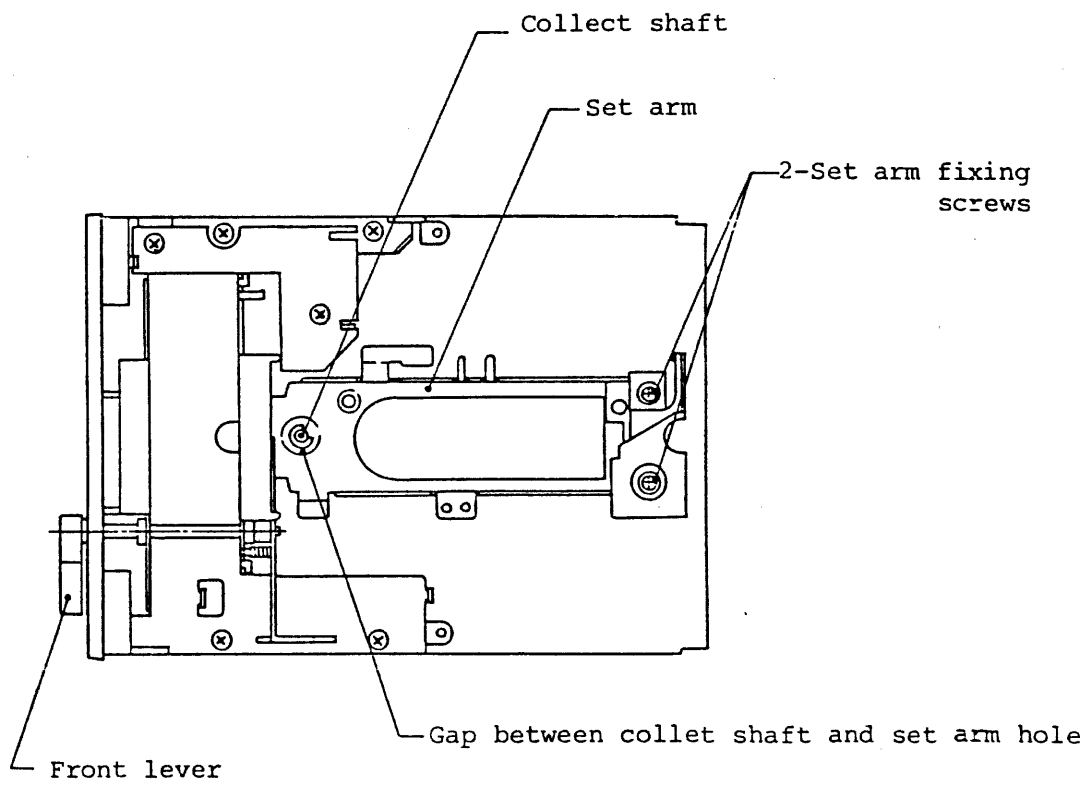
(Fig.411) Adjustment of set arm position

4-4-2. Check and Adjustment of Holder Position

(A) Equipment

(1) Corss point screwdriver, M3

(2) MAX media jig C

(3) MAX media jig E

(B) Check and adjustment procedure

(1) Insert the MAX media jig E from open side until it strikes the frame
    stopper. (See Fig.412).

(2) When closing the front lever at the stop side ·of the MAX media jig E,
    confirm that the wing of the front lever disturbs the rotation and that
    the lever cannot be closed.

(3) When turning the MAX media jig E over to insert it for pass side, and
    closing the front lever, confirm that the lever can be closed.

(4) If the item (2) or (3) is not satisfied, adjust the holder position
    according to the following procedure.

   (a) Loosen four fixing screws (see Fig.413) of the holder so that the
       holder can be moved manually without going out of place.

   (b) Install the MAX media jig C from open side to set it to be in contact
       with the frame stopper.

   (c) Turn the front lever to close position. Loosen the fixing screws of
       the holder again to make the holder move toward the arrow indicated
       direction in Fig.413, then depress the wing area of the front lever
       against the MAX media jig C. Refer to Fig.414.

(d) Tighten the four fixing screws of the holder with specified torque.

(e) Confirm items (1) through (3).

(f) Check for the file protect sensor according to item 4-4-5.

(g) Check and adjust the index burst timing according to item 4-4-15.
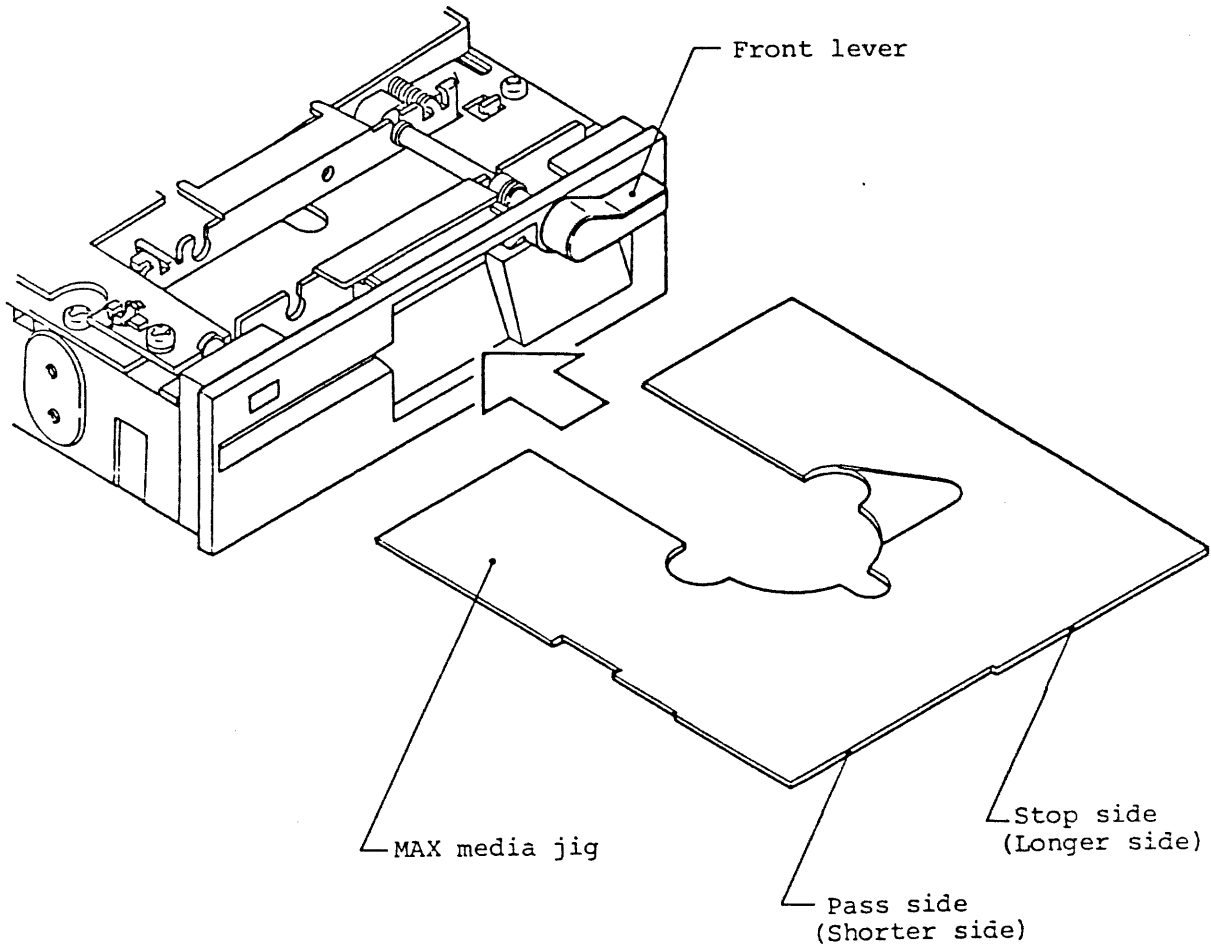
(Fig.412) Insertion of MAX media jig

Holder

Front lever

Holder fixing screws
2-each side
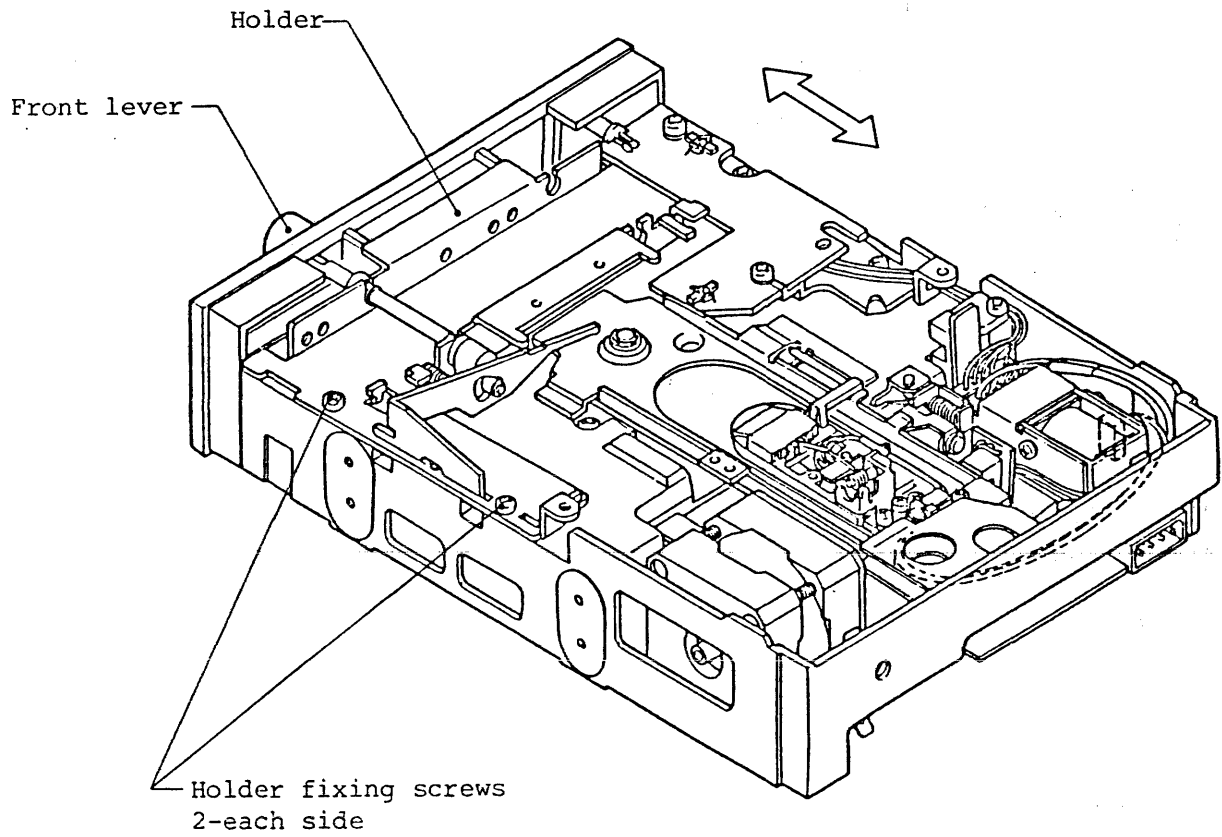
(Fig.413) Adjustment of holder position 1

Front bezel

Front lever

MAX media jig

Wing
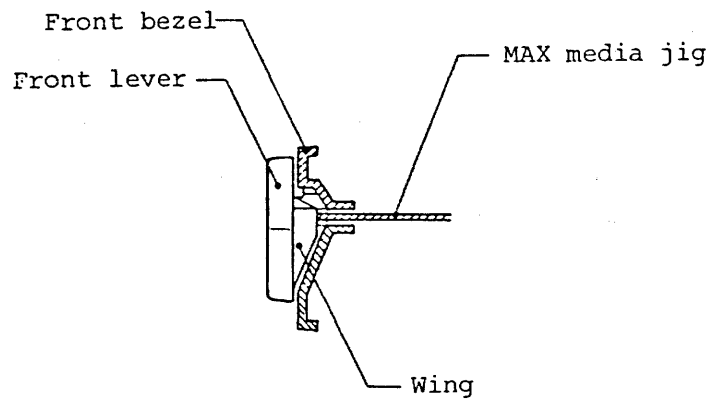
(Fig.414) Adjustment of holder position 2

4-4-3. Check and Adjustment of Arm Lifter

This item is applied only for the FDD with the head load solenoid, and the adjusting method is different for single sided and for double sided.

4-4-3-1. Double sided

(A) Equipment

(1) Common screwdriver, small size

(2) Work disk

(3) SKA or user's system

(4) Oscilloscope

(5) Locking paint

(B) Check and adjustment procedure

(1) General method

(a) Install a work disk and start the spindle motor.

(b) Set the head to track 00.

(c) Execute head loading.

(d) Confirm that the gap between the upper arm and the arm lifter is larger than 0.2mm. If the gap is narrower than 0.2mm, turn the adjusting setscrew of the arm lifter. Refer to Figs.415 and 416.

(e) Unload the head.

(f) Confirm that the upper arm is lifted slightly by the arm lifter.

Arm lifter

Arm lifting part

Arm lifter adjusting screw

Locking paint

Head load solenoid Ass'y

Head carriage Ass'y
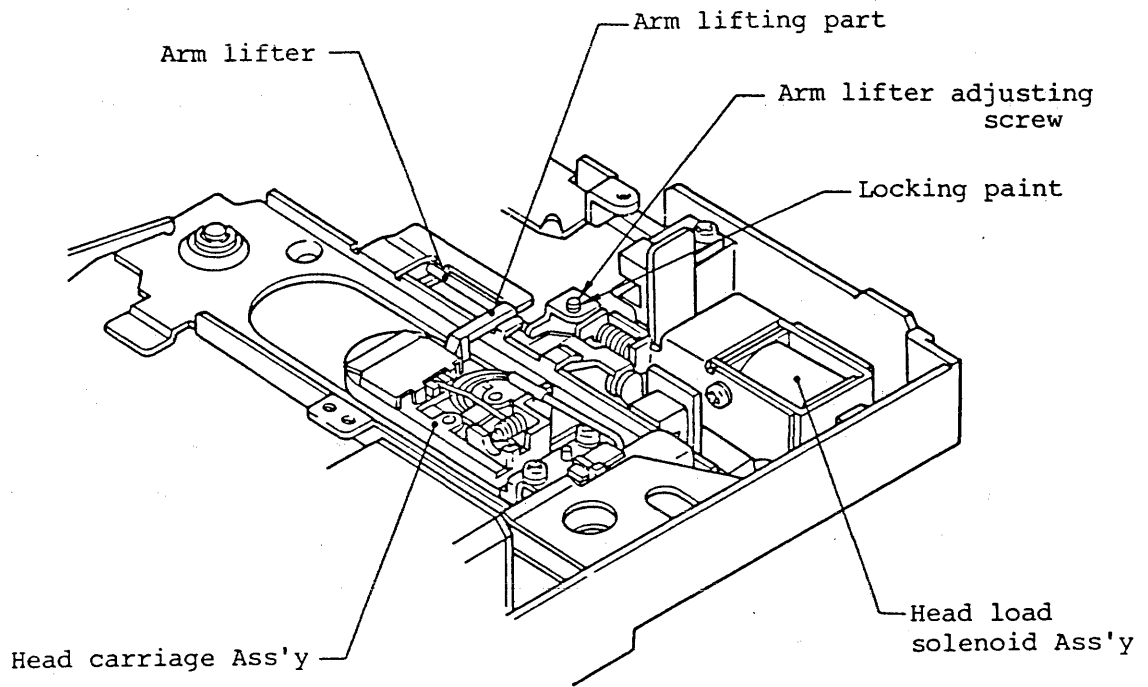
(Fig.415) Adjustment of arm lifter

Arm lifting part

Upper arm

0.2mm,Min.

Head carriage Ass'y
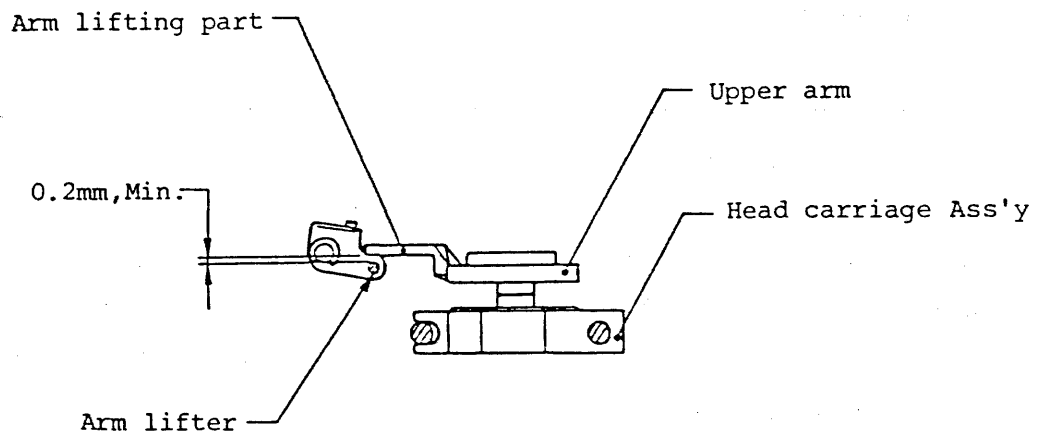
Arm lifter

Note: Viewed from front bezel side.

(Fig.416) Gap of arm lifter

(g) Use two channels of oscilloscope. Connect the 1st channel to the
    head load command signal and the 2nd channel to TP7 or TP8 on the
    PCBA MFD control #H. Triggering is done by the head load command.

    Oscilloscope range
        The 1st channel: DC mode, 2V, 10msec
        The 2nd channel: AC mode, 0.5 ∿ 1V, 10msec

Note: For the purpose of check and adjustment in this item, it is not
      proper to execute the head loading by the MOTOR ON signal. Use
      either of the DRIVE SELECT signal or the IN USE/HEAD LOAD signal.
      Refer to item 4-2-4-8 or the Specification item 1-12-1).

(h) Select the side 1 head.

(i) Execute the head loading.

(j) Execute 2F write operation (WRITE DATA frequency of 250KHz for
    FD-55AV ∿ FV and 500KHz for FD-55GV) for one rotation of the disk.

(k) Unload the head.

(L) Repeat the head loading and unloading alternately (tapping operation)
    and observe the waveform of TP7 or TP8 by the oscilloscope.

(m) Set the oscilloscope trigger to the positive mode and observe the read
    waveform at TP7 or TP8 after the input of an unload command. Confirm
    that there is no big spike noise (excludes a small one) or there is
    not a continuous unload level (excludes the noise level) as shown
    by dotted line in Fig.417.
    In such event that either of the spike noise or continuous unload
    level is observed in the waveform, fine adjust the setscrew of the
    arm lifter.

Head load command   ┌─────────────── TRUE ───────────────────

TP7 or TP8

                    Head load command   Head load time
                                         (A/B≥0.7 after 35ms)
                                         (Settled at 50ms)

Head unload command ─┐   FALSE

TP7 or TP8   ── Spike noise

                    Head unload command   Residual read level
                                             (Unload level)

(Fig.417) Read waveforms at head loading/unloading

Note: This item shall be executed when the side 1 head is selected.
      If the side 1 head is lifted too high during unload operation,
      spike noise will be observed, while unload level will be observed
      when it is too low.

(n) Set the oscilloscope trigger to the negative (-) mode and observe
    the waveform at TP7 or TP8 after the input of a head load command.
    Confirm that the read waveform more than 50msec after the head load
    command is almost settled.
    Or confirm that bottom "A" of the read level more than 35msec after
    the input of the head load command is more than 0.7 against the
    average read level "B".   (A/B ≥ 0.7 in Fig.417).

(o) Make the head move to the innermost track.

(p) Repeat the procedure from item (i) to (n) and adjust so that the items (m) and (n) are satisfied at track 00 and at the innermost track.

(q) The items (m) and (n) are also applied to the side 0 head. However, as to the unload level in item (m) will be excluded unless it is the same read level as the head load condition.
    Confirm in the same manner by selecting the side 0 head.

(r) Again set the head to track 00.

(s) After opening the front lever, draw out the disk slowly. In the process of drawing out, the side 0 and side 1 heads shall not catch the head window edge of the disk jacket (opening area of the jacket to make the head be in contact with the disk surface). The jacket can be drawn out smoothly with appropriate space margin.

(t) Insert the disk slowly and confirm that the disk jacket does not touch the side 0 nor side 1 head and goes into the FDD smoothly with appropriate space margin.

(u) If the items (p), (q), (s) or (t) is out of the specification, following causes are assumed.

    i) Inferior disk:
        Disk and/or jacket is deformed or the disk may have drop-outs.
        In such event, replace the work disk with a new one.
    ii) Inferior head carriage Ass'y:
        Replace the head carriage Ass'y according to item 4-5-1.
    iii) Inferior head load solenoid:
        Replace the head load solenoid Ass'y according to item 4-5-5.
    iv) Inferior PCBA MFD control #H:

Replace the PCBA MFD control #H according to item 4-5-7. (No replation to items (s) and (t)).

Note: Apply a drop of locking paint, if the setscrew is adjusted. And if the strap setting is changed, back it to the initial setting after the adjustment.

(2) SKA method

   (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch
       to the PSA side.

   (b) Install a work disk.

   (c) Start the spindle motor by key "5". (MON indicator turns on).

   (d) Execute drive select by key "0". (DS0 indicator turns on).

   (e) Key in "C0" and confirm that the TRACK indication becomes "00".
       (RECALIBRATE)

   (f) Confirm that the gap between the upper arm and the arm lifter is
       larger than 0.?mm. If the gap is narrower than 0.2mm, turn the
       adjusting setscrew of the arm lifter. Refer to Figs.415 and 416.

   (g) Release the drive select by key "0". (DS0 indicator turns off).

   (h) Confirm that the upper arm is lifted slightly by the arm lifter.

   (i) Use two channels of oscilloscope. Connect the 1st channel to the
       DOUT terminal and the 2nd channel to the DIF terminal of the SKA.
       Apply negative trigger by the DOUT terminal.

       Oscilloscope range
           The 1st channel: DC mode, 2V, 10msec
           The 2nd channel: AC mode, 0.5 ∿ 1V, 10msec

      Note: For the check and adjustment in this item, it is required to set
            the straps according to item 4-2-4-8.

(j) Key in "BC F".   (DRIVE SELECT observation)

(k) Select side 1 head by key "4".   (SIDE 1 indicator turns on).

(L) Execute drive select by key "0".   (DS0 indicator turns on).

(m) Key in "C9".   (HEAD LOAD TIME)

(n) Observe the waveform of the DIF terminal at head unloading using the oscilloscope.
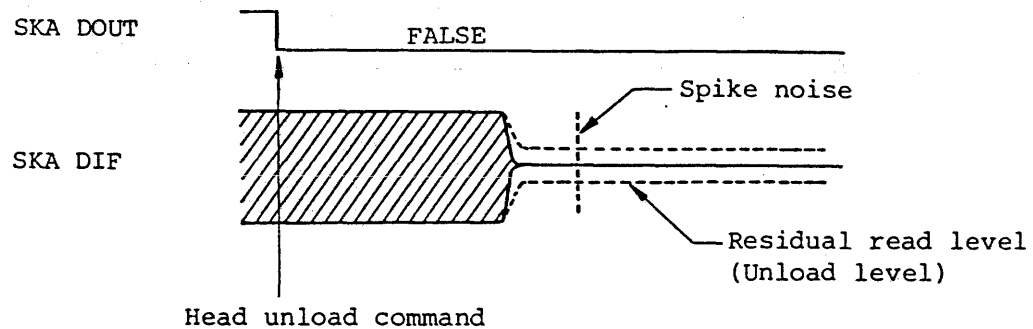
(Fig.418) Read waveform at head unloading

(o) Confirm that there is no big spike noise (excludes a small one) or there is not a continuous unload level (excludes the noise level) as shown by dotted line in Fig.418.

In such event that either of the spike noise or continuous unload level is observed in the waveform, fine adjust the setscrew of the arm lifter.

Note: This item shall be executed when the side 1 head is selected (SIDE 1 indicator turns on).

If the side 1 head is lifted too high during unload operation, spike noise will be observed, while unload level will be observed when it is too low.

(p) Confirm that the DATA indicator ☐☐☐☐ (%) of the SKA indicates a value within the following range.
Head load settling level: 70%, Min.

(q) Key in "F". (STOP)

(r) If the DS0 indicator of the SKA is off, execute drive select by key "0". (DS0 indicator turns on).

(s) Key in "C1". (SEEK TMAX).

(t) Repeat the procedure from items (m) to (p) and adjust so that the items (o) and (p) are satisfied at track 00 and at the innermost track.

(u) Key in "F". (STOP)

(v) The items (o) and (p) are also applied to the side 0 head. However, as to the unload level in item (o) will be excluded unless it is the same read level as the head load condition.
Depress key "4" to turn off the SIDE 1 indicator of the SKA and confirm in the same procedure of items (L) through (u) for the side 0 head.

(w) Key in "C0" and confirm that the TRACK indication becomes "00". (RECALIBRATE)

(X) After opening the front lever, draw out the disk slowly. In the process of drawing out, the side 0 and side 1 heads shall not catch the head window edge of the disk jacket (opening area of the jacket to make the head be in contact with the disk surface). The jacket can be drawn out smoothly with appropriate space margin.

(y) Insert the disk slowly and confirm that the disk jacket does not

touch the side 0 nor the side 1 head and goes into the FDD smoothly with appropriate space margin.

(z) If the items (t), (v), (x), or (y) is out of the specification, refer to item (u) of "General method".

Note: Apply a drop of locking paint, if the setscrew is adjusted.

4-4-3-2. Single sided

(A) Equipment

(1) Common screwdriver, small size

(2) Work disk

(3) SKA or user's system

(4) Locking paint

(B) Adjustment procedure

(1) General method

(a) Install a work disk and start the spindle motor.

(b) Set the head to track 00.

(c) Execute head loading.

(d) Confirm that the gap between the pad arm and the arm lifter is larger than 0.2mm. If the gap is narrower than 0.2mm, turn the adjusting screw of the arm lifter. Refer to Figs.415 and 416.

(e) Unload the head.

(f) Confirm that the pad arm is lifted slightly by the arm lifter.

(g) Make the head move to the innermost track.

(h) Execute head loading and repeat the procedure from item (d) through (f).

(i) Set the head to track 00 again.

(j) Repeat the procedure of items (c) through (f).

Note: After adjusting the setscrew, apply a drop of locking paint.

(2) SKA method

    (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch
        to the PSA side.

    (b) Install a work disk.

    (c) Start the spindle motor by key "5". (MON indicator turns on).

    (d) Execute drive select by key "0". (DS0 indicator turns on).

    (e) Key in "C0" and confirm that the TRACK indication becomes "00".
        (RECALIBRATE)

    (f) Confirm that the gap between the pad arm and the arm lifter is
        larger than 0.2mm. If the gap is narrower than 0.2mm, turn the
        adjusting setscrew of the arm lifter. Refer to Figs.415 and 416.

    (g) Release the drive select by key "0". (DS0 indicator turns off).

    (h) Confirm that the pad arm is lifted slightly by the arm lifter.

    (i) Execute drive select by key "0". (DS0 indicator turns off).

    (j) Key in "C1". (SEEK TMAX).

    (k) Repeat the procedure of items (f) through (i).

    (L) Key in "C0". (RECALIBRATE)

    (m) Repeat the procedure of items (f) through (i).

    Note: If the setscrew is adjusted, apply a drop of locking paint.

4-4-4. Check of CSS Ass'y

This item applies only to the double sided CSS models (without head load solenoid).

(A) Equipment

(1) Work disk

(2) SKA or user's system

(B) Check procedure

(1) General method

(a) Open and close the front lever with no insertion of a disk.

(b) Confirm that the side 1 head is lifted even if the front lever is closed and it has enough gap against the side 0 head. (See Fig.419).
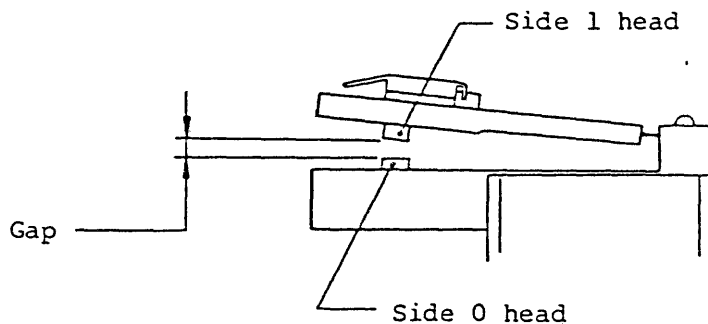
(Fig.419) Gap between side 0 and side 1 heads

(c) After opening the front lever, insert a work disk slowly.
Confirm that the disk jacket does not touch the side 0 nor side 1 head and goes into the FDD smoothly with appropriate space margin.

(d) Draw out the disk slowly. Confirm that the side 0 and side 1 heads
    do not catch the head window edge of the disk jacket (opening area
    of the jacket to make the head be in contact with the disk surface)
    and that the jacket can be drawn out smoothly with appropriate space
    margin.

(e) Confirm that the cam (natural color) of the CSS Ass'y attached to the
    left side of the head carriage moves as in Fig.420 by opening/closing
    of the front lever and insertion/ejection of the disk.

i) Disk is not fully inserted.   ii) Disk is fully inserted and
                                      front lever is close.

(Fig.420) Cam rotation of CSS Ass'y

(f) Insert a work disk and start the spindle motor.

(g) Set the head to track 00.

(h) In the close condition of the front lever, confirm that the gap
    between the upper arm and the arm lifter is 0.2mm, Min. Refer to
    Fig.416.

(i) Make the head move to the innermost track.
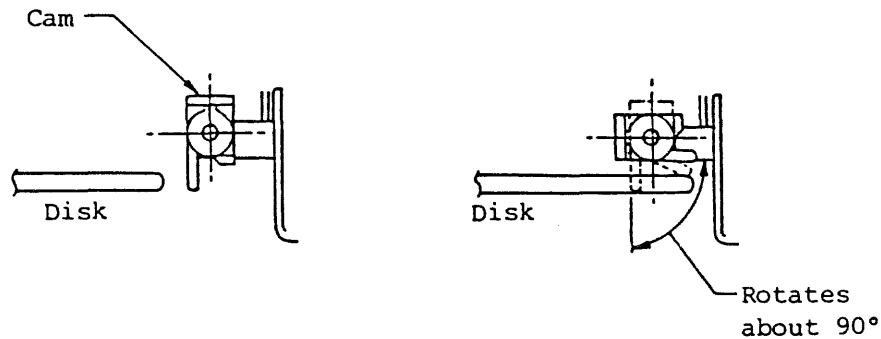
(j) Confirm as in item (h).

(2) SKA method

(a) Open and close the front lever with no insertion of a disk.

(b) Confirm that the side 1 head is lifted even if the front lever is
    close and it has enough gap against the side 0 head. Refer to Fig.419.

(c) After opening the front lever, insert a work disk slowly.
    Confirm that the disk jacket does not touch the side 0 nor side 1
    head and goes into the FDD smoothly with appropriate space margin.

(d) Draw out the disk slowly. Confirm that the side 0 and side 1 heads
    do not catch the head window edge of the disk jacket (opening
    area of the jacket to make the head be in contact with the disk
    surface) and that the jacket can be drawn out smoothly with
    appropriate space margin.

(e) Confirm that the cam (natural color) of the CSS Ass'y attached to the
    left side of the head carriage moves as in Fig.420 by opening/closing
    of the front lever and insertion/ejection of the disk.

(f) Connect the SKA according to item 4-2-4 and set the FD PWR switch to
    the PSA side.

(g) Start the spindle motor by key "5". (MON indicator turns on).

(h) Execute drive select by key "0". (DS0 indicator turns on).

(i) Key in "C0" and confirm that the TRACK indication becomes "00".
    (RECALIBRATE)

(j) In the close condition of the front lever, confirm that the gap
    between the upper arm and the arm lifter is 0.2mm, Min. Refer to
    Fig.416.

(k) Key in "Cl". (SET TMAX).

(L) Confirm as in item (j).

4-4-5. Check of File Protect Sensor

(A) Equipment

 (1) MAX media jig C

 (2) KSA or user's system

(B) Check procedure

 (1) General method

  (a) Place the FDD on the work bench with the LED indicator up and the
      front lever down. (See Fig.421).

  (b) Connect an oscilloscope (DC range, 2V/div) to the WRITE PROTECT
      interface line.

  (c) Insert the MAX media jig C from open side and set it so that the
      notch A area is located on the light pass from the file protect
      sensor LED. (See Fig.421).

  (d) Adjust the orientation of the FDD so that it is not exposed with
      strong light.

  (e) Confirm that the WRITE PROTECT signal goes to LOW level when power is
      supplied and the FDD is DRIVE SELECTed.

  (f) Pull out the jig a little so that the notch B area is located on the
      light pass.

  (g) Confirm that the WRITE PROTECT signal goes to HIGH level.

LED indicator

MAX media jig

Notch B

Notch A

File protect
sensor

Front lever
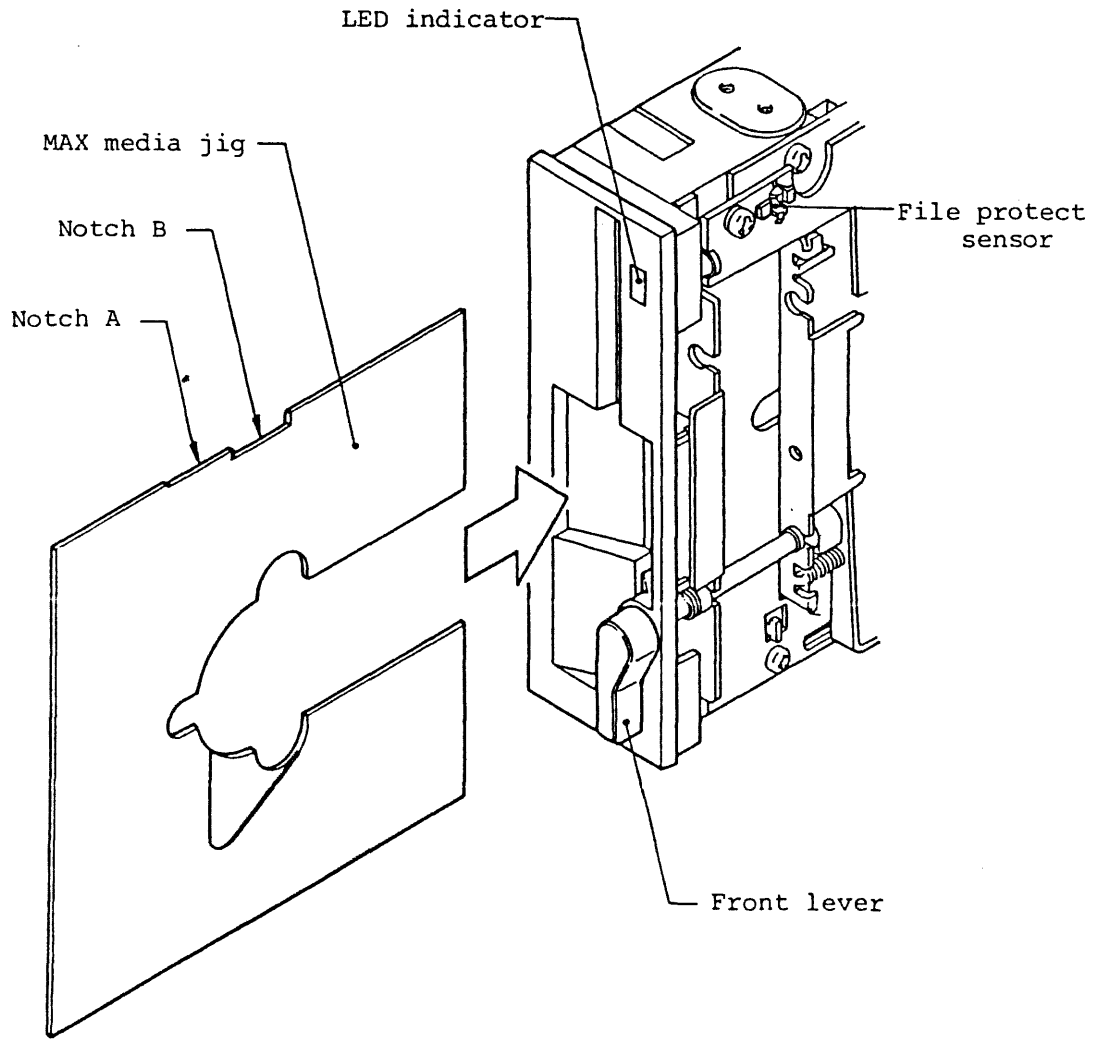
(Fig.421) Check of file protect sensor

(2) SKA method

    (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch to the PSA side.

    (b) Insert the MAX media jig C from open side and set it so that the notch A area is located on the light path from the file protect sensor LED. (See Fig.421).

    (c) Adjust the orientation of the FDD so that it is not exposed with strong light.

    (d) Confirm that the WPROT indicator of the SKA turns on, when the FDD is selected by key "0". (DS0 indicator turns on).

    (e) Pull out the jig a little so that the notch B area is located on the light path.

    (f) Confirm that the WPROT indicator turns off.

4-4-6. Check of Disk Rotation Speed

Disk rotation speed is set to 300rpm for FD-55AV ∿ FV and 360rpm for
FD-55GV.

(A) Equipment

(1) SKA or user's system

(2) Frequency counter (not required when the SKA is used)

(3) Work disk (for high density)

(B) Check procedure

(1) General method

(a) Connect a frequency counter to TP1 (Index) on the PCBA MFD control #H
    or to the INDEX interface signal line.

(b) Install a work disk and start the spindle motor.

(c) Set the head to track 00.

(d) Execute the head loading.

(e) Confirm that the pulse interval at TP1 or at the INDEX interface is
    within the following range.

        FD-55AV ∿ FV: 200 ± 3msec
        FD-55GV: 166.7 ± 2.5msec

(2) SKA method

   (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch
       to the PSA side.

   (b) Install a work disk.

   (c) Start the spindle motor by key "5". (MON indicator turns on).

   (d) Execute drive select by key "0". (DS0 indicator turns on).

   (e) Key in "C0" and confirm that the TRACK indication becomes "00".
       (RECALIBRATE)

   (f) Key in "C3". (INDEX PERIOD)

   (g) Confirm that the DATA indicator ⬜⬜⬜⬜ (ms) indicates a value within
       the following range.

       FD-55AV ∿ FV: 200 ± 3msec
       FD-55GV: 166.7 ± 2.5msec

   (h) Depress "F" key. (STOP)

4-4-7. Check of Erase Gate Delay

The purpose of this item is to confirm the function of the control LSI.
This item is not so important as far as the FDD operates normally.

(A) Equipment

(1) SKA or user's system
(2) Oscilloscope (not required when the SKA is used)
(3) Work disk

(B) Check procedure

(1) General method

(a) Use two channels of oscilloscope. Connect the trigger channel to the
WRITE GATE interface line and the other channel to TP2 (Erase gate
delay) on the PCBA MFD control #H.
Oscilloscope range: For both channels, DC mode, 5V, 100μsec

(b) Install a work disk and start the spindle motor.

(c) Execute the head loading.

(d) Set the oscilloscope to the negative trigger (-) mode. Make the
WRITE GATE signal TRUE (write command).

(e) Confirm that "t1" (Erase on delay) in Fig.422 is within the following
range.
FD-55AV ∿ FV: 200 ∿ 320μsec
FD-55GV: 175 ∿ 210μsec

(f) Set the oscilloscope to the positive trigger (+) mode. Make the
WRITE GATE signal FALSE.

(g) Confirm that "t2" (Erase off delay) in Fig.423 is within the following range.

    FD-55AV ∿ FV: 860 ∿ 950μsec

    FD-55GV: 500 ∿ 560μsec.
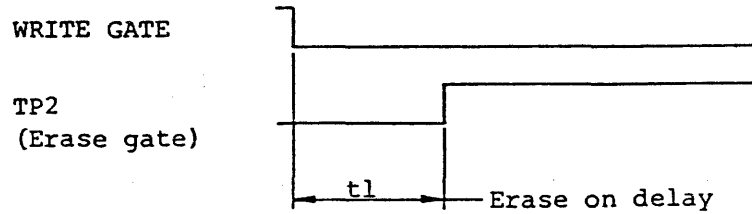
(Fig.422) Erase on delay
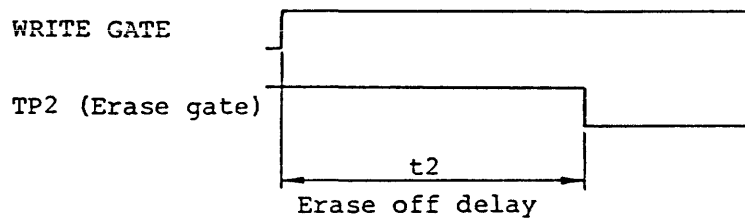
(Fig.423) Erase off delay

(2) SKA method

    (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch
        to the PSA side.

    (b) Install a work disk.

    (c) Start the spindle motor by key "5". (MON indicator turns on).

    (d) Execute drive select by key "0". (DS0 indicator turns on).

    (e) Key in "7". (WRITE GATE ON).

    (f) Confirm that the DATA indicator ⬜⬜⬜⬜ (μs) shows a value within the
        following range.
            Erase on delay, FD-55AV ∿ FV: 200 ∿ 320μsec
                            FD-55GV: 175 ∿ 210μsec

    (g) Key in "7" again. (WRITE GATE OFF)

    (h) Confirm that the DATA indicator ⬜⬜⬜⬜ (μs) shows a value within the
        following range.
            Erase off delay, FD-55AV ∿ FV: 860 ∿ 950μsec
                            FD-55GV: 500 ∿ 560μsec

4-4-8. Check and Adjustment of Head Touch

Note: The adjustment is applied only to a single sided FDD.

(A) Equipment

(1) Work disk

(2) Common screwdriver, small size

(3) SKA or user's system

(4) Oscilloscope (not required when the SKA is used)

(5) DC clip on ammeter (not required when the SKA is used)

(6) Locking paint

(B) Check and adjustment procedure

(1) General method

(a) Connect an oscilloscope to TP7 or TP8 (Differentiation amp.) on the
PCBA MFD control #H.
Oscilloscope range: AC mode, 0.1 ∿ 0.2V

(b) Install a work disk and start the spindle motor.

(c) Set the head to the innermost track.

(d) Execute the head loading.

(e) Repeat the cycle of one write rotation and one read rotation.
Write data should be the fixed pattern of 2F (250KHz of WRITE DATA
frequency for FD-55AV ∿ FV and 500KHz for FD-55GV).

(f) Write down the average read level measured during the read operation
of item (e).

(g) Execute item (e) and (f) with a slight depression (very slight depression easy to release: 10 ∿ 20g) by a finger on the top of the upper head (double sided) or of the pad arm (single sided), and measure the average read level as in item (f).

(h) Confirm that the read level measured in item (f) is greater than 80% of that in item (g).

(i) For a double sided FDD, execute items (e) through (h) respectively for side 0 and side 1 heads.

(j) After making the head move to track 00, execute items (e) through (i).

(k) Head touch adjustment for a single sided FDD:

    i) At the innermost track, turn the groove on the upper side of the head pad by 30° steps, approx. with a common screwdriver (see Fig.424). At each turning of the groove, execute write and read operations in item (e).
    Be sure to take apart the common screwdriver from the head pad during write or read operation.
    Note: Be careful not to push the head pad strongly with the common screwdriver. Also do not touch the pad surface to which a disk will be in contact.

    ii) After turning the pad position around 360°, set the position again to the position where the highest read level was obtained. Then execute items (e) through (h) at the innermost track.

    iii) Continue the operation until the item (h) is sufficiently satisfied. Following causes are assumed for the insufficient result in item (h) after fine adjustment of the pad position.

①Inferior head pad:

   Replace the pad according to item 4-5-12.

②Inferior disk:

   Disk and/or jacket is deformed or damaged. Replace the work
   disk with a new one.

③Inferior pressure of the jacket pads:

   If the jacket pad attached under the set arm (see Fig.505, Nos.4,
   5, 6) does not touch the disk jacket surface, replace the pads.

Caution: If the jacket surface is excessively pressed, it might be
          deformed or the spindle motor might be overloaded because
          of increasing the rotation torque. If item③is done,
          measure the +12V current consumption of the FDD and confirm
          that the current does not exceed 300mA by an DC clip-on
          ammeter. For a commercially available general disks, the
          desirable current is 250mA, Max.

④Inferior head:

   Replace the head carriage Ass'y according to item 4-5-1.

iv) Remove the work disk and apply a drop of locking paint around the
    rotating area of the head pad. Be careful not to smear the groove
    for common screwdriver with the locking paint.

(L) Possible causes for the insufficient head touch in a double sided FDD:

    Following causes are assumed for the insufficient result in items (h)
    through (j) on a double sided FDD.

    i) Inferior disk:
       Disk and/or jacket is deformed or damaged. Replace the work disk
       with a new one.

   ii) Inferior head flexture:
       Because of the failed performance of the arm lifter in item 4-4-3
       (model with head load solenoid) or the failed performance of the
       CSS Ass'y in item 4-4-4 (CSS model without head load solenoic),

Head pad ⌐   ⌐ Pad arm

Groove for common ⌐
      screwdriver

Locking paint ⌐
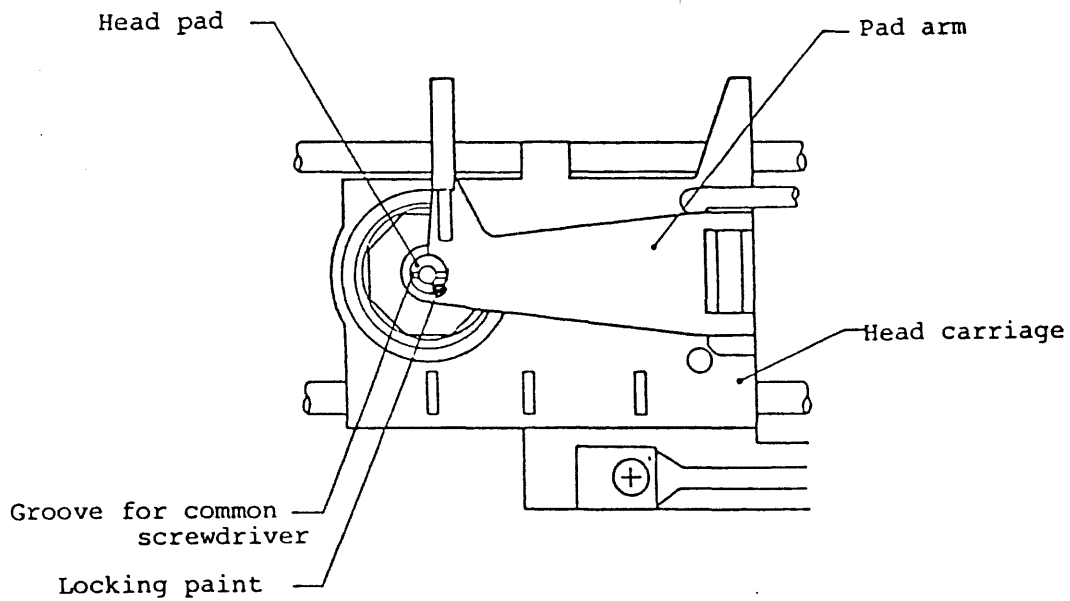
(Fig.424) Adjustment of head pad position (single sided FDD)

the flexture on which the head piece is located may be deformed.
Remove the disk. Then open and close the front lever slowly to
observe the gap between the side 1 and side 0 heads from the front
bezel. If the two head surfaces are not in parallel each other,
it is considered to be the deformation.
Replace the head carriage Ass'y according to item 4-5-1.
iii) Inferior pressure of the jacket pads:
    If the jacket pad attached under the set arm (see Fig.505, No.4
    and No.6) does not touch the jacket surface, replace the pads.

    Caution: If the jacket surface is excessively pressed by the pad
             No.6 (touch pad), it might cause wear out of the disk or
             the spindle motor might be overloaded because of increasing
             the rotation torque.

(2) SKA method

(a) Connect the SKA according to item 4-2-4 and set the FD PWR switch
    to the PSA side.

(b) Install a high density work disk.

(c) Start the spindle motor by key "5". (MON indicator turns on).

(d) Execute drive select by key "0". (DS0 indicator turns on).

(e) Key in "C0" and confirm that the TRACK indication becomes "00".
    (RECALIBRATE)

(f) Key in "C1". (SEEK TMAX)

(g) Key in "D3". (WRITE/READ LEVEL PRE 2F)

(h) Write 2F and read operations are repeated.
    The DATA indicator ▢▢▢▢ (mV) indicates the average read level
    of TP4 and TP5 (Pre-amp.) after each cycle of operation (one rotation
    of write and one rotation of read) is finished.

(i) Observe the DATA indicator ▢▢▢▢ (mV) with a slight depression
    (very slight depression easy to release: 10 ∿ 20g) by a finger on
    the top of the upper head.

(j) Confirm that the read level measured in item (h) is more than 80% of
    that in item (i).

(k) For a double sided FDD, depress "F" key to stop and then depress "4"
    key to execute items (g) through (j) for side 0 and side 1 heads
    respectively. The side is changed alternately by a depression of
    "4" key. If side 1 is selected, SIDE 1 indicator of the SKA turns on.

(L) Key in "C0" (RECALIBRATE) and execute items (g) through (k) in the
    similar way.

(m) Head touch adjustment for a single sided FDD:
    Refer to item (k) of "General method".
    +12V current consumption in item (k)-iii), "Caution" should be done
    as follows.

    i) Stop all the commands already input by depressing "F" key.
   ii) Key in "DF".   (+12V CURRENT)
  iii) Measure the +12V current consumption at that time by the DATA
       indicator ⬜⬜⬜ (mA).
   iv) Key in "F" after the measurement completes.   (STOP)

(n) Possible causes for the inferior head touch in a double sided FDD:
    Refer to item (L) of "General method".

4-4-9. Check and Adjustment of Asymmetry

(A) Equipment

(1) Common screwdriver, small size

(2) Work disk (for high density)

(3) SKA or user's system

(4) Oscilloscope

(B) Check and adjustment procedure

(1) General method

(a) Connect an oscilloscope to the READ DATA interface line.
Oscilloscope range: DC mode, 2V, 0.5 $\sim$ 1µsec

(b) Install a work disk and start the spindle motor.

(c) Set the head to the innermost track.

(d) Execute the head loading.

(e) Execute 1F write operation for one rotation of the disk (125KHz of
WRITE DATA frequency for FD-55AV $\sim$ FV and 250KHz for FD-55GV).

(f) Measure the asymmetry referring to Fig.425.

Note: Oscilloscope should be so set that three READ DATA pulses can be
observed. Asymmetry width should be measured at the second READ
DATA pulse from the trigger pulse.

(g) Confirm that the asymmetry is within the following range.
Innermost track 1F asymmetry, FD-55AV $\sim$ FV: 0.6µsec, Max.
FD-55GV: 0.3µsec, Max.

```
                ┌─┐      ┌╥┐┌─┐        ┌─┐┌─
READ DATA ──┐ ┌─┘ └──────┘║│└─┘────────┘ └┘
           └─┘            │║│
                          │║├── Asymmetry
                      ────┤║
                          │║
                      │   │╫── 1F interval
                      ├───────┤
                      │
           Trigger
```
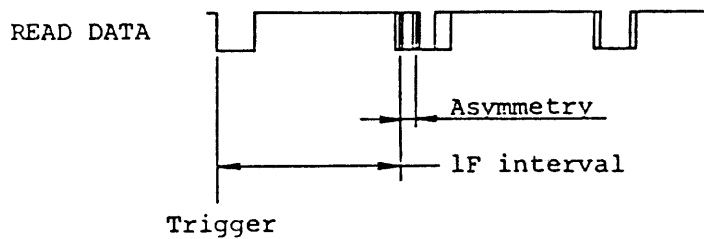
(Fig.425) Measurement of asymmetry

(h) For a double sided FDD, execute items (e) through (g) for side 0 and
    side 1 heads respectively.

(i) If the value in item (g) or (h) is out of the specified range, adjust
    according to the following procedure.

    i) Adjust the variable resistor, R1 on the PCBA MFD control #H so
       that the asymmetry takes a small value while repeating 1F write
       and 1F read operations alternately.

    ii) For a double sided FDD, repeat the operation in item i) for side 0
        and side 1 heads alternately. The variable resistor shall be so
        adjusted that both asymmetry for side 1 and side 0 heads take the
        minimum value.

(j) If the adjustment in item (i) cannot be done sufficiently, or it is
    too difficult to adjust, following causes are assumed.

    i) Leakage flux density in the environmental condition of the FDD
       is high:
       If there is some flux source near the FDD such as magnet,
       transformer, motor, Brown tube, magnetized iron plate, etc., take
       it apart from the FDD. Then measure the asymmetry and adjust again.

    ii) Inferior disk:
        Replace the work disk.

    iii) Inferior head:
         Replace the head carriage Ass'y according to item 4-5-1.

iv) Inferior PCBA MFD control #H:

Replace the PCBA according to item 4-5-7.

(2) SKA method

    (a) Connect the SKA according to item 4-2-4 and set the FD PWR switch
        to the PSA side.

    (b) Key in "B1F". (1F DUTY)

    (c) Connect an oscilloscope to the DOUT terminal of the SKA.
        Oscilloscope range: DC mode, 2V, 0.1 $\sim$ 0.2μsec

    (d) Install a work disk.

    (e) Start the spindle motor by key "5". (MON indicator turns on).

    (f) Execute drive select by key "0". (DS0 indicator turns on).

    (g) Key in "C0" and confirm that the TRACK indication becomes "00".
        (RECALIBRATE)

    (h) Key in "C1". (SEEK TMAX)

    (i) Key in "D4". (WRITE/READ LEVEL PRE 1F)

    (j) Measure the asymmetry as in Fig.426.
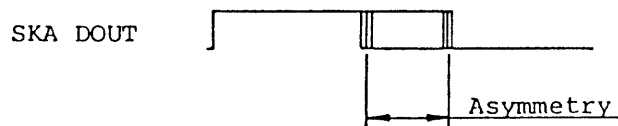
(Fig.426) Measurement of asymmetry

    (k) Confirm that the asymmetry is within the following range.

Innermost track 1F asymmetry, FD-55AV ∿ FV: 0.6µsec, Max.

FD-55GV: 0.3µsec, Max.

(L) For a double sided FDD, depress "4" key and execute items (i) through
(k) for side 0 and side 1 heads respectively. The side is changed
alternately by a depression of "4" key. If the side 1 is selected,
SIDE 1 indicator of the SKA turns on.

(m) If the value in item (k) or (L) is out of the specified range, adjust
according to the following procedure.

   i) Adjust the variable resistor, R1 on the PCBA MFD control #H so
      that the asymmetry takes a small value by keying in "D4".
  ii) For a double sided FDD, execute the operation in item i) for
      both sides alternately by changing the side by key "4". The
      variable resistor shall be so adjusted that both asymmetry for
      side 1 and side 0 heads take the minimum value.

(n) If the adjustment in item (m) cannot be done sufficiently, or if it
is too difficult to adjust, refer to item (j) of "General method".

4-4-10. Check of Read Level

(A) Equipment

(1) Level disk

(2) SKA or user's system

(3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP7 and TP8
(Differentiation amp.) on the PCBA MFD control #H.
Oscilloscope range: AC mode, 0.2 ∿ 0.5V
Set both channels, 1 and 2 to the above range. Set either of the
channels to Invert mode and Add both channels.

(b) Install a level disk and start the spindle motor.

(c) Set the head to the innermost track.

(d) Execute the head loading.

(e) Execute 2F write operation for one rotation of the disk (250KHz of
WRITE DATA frequency for FD-55AV ∿ FV and 500KHz for FD-55GV).

(f) Measure the average amplitude (Vp-p) of the read waveform as in
Fig.427.

(g) Calculate the read level by substituting the following expression
with the measured value in item .(f) and READ LEVEL calibration value
(see level disk label).
Read level (True value) = Measured value x 100/Calibration value(%)

TP 7, TP8 (Add)   Vp-p
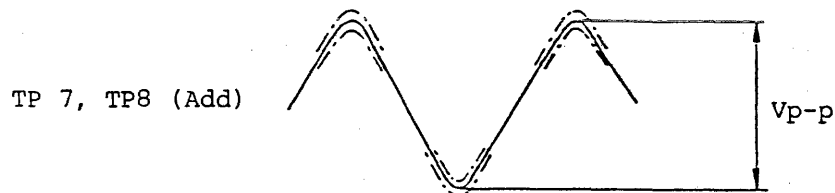
(Fig.427) Measurement of average read level (2F)

(h) Confirm that the true value of the read level is 0.8Vp-p, Min.

(i) For a double sided FDD, execute items (e) through (h) for side 0 and side 1 heads respectively.

(j) If the value in item (h) or (i) is out of the specified range, following causes are assumed.

   i) Inferior disk:
      Disk and/or jacket is deformed or damaged. Replace the level disk with a new one.
  ii) Abnormal disk rotational speed:
      Check for the speed according to item 4-4-6.
 iii) Inferior head touch:
      Check for the head touch according to item 4-4-8.
  iv) Inferior head:
      Replace the head carriage Ass'y according to item 4-5-1.
   v) Inferior PCBA MFD control #H:
      Replace the PCBA MFD control #H according to item 4-5-7.

(k) Eject the level disk and release the Invert and Add modes of the oscilloscope.

(2) SKA method

 (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch
   to the PSA side.

 (b) Install a level disk.

 (c) Start the spindle motor by key "5". (MON indicator turns on).

 (d) Execute drive select by key "0". (DS0 indicator turns on).

 (e) Key in "C0" and confirm that the TRACK indication becomes "00".
   (RECALIBRATE)

 (f) Key in "C1". (SEEK TMAX)

 (g) Key in "D7". (WRITE/READ LEVEL DIF 2F)
   Calibration value of the level disk should be set previously in the
   SKA.

 (h) Confirm that the DATA indicator ⬚⬚⬚ (mVo-p) indicates the value
   of 400mVo-p, Min.

 (i) For a double sided FDD, depress key "4" and execute items (g) and
   (h) for side 0 and side 1 heads respectively. The side is changed
   alternately by a depression of "4" key. If side 1 is selected, SIDE 1
   indicator of the SKA turns on.

 (j) If the value in item (h) or (i) is out of the specified range, refer
   to item (j) of "General method".

 (k) Eject the level disk.

4-4-11. Check of Resolution

(A) Equipment

(1) Level disk

(2) SKA or user's system

(3) Oscilloscope (not required when the SKA is used)

(B) Check procedure

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP4 and TP5
(Pre-amp.) on the PCBA MFD control #H.
Oscilloscope range: AC mode, 20mV $\sim$ 0.1V
Set both channels, 1 and 2 to the above range. Set either of the
channels to Invert mode and Add both channels.

(b) Install a level disk and start the spindle motor.

(c) Set the head to the innermost track.

(d) Execute the head loading.

(e) Execute 1F write operation for one rotation of the disk (125KHz of
WRITE DATA frequency for FD-55AV $\sim$ FV and 250KHz for FD-55GV).

(f) Measure the average amplitude (V1F) as in Fig.428.

(g) Execute 2F write operation as in item (e) (doubled in frequency to
that in item (e)).

(h) Measure the average amplitude (V2F) as in Fig.428.
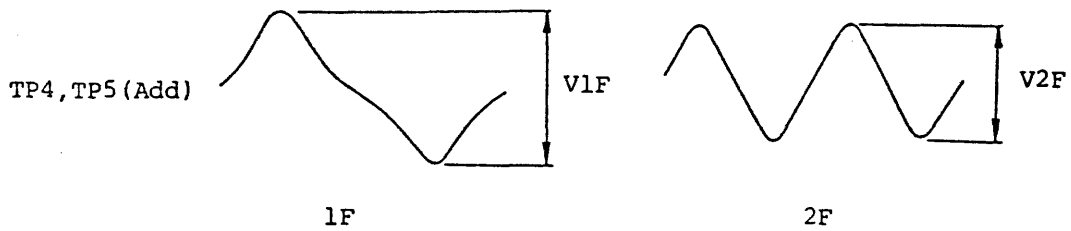
(Fig.428) Measurement of resolution

(i) Calculate the resolution by substituting the following expression
with the measured values V1F, V2F, and RESOLUTION calibration value
(see level disk label).

Resolution (true value) = V2F/V1F x 100/Calibration value (%)

(j) Confirm that the true value of resolution is within the following
range.
Innermost track resolution, FD-55AV, BV: 55%, Min.

FD-55EV, FV, GV: 60%, Min.

(k) For a double sided FDD, execute items (e) through (j) for side 0
and side 1 heads respectively.

(L) If the value in item (j) or (k) is out of the specified range,
following causes are assumed.

  i) Inferior disk:
Disk and/or jacket is deformed or damaged. Replace the level
disk with a new one.
 ii) Inferior disk rotational speed:
Check for the speed according to item 4-4-6.
iii) Inferior head touch:
Check for the head touch according to item 4-4-8.
 iv) Inferior head:

Replace the head carriage Ass'y according to item 4-5-1.

v) Inferior PCBA MFD control #H:

Replace the PCBA MFD control #H according to item 4-5-7.

(m) Eject the level disk and release the Invert and Add modes of the oscilloscope.

(2) SKA method

    (a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch
        to the PSA side.

    (b) Install a level disk.

    (c) Start the spindle motor by key "5". (MON indicator turns on).

    (d) Execute drive select by key "0". (DS0 indicator turns on).

    (e) Key in "C0" and confirm that the TRACK indication becomes "00".
        (RECALIBRATE)

    (f) Key in "C1". (SEEK TMAX)

    (g) Key in "D8". (RESOLUTION)
        The calibration value of the level disk should be set previously in
        the SKA.

    (h) Confirm that the DATA indicator ⊏⊤⊤⊤⊐ (%) indicates the value within
        the following range.
        Innermost track resolution, FD-55AV, BV: 55%, Min.
                                  FD-55EV, FV, GFV: 60%, Min.

    (i) For a double sided FDD, depress key "4" and execute items (g) and
        (h) for side 0 head and side 1 head respectively. The side is
        changed alternately by a depression of "4" key. If side 1 is
        selected, SIDE 1 indicator of the SKA turns on.

    (j) If the value in item (h) or (i) is out of the specified range, refer
        to item (L) of "General method".

    (k) Eject the level disk.

4-4-12. Check and adjustment of Track Alignment

(A) Equipment

(1) Cross point screwdriver, M3

(2) Alignment disk

(3) Alignment adjustment jig or M3 screw of 15mm long

(4) SKA or user's system

(5) Oscilloscope

(6) Hygrometer

(7) Locking paint

(B) Check and adjustment procedure

Note: Check and adjustment of track alignment should be done in an environment of general room temperature and humidity. Even if the environmental condition is within the specified operational condition extreemly high or low temperature, or extreemly high or low humidity shall be avoided. Check and adjustment should be done after two hours, Min. of storing in the above mentioned condition.
It is recommended that the orientation of the FDD for the track alignment check is the same as when the FDD is actually installed in the user's system.

(1) General method

(a) Use two channels of an oscilloscope and connect them to TP7 and TP8 (differentiation amp.) on the PCBA MFD control #II. Also connect the external trigger of the oscilloscope to TP1 (Index) and apply positive trigger.
Oscilloscope range: AC mode, 0.2 ∿ 0.5V, 20msec
Set both channels, 1 and 2 to the above range. Set either of the channels to Invert mode and Add both channels.

(b) Install an alignment disk and start the spindle motor.

(c) Execute the head loading.

(d) Set the head to the following alignment check track.
    Alighment check track, 48tpi (FD-55AV, BV): Track 16
                           96tpi (FD-55EV, FV, GV): Track 32

(e) Confirm that two lobe patterns as in Fig.429 can be observed (it is not necessary that the levels of VA and VB are equal).

TP7 and TP8 (Add)

48tpi

96tpi
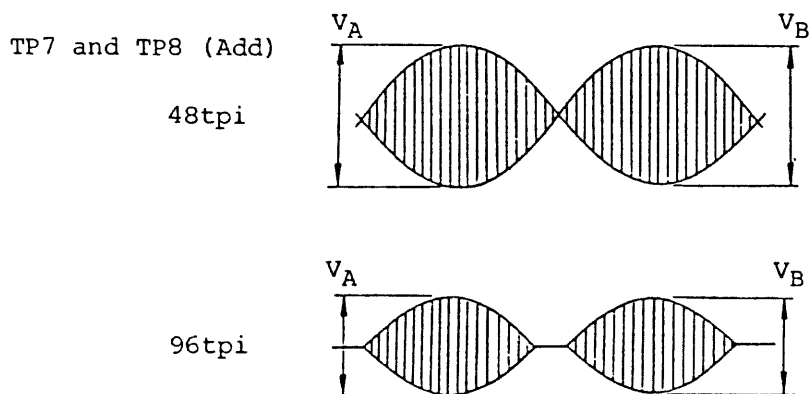
(Fig.429) Alignment check lobe pattern

If only one lobe pattern can be observed or if two lobes become one pattern, the head is not on the alignment check track.
In such event, execute step-out or step-in for the following tracks' space to obtain the most similar waveform to that in Fig.429.
        48tpi: 2 tracks
        96tpi: 4 tracks

Note: The above number of tracks to be stepped is required to make the alignment track position be fit with the magnetized condition of the basic magnetized phase "A" of the stepping motor. If the stepped track numbers are inassured, set it again from track 00 (TRACK 00 output signal becomes TRUE).

For a 48tpi FDD, the lobe pattern in Fig.429 shall be observed at the even track, while it shall be observed at the track of multiple number of four for a 96tpi FDD.

(f) After one or several step-outs from the check track, step in the head to the check track again and measure VA and VB at that time.

(g) Calculate the true value of misalignment by substituting the value in item (f) and ALIGNMENT calibration value (see alignment disk label, attention to the side).

$$\text{Misalignment(true value)} = \left(\frac{VA-VB}{\text{Larger value in VA \& VB}} \times 100 - \text{Calibration value} \right) - (\text{Relative humidity}-50) \times K$$

"K" is humidity compensation factor.

    48tpi: K=0.26
    96tpi: K=0.42

e.g. 96tpi, VA=0.58V, VB=0.61V, Calibration value=-6(%)
    Relative humidity= 65%:

$$\text{Misalignment(true value)} = \left\{ \frac{0.58 \times 0.61}{0.61} \times 100-(-6) \right\} - (65-50) \times 0.42 \simeq -5.2(\%)$$

If the calculated value is positive, the magnetic head is shifted inward from the reference position, while the head is shifted outward from the reference position when the value is negative.

(h) Conversely, measure VA and VB when the head is on the alignment check track by stepping-out after one or several step-ins.

(i) Calculate the true value of misalignment as described in item (g).

(j) Confirm that both of the calculated values in items (a) and (i) are within the following range.
True value of misalignment: 30%, Max.

(k) For a double sided FDD, execute items (d) through (j) for side 0 and side 1 heads respectively.

(L) If the value in item (j) or (k) is out of the specified range, adjust the track alignment according to the following procedure:

   i) Loosen two fixing screws of the stepping motor a little.
   ii) Insert the alignment adjustment jig or M3 screw from the back side of the FDD as shown in Fig.430.
   iii) Repeat step-in and step-out operations and adjust the misalignment to be the smallest on the alignment check track during both step-in and step-out operations by turning the jig or the screw (stepping motor moves little by little).

   Note: When you adjust the alignment by observing the lobe pattern using the oscilloscope, pay attention to the calibration value on the alignment disk label and the ambient relative humidity.

   ① Calibration value + (Relative humidity - 50) x K $\geq$ 0:
   When the left side lobe pattern level, VA is assumed as "1", lobe pattern ratio should be so adjusted that the right side lobe pattern level VB takes the following value:

   $$VB = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

   ② Calibration value + (Relative humidity - 50) x K $\geq$ 0:
   When the right side lobe pattern level, VB is assumed as "1", lobe pattern ratio should be so adjusted that the left side lobe pattern level VB takes the following value.

$$VA = 1 - \frac{\text{Calibration value} + (\text{Relative humidity} - 50) \times K}{100}$$

e.g. 96tpi, Calibration value = -6%, Relative humidity = 35%:

-6 + (35 - 50) x 0.42 = -12.3 < 0

$$VA = 1 - \frac{-6 + (35 - 50) \times 0.42}{100} = 0.88$$

Therefore, the target value of VA when VB is assumed as "1"
is 0.88.

iv) For a double sided FDD, repeat the adjusting operation in item
iii) alternately for side 0 and side.1 heads until the both
misalignment take the smallest value.

v) Tighten the two fixing screws of the stepping motor little by
little for adjusting the true value of misalignment after
tightening the screws with the specified torque to be within ±20%.

vi) Remove the alignment disk.

vii) Apply a drop of locking paint to the head of the stepping motor
fixing screws.

viii) Check and adjust the track 00 sensor according to item 4-4-13.

ix) Check or adjust the track 00 stopper according to item 4-4-14.

(m) Release the Invert and Add modes of the oscilloscope.

Stepping motor

Alignment adjustment jig
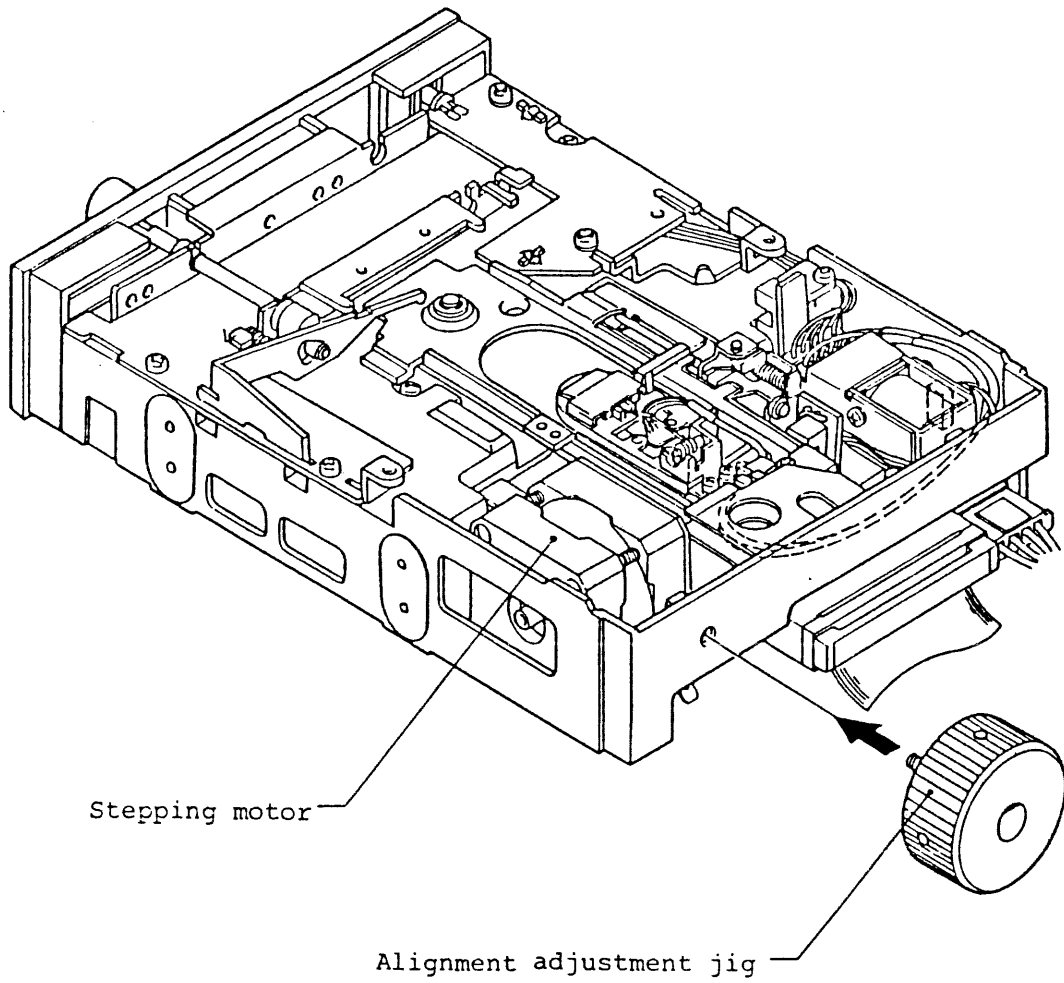
(Fig.430) Adjustment of track alignment

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to
    the PSA side.

(b) Use two channels of an oscilloscope. Connect the 1st channel to the
    DOUT terminal of the SKA and the 2nd channel to the DIF terminal
    of the SKA. Apply positive trigger by DOUT terminal.
    Oscilloscope range
        The 1st channel: DC mode, 2V, 20msec
        The 2nd channel: AC mode, 0.2 ∿ 0.5V, 20msec

(c) Key in "B9F". (INDEX observation)

(d) Install an alignment disk.

(e) Start the spindle motor by key "5". (MON indicator turns on).

(f) Execute drive select by key "0". (DS0 indicator turns on).

(g) Key in "C0" and confirm that the TRACK indication becomes "00".
    (RECALIBRATE)

(h) Set the head to the alignment check track by the following operation:
    48tpi (FD-55AV,BV): Key in "C2 16" and confirm that the TRACK
                        indication becomes "16".
    96tpi (FD-55EV, FV, GV): Key in "C2 32" and confirm that the TRACK
                        indication becomes "32".

(i) Confirm that two lobe patterns as in Fig.429 can be observed by the
    oscilloscope (it is not necessary that the levels of VA and VB are
    equal).
    If only one lobe pattern can be observed or if two lobes become one
    pattern, the head is not on the alignment check track.

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In such event, execute step-in or step-out of the following tracks' space to obtain the most similar waveform to that in Fig.429. Step operation can be done by key "8" (STEP-IN) and key "9" (STEP-OUT). By a depression of these keys, head will move for one track space.

    48tpi: 2 tracks

    96tpi: 4 tracks

Note: The above number of tracks to be stepped in required to make the alignment track position be fit with the magnetized condition of the basic magnetized phase "A" of the stepping motor.
For a 48tpi FDD, the lobe pattern shall be observed at the even track, while it shall be observed at the track of multiple number of four for a 96tpi FDD.

(j) For a 96tpi FDD, the following steps shall be done under the turn on condition of the H GAIN indicator in order to improve the measurement accuracy and switching of humidity coefficient. Turn on the H GAIN indicator by depressing "DD" key.
For a 48tpi FDD, confirm the H GAIN indicator is off. If it is on, turn it off by depressing "DD" key.

(k) Key in "E3". (ALIGNMENT)
Calibration value of the alignment disk and environmental relative humidity should be set previously in the SKA.

(L) Confirm all the indications on the DATA ⊏⊐⊐⊐⊐ (%) indicator are within ±30%.
The initial digit of the DATA indicator is the symbol. ⊢ (+) mark indicates that the head is shifted inward from the reference position, while − mark indicates that the head is shifted outward.

(m) For a double sided FDD, execute the same check for side 1 head according to the following procedure.

i) Key in "0" following the operation of item (L) (during execution
   of E3 command) and confirm that SIDE 1 indicator turns on.

ii) Confirm as in item (L).

Note: In order to change the head to side 0, key in "0" again.
      (SIDE 1 indicator turns off).

(n) Depress "F" key. (STOP)

(o) If the value in item (L) or (m) is out of the specified range, adjust
    the track alignment according to the following procedure.

    i) Loosen the two fixing screws of the stepping motor a little.

   ii) Insert the alignment adjustment jig or M3 screw from the back
    side of the FDD as shown in Fig.430.

  iii) Key in "E3" and adjust the jig or M3 screw so that the DATA
    indicator ⬜⬜⬜ (%) shows the smallest value. The stepping motor
    moves little by little when the jig or the screw is turned.

   iv) For a double sided FDD, repeat the adjusting operation in item iii)
    alternately for side 0 and side 1 heads until the both misalignment
    take the smallest value.

    v) Tighten the two fixing screws of the stepping motor little by
    little to obtain the value within ±20% on the DATA indicator when
    the screws are tightened with the specified torque.

   vi) Remove the alignment disk.

  vii) Apply a drop of locking paint on the screw head of the stepping
    motor fixing screws.

 viii) Check and adjust the track 00 sensor according to item 4-4-13.

   ix) Check or adjust the track 00 stopper according to item 4-4-14.

(p) Release the Invert and Add modes of the oscilloscope.

(q) If the H GAIN indicator of the SKA is on, key in "DD" again to turn
    off the H GAIN indicator of the SKA.

4-4-13. Check and Adjustment of Track 00 Sensor

(A) Equipment

(1) Cross point screwdrivers, M2.6, M3

(2) Work disk

(3) Alignment disk

(4) SKA or user's system

(5) Oscilloscope (or digital voltmeter)

(6) Locking paint

(B) Check and adjustment procedure

Note: Check and adjustment of the track 00 sensor using this general
method is not so precise. It is recommended to use the SKA method
in item (2) as much as possible.

(1) General method

(a) Connect an oscilloscope or a digital voltmeter to TP3 (Track 00
sensor) on the PCBA MFD control #H.
Oscilloscope range: DC mode, 1V

(b) Install a work disk and start the spindle motor.

(c) Execute the head loading

(d) Confirm that the voltage at TP3 is within the following range when the
head is set to track 00.
Track 00 position TP3 voltage: 3.7V, Min.

(e) Turn the power off of the FDD and then turn it on again. Confirm
that the stop position of the head carriage did not change at power
off and on. This item aims to confirm that the track 00 position

matches the basic magnetized phase A of the stepping motor.

(f) Set the head to the following track.
    48tpi (FD-55AV, BV): Track 02
    96tpi (FD-55EV, FV, GV): Track 04

(g) Confirm that the voltage at TP3 is within the following range at
    the track position in item (f).
    TP3 voltage at track 02 (48tpi) or 04 (96tpi): 0.5V, Max.

(h) If the value in item (d), (e), or (g) is out of the specified range,
    adjust the position of the track 00 sensor according to the following
    procedure.

    i) If the track 00 stopper (small metal parts) is equipped, loosen
       the fixing screw of the stopper (see Fig.433) and shift the
       stopper in the step-out direction (make apart from the rear side
       of the head carriage).
    Note: If the V-type carriage (refer to Table 505) is mounted, the
          track 00 stopper is not equipped. Item i) is not required for
          this case.
    ii) Connect the oscilloscope to TP7 or TP8 (Differentiation amp.)
        of the PCBA MFD control #H.
        Oscilloscope range: AC mode, 0.2 ∿ 0.5V, 20msec
    iii) Install an alignment disk. The track alignment should be adjusted
         correctly according to item 4-4-12.
    iv) Make the head move to the position where the lobe pattern as in
        Fig.429 can be observed.
    v) Remove the alignment disk.
    vi) Connect the oscilloscope or digital voltmeter to TP3 (Track 00
        sensor) on the PCBA MFD control #H.
        Oscilloscope range: DC mode, 1V
    vii) Step out the head for the following space from the position where
         the normal lobe pattern is observed.

48tpi: 15 tracks (the head will be on track 01)

96tpi: 30 tracks (the head will be on track 02)

viii) Install a work disk.

. ix) Loosen the fixing screw of the track 00 sensor (see Fig.431) and move the sensor a little so that the voltage at TP3 falls within the following range.

TP3 voltage at track 01 (48tpi) or track 02 (96tpi):

1V ∿ 3V (2V, approx. center)

x) Confirm the items (d) through (g).

xi) Adjust the track 00 sensor position so that the values in items (ix) and (x) satisfy the specification when the screw has been tightened with the specified torque (3Kg.cm).

xii) If the track 00 stopper is equipped, adjust the track 00 stopper according to item 4-4-14.
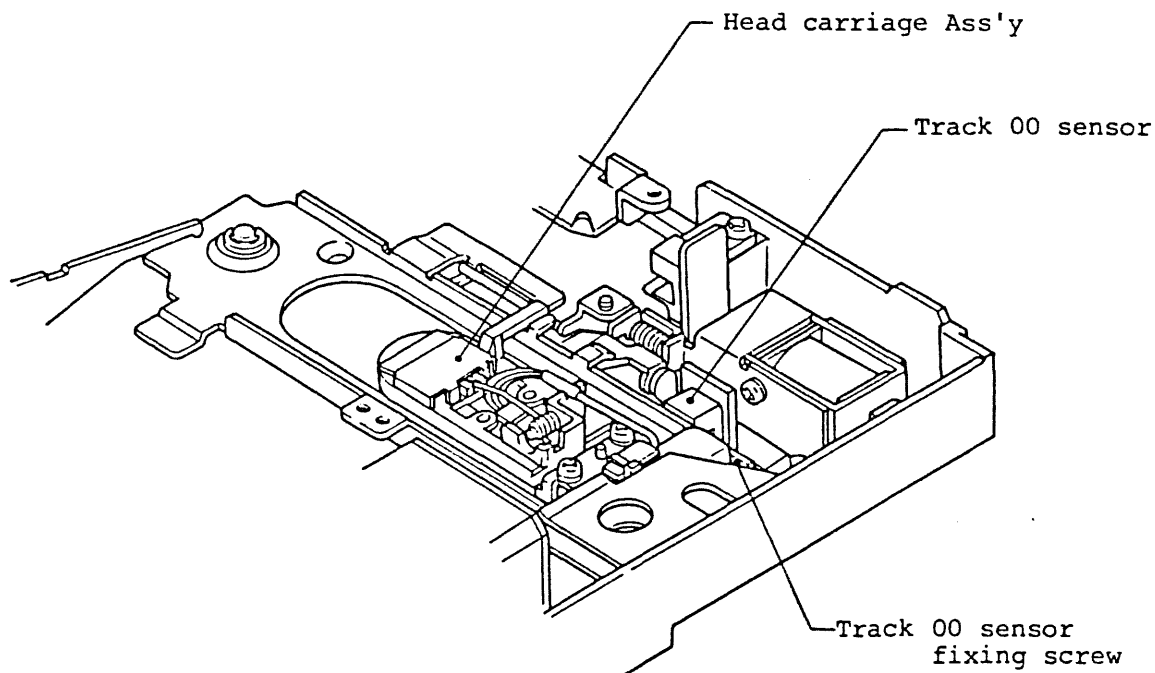
(Fig.431) Adjustment of track 00 sensor

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to
    the PSA side.

(b) Use two channels of socilloscope and connect them as follows:

    i) The 1st channel: SKA DOUT terminal

                        DC mode, 5V, 5 ~ 10msec
   ii) The 2nd channel: PCBA MFD control #H TP3 (Track 00 sensor),

                        2V range
  iii) External trigger: DIRECTION SELECT interface signal (Interface

                        connector pin No.18) or pin 3 of J3 (resistor

                        network RA1 for terminator) on the PCBA MFD

                        control #H

                        (+) trigger.

(c) Key in "B8 F".   (STEP observation)

(d) Install a work disk and start the spindle motor by key "5".
    (MON indicator turns on).

(e) Execute drive select by key "0".   (DS0 indicator turns on).

(f) Set the step rate and the settling time as follows referring to item
    4-2-4-3.
        48tpi (FD-55AV, BV): Step rate 6msec, Settling time 15msec
        96tpi (FD-55EV, FV, GV): Step rate 3msec, Settling time 15msec

(g) Key in "C0" and confirm that the TRACK indication becomes "00".
    (RECALIBRATE)

(h) Key in "C5".   (T00 TIMING, SEEK ±5)

(i) Measure the timing of points A and B and the voltages VL and VH

referring to Fig.432. The values should be with the following range.

TP3 clip timing, A: tA in Fig.432.

TP3 clip timing, B: tB in Fig.432.

TP3 voltage, VL: 0.5V, Max.

TP3 voltage, VH: 3.7V, Min.

Step-out

DIRECTION SELECT
(External trigger)

Step-in

SKA DOUT

1 2 3 4 5   1 2 3 4 5

VH

A

B

TP3
(Track 00 sensor)

VL

2V

0V

48tpi

tA
0∿4ms

tB
+3∿-1ms

Track 00
detection

1 2 3 4 5   1 2 3 4 5

SKA DOUT

VH

A

B

TP3
(Track 00 sensor)

VL

2V

0V

tA
0∿4ms

tB
0∿4ms

96tpi

Track 00 detection
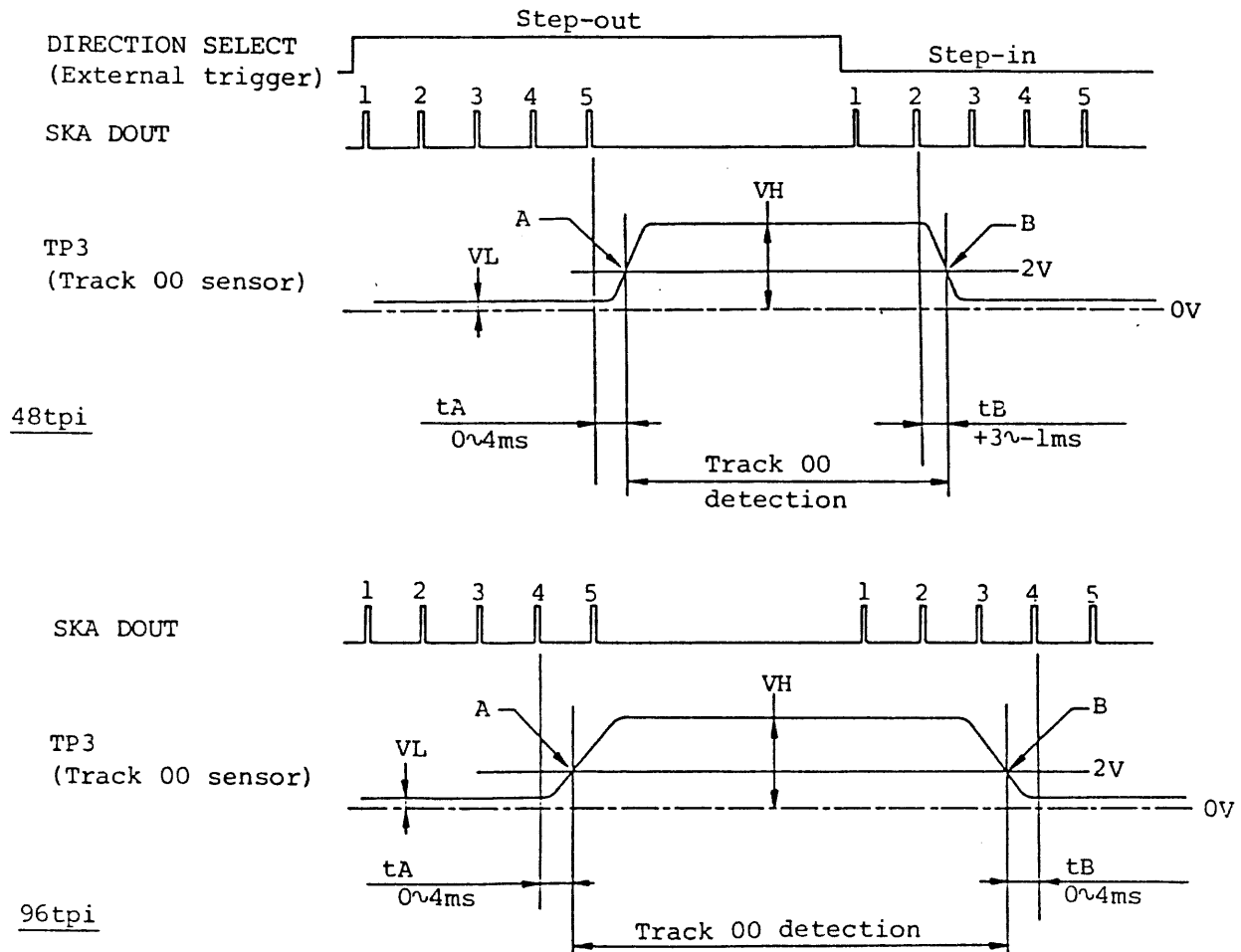
Note: VL and VH shall be smooth without undulations

(Fig.432) Track 00 sensor output waveform

(j) Key in "F". (STOP)

(k) Turn the FD PWR switch of the SKA off at the track 00 position and
then set it again to the PSA side. Confirm that the stop position
of the head carriage did not change at power off and on.

(L) If the value in item (i) or (k) is out of the specified range, adjust
the position of the track 00 sensor according to the following
procedure.

i) If the track 00 stopper (small metal parts) is equipped, loosen
the fixing screw of the stopper (see Fig.433) and shift the stopper
in the step-out direction (make apart from the rear side of the
head carriage).

Note: If the V-type carriage (refer to Table 505) is mounted, the
track 00 stopper is not equipped. Item i) is not required for
this case.

ii) Connect the 2nd channel of the oscilloscope to TP7 or TP8
(Differentiation amp.) of the PCBA MFD control #H and change the
trigger to this channel.
Oscilloscope range: AC mode, 0.2 ～ 0.5V, 20msec

iii) Install an alignment disk. The track alignment should be correctly
adjusted according to item 4-4-12.

iv) Key in "C0" and confirm that the track indicator becomes "00".
(RECALIBRATE).

v) Key in the following number and confirm that two lobe patterns as
in Fig.429 can be observed.
    48tpi: C2 16
    96tpi: C2 32
If normal lobe pattern cannot be observed, move the head to the
track position where the typical lobe pattern can be observed by
stepping in by key "8" or by stepping out by key "9".

vi) Remove the alignment disk.

vii) Key in the following number. (SET TRACK NUMBER)
    48tpi: E4 16
    96tpi: E4 32

viii) Key in "C2 00". (SEEK 00)

   Don't key in "C0". (RECALIBRATE)

ix) Change the connection of the oscilloscope as in item (b).

x) Key in "C5". (T00 TIMING SEEK ±5)

xi) Loosen the fixing screw of the track 00 sensor (see Fig.431) and adjust the sensor position where the requirements in item (i) are all satisfied.

xii) Repeat the adjustment so that the values in item (i) fall within the specified range when the fixing screw has been tightened with the specified torque (3Kg.cm).

xiii) If the track 00 stopper is equipped, adjust the track 00 stopper according to item 4-4-14.

4-4-14. Check and Adjustment of Track 00 Stopper

If V-type carriage (see Note 12 and Table 505 in item 5-2-1) is used, adjustment of this item is not required.

(A) Equipment

(1) Cross point screwdriver, M3
(2) SKA or user's system

(B) Check and adjustment procedure

(1) General method

(a) Set the head to track 00.

(b) Step out the head from the track 00 position.

(c) Confirm that the head carriage does not move by the step-out command (head carriage rests on track 00).

(d) Confirm that the gap between the head carriage and the extreme end of the track 00 stopper is 0.1 ∿ 0.45mm. (See Fig.433).
If the V-type carriage is mounted, the track 00 stopper (small metal parts) is not equipped and the frame protruding point works like as a stopper.

(e) Repeat step-in and step-out operations between track 00 and track 05. Confirm that no impact sound can be heard between the head carriage and the track 00 stopper.

(f) Turn off the FDD power and depress the head carriage lightly against the track 00 stopper with fingers. (See Fig.433).

(g) Confirm that the head carriage automatically returns to the initial position (track 00) when the power is turned on again.

(h) If the small parts for track 00 stopper is equipped (for L-type carriage, refer to Table 504), and if any one of the items (d) through (g) is not satisfied, adjust the track 00 stopper position according to the following procedure.

   i) Set the head to track 00.

  ii) Loosen the fixing screw of the track 00 stopper. (See Fig.433).

 iii) Adjust the stopper position so that the gap between the stopper and the head carriage becomes 0.25mm, approx. And then tighten the screw with the specified torque.

  iv) Execute items (a) through (g).
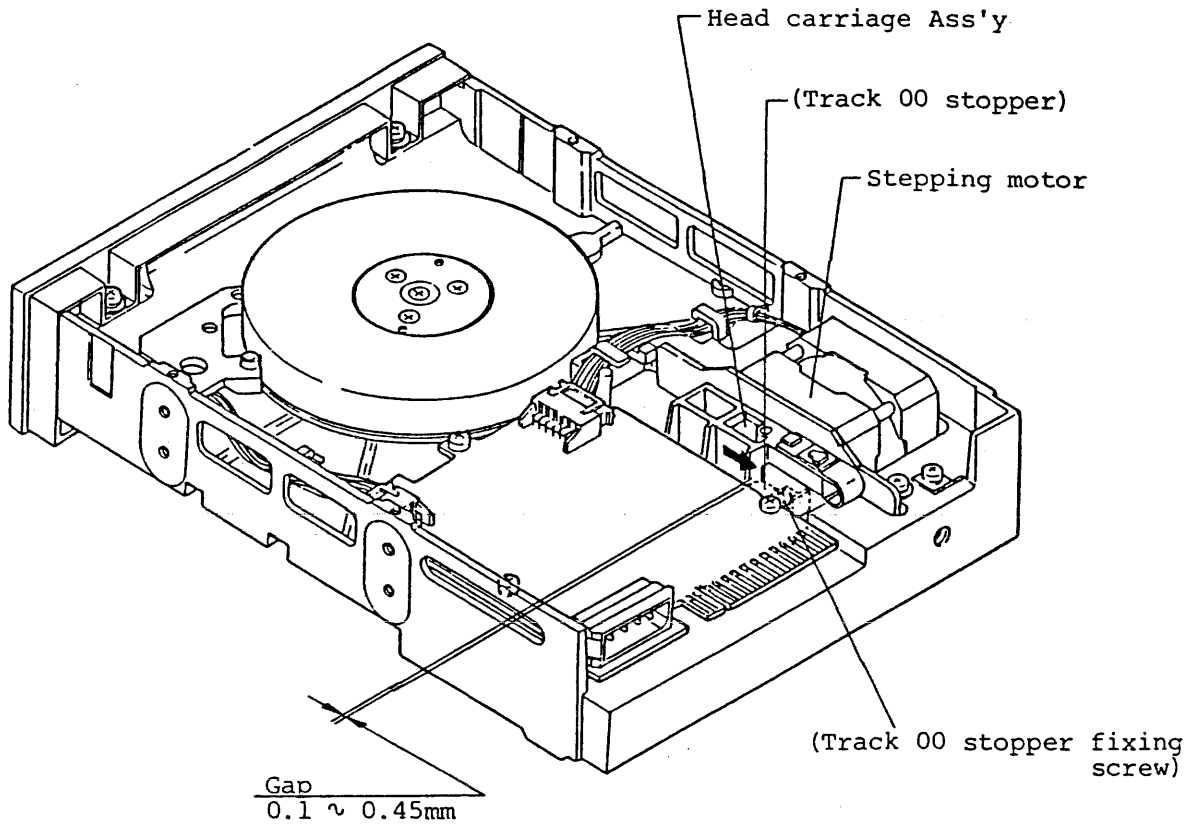
Note: Track 00 stopper (small metal parts) is not equipped if the V-type carriage is mounted. For this case, frame protruding point works like as a stopper.

(Fig.433) Check and adjustment of track 00 stopper

(2) SKA method

    (a) Connect the SKA referring to item 4-2-4 and set the FD PWR
        switch to the PSA side.

    (b) Execute drive select by key "0". (DS0 indicator turns on).

    (c) Key in "C0" and confirm that the TRACK indication becomes "00".
        (RECALIBRATE)

    (d) Set the step rate and the settling time as follows referring to item
        4-2-4-3.
        48tpi (FD-55AV, BV): Step rate 6msec, Settling time 15msec
        96tpi (FD-55EV, FV, GV): Step rate 3msec, Settling time 15msec

    (e) Key in "9". (STEP OUT)

    (f) Confirm that the head carriage does not move even if "9" is keyed in
        (head carriage rests on track 00).

    (g) Confirm that the gap between the head carriage and the extreme end
        of the track 00 stopper is 0.1 ∿ 0.45mm. (See Fig.433).
        If the V-type carriage is mounted, the track 00 stopper (small metal
        parts) is not equipped and the frame protruding points works like as
        a stopper.

    (h) Key in "C0" and key in "C5". (STEP TIMING, SEEK ±5)

    (i) Confirm that no impact sound can be heard between the head carriage
        and the track 00 stopper.

    (j) Turn off the FD PWR switch of the SKA and depress the head carriage
        lightly against the track 00 stopper. (See the arrow mark in Fig.433).

(k) Confirm that the head carriage automatically returns to the initial
    position (track 00) when the FD PWR switch is set to the PSA side
    again.

(L) If the small parts for track 00 stopper is equipped (for L-type
    carriage, refer to Table 504), and if any one of the items (g)
    through (k) is not satisfied, adjust the track 00 stopper position
    according to the following procedure.

  i) Key in "C0" and confirm that the TRACK indication becomes "00".
     (RECALIBRATE)
 ii) Loosen the fixing screw of the track 00 stopper. (See Fig.433).
iii) Adjust the stopper position so that the gap between the stopper
     and the head carriage becomes 0.25mm, approx.
     And then tighten the screw with the specified torque.
 iv) Execute items (a) through (k).

4-4-15. Check and Adjustment of Index Burst Timing

(A) Equipment

  (1) Cross point screwdriver, M3

  (2) Alignment disk

  (3) SKA or user's system

  (4) Oscilloscope (not required when the SKA is used)

(B) Check and adjustment procedure

  (1) General method

    (a) Use two channels of an oscilloscope. Connect the 1st channel to TP1
        (index) on the PCBA MFD control #H and the 2nd channel to TP4 or TP5
        (Pre-amp.). Apply positive trigger by TP1.
        Oscilloscope range
                The 1st channel: DC mode, 2V, 50μsec
                The 2nd channel: AC mode, 0.5V, 50μsec

    (b) Install an alignment disk and start the spindle motor.

    (c) Execute the head loading.

    (d) Set the head to the following track:
            48tpi (FD-55AV, BV): Track 01
            96tpi (FD-55EV, FV, GV): Track 02

    (e) Measure "t" in Fig.434.

    (f) Substitute the following equation with the measured value in item
        (e) and INDEX TIMING calibration value (see alignment disk label).

        Index burst timing (true value) = Measured value - Calibration value
                                                                          (μs)

```
TP1 (Index) ___|‾‾‾‾‾‾‾‾‾‾‾‾|_____

TP4 or TP5  ___|‖ΛΛΛ_____

              | t |  Index burst delay
```
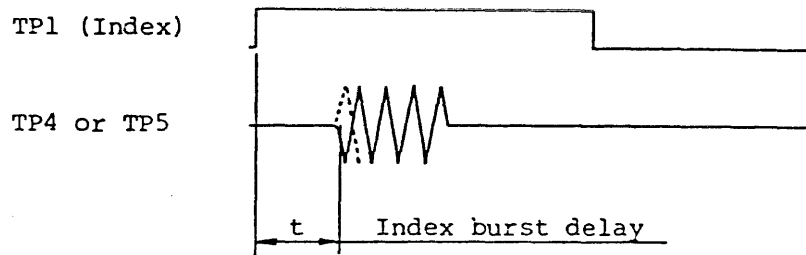
(Fig.434) Index burst timing

(g) Confirm that the true value of the index burst timing is within the
following range.

FD-55AV ∿ FV: 200 ± 200μsec

FD-55GV: 165 ± 165μsec

(h) If the value in item (g) is out of the specified range, adjust the
index sensor Ass'y position according to the following procedure.

i) Loosen the fixing screws (see Fig.435) of the PCBA front OPT #H
and adjust its position to make the true value of the index burst
timing fall in the specified range in item (g).

ii) Repeat the adjustment so that the true value of the index burst
timing falls in the range of item (g) when the fixing screw has
been tightened with the specified torque (4.5Kg.cm).

(i) Remove the alignment disk.

PCBA front OPT fixing screws

Adjusting direction of
sensor

PCBA front OPT #H
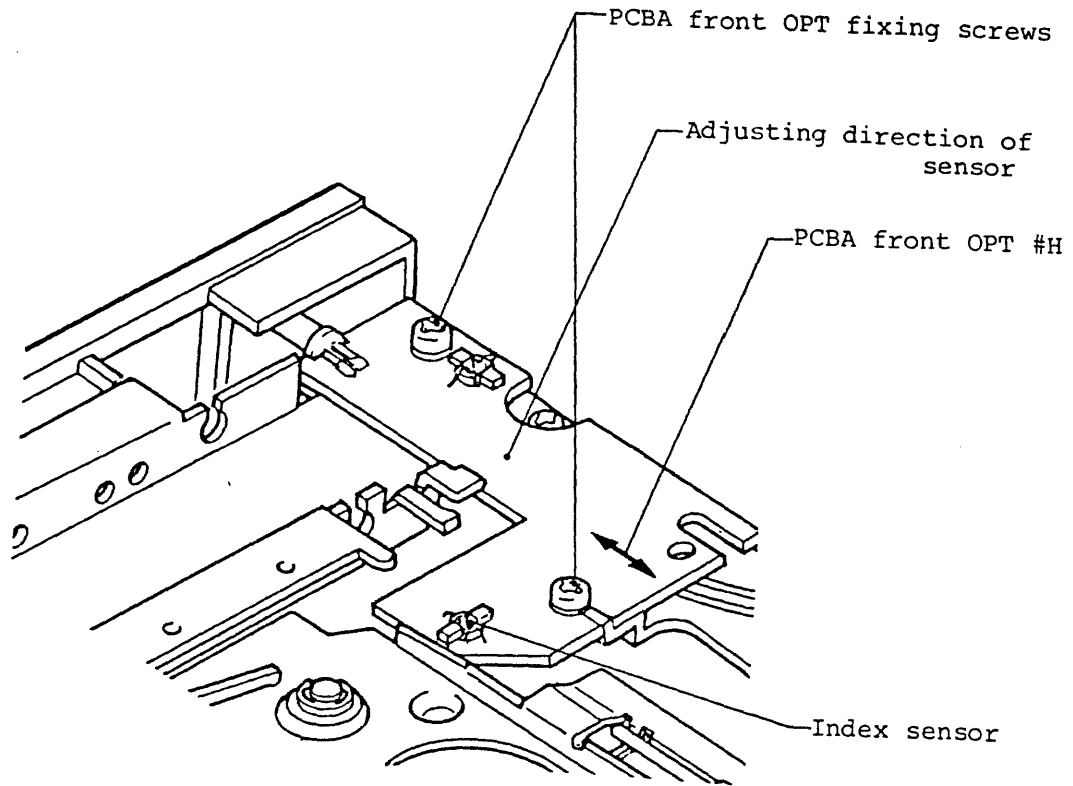
Index sensor

(Fig.435) Adjustment of index sensor

(2) SKA method

(a) Connect the SKA referring to item 4-2-4 and set the FD PWR switch to the PSA side.

(b) Install an alignment disk.

(c) Start the spindle motor by key "5". (MON indicator turns on).

(d) Execute drive select by key "0". (DS0 indicator turns on).

(e) Key in "C0" and confirm that the TRACK indication becomes "00". (RECALIBRATE)

(f) Set the head to the index check track by the following operation:
    48tpi (FD-55AV, BV): Key in "C2 01" and confirm that the TRACK
                         indication becomes "01".
    96tpi (FD-55EV, FV, GV): Key in "C2 02" and confirm that the TRACK
                         indication becomes "02".

(g) Key in "E6". (INDEX TIMING)
    The calibration value of the index timing should be set previously in the SKA.

(h) Confirm that the DATA indicator ☐☐☐☐ (μs) indicates the value within the following range.
    FD-55AV ∿ FV: 200 ± 200μsec
    FD-55GV: 165 ± 165μsec

(i) Key in "F". (STOP)

(j) If the value in item (h) is out of the specified range, adjust the index sensor Ass'y position according to the following procedure

i) Loosen the fixing screws (see Fig.435) of the PCBA front OPT #H
     and its position so that the DATA indication under execution of
     item (g) shows the median value in the specified range of item (h).
 ii) Repeat the adjustment so that the DATA indication takes the median
     value when the fixing screw has been tightened with the specified
     torque (4.5Kg.cm)
iii) Depress "F" key. (STOP)

(k) Remove the alignment disk.

4-5. MAINTENANCE PARTS REPLACEMENT

4-5-1. Replacement of Head Carriage Ass'y

There are two types of the head carriage Ass'y for a double sided FDD.
One is V-type carriage (refer to Table 505) and the other is L-type
carriage (refer to Table 504). Both of them are different in replacing
method. For a single sided FDD, only L-type carriage is used.

4-5-1-1. Replacement of V-type carriage

(A) Equipment

(1) Cross point screwdriver, M3

(2) Common screwdriver, small size

(3) A pair of tweezers

(4) Alcohol and gauze

(5) Locking paint

(6) Oil (FLOIL 946P)

(7) SKA or user's system

(8) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect the head connector (J9) and remove the head cable from the
    cable guide (Fig.505, No.11).

(2) Remove the set arm sub Ass'y (Fig.505, No.3) by removing the two fixing
    screws (Fig.505, S8).

(3) Turn the FDD over so that the spindle motor side (bottom side) goes up.
    Depress A point of the steel belt (Table 505, No.23C) in Fig.436 in
    the direction of arrow mark using a common screwdriver or rear end of
    a tweezers, to make the locking paint 1 free.

Belt hook 1 ─┐   ┌─ Locking paint 1

Locking paint 2─┐   ┌─ Steel belt

                                    ┌─Step (4)
                                    ─Belt spring

Locking paint 3 ─┘   Step (3)
                  └─Spring guide
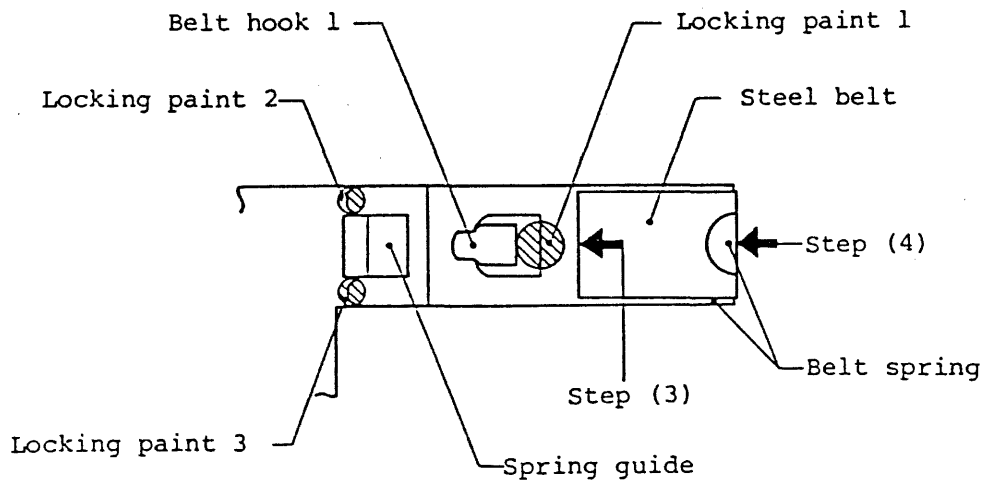
(Fig.436) Belt hook area in the back side of V-type carriage

(4) Depressing B area of the belt spring (Table 505, No.23d) and steel belt
    in Fig.426 with fingers in the direction of arrow mark, remove the steel
    belt from the belt hook 1 of the carriage using a pair of tweezers.

(5) Make the belt spring slide in the reverse direction of the arrow mark
    in Fig.436 using a pair of tweezers, and make the locking paint 2 and
    3 free. Then remove the belt spring from the spring guide of the
    carriage.

(6) Place the FDD so that the top side comes up. Pull C point of the steel
    belt in the direction of arrow mark in Fig.437 using a pair of tweezers
    to make the locking paint 4 free. Then remove the steel belt from the
    belt hook 2 of the carriage.

(7) Remove three screws (Fig.505, S1) to remove the spring guides A and
    B (Fig.505, Nos.24 & 25) which fix two guide shafts (Table 505, No.23b).

(8) Remove the head carriage Ass'y with the guide shafts (see Fig.438).

Belt hook 2 ─┐   ┌─ Locking paint 4
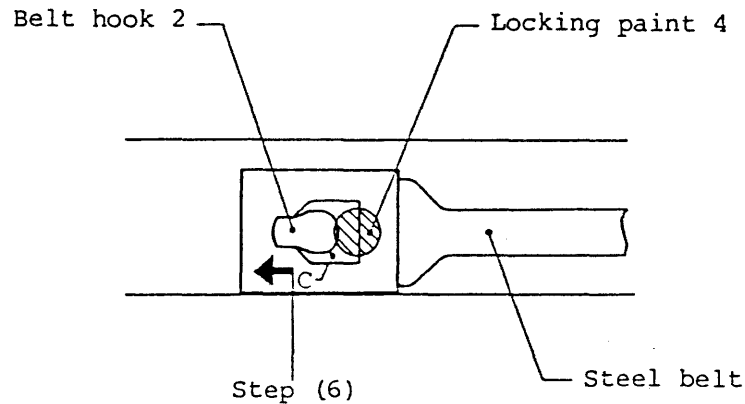
Step (6)   └─ Steel belt

(Fig.437) Belt hook area on the top side of the V-type carriage

(9) Remove the screw (Fig.505, S1) on the capstan of the stepping motor
    Ass'y and remove the steel belt and the plate washer (Fig.505, No.26).

(10) Fix a new steel belt (accessory of V-type carriage) temporarily to the
     capstan with the plate washer and the screw in item (9) as they were.

    Notes: 1. Fundamentally, the steel belt and the belt spring should be
              replaced with the head carriage. However, if there is no
              inferior points for these belt and spring, they may be used
              after cleaning the surface carefully with alcohol and gauze.

           2. Steel belt and belt spring are different for V-type carriage
              and L-type carriage. When a carriage is replaced with another
              type, be sure to replace the steel belt and belt spring together.

           3. Pay attention not to damage the surface of the steel belt or
              the capstan.

(11) Install a new head carriage Ass'y with two guide shafts in the reverse
     order of items (3) through (8).

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When fixing the steel belt to the carriage, install the belt spring at the bottom side first, and hook the steel belt to the belt hook 1 (Fig.436).

Then place the FDD with the top side up. Pull the steel belt in the direction of arrow mark in Fig.437 using a pair of tweezers and hook it to the belt hook 2.

Note: 4. When replacing the head carriage Ass'y, replace the two guide shafts at the same time because of matching the respective hole diameter of the carriage with those of the guide shafts. Each guide shaft is to be designated in combination with corresponding hole of the head carriage Ass'y.
Guide shaft which goes through the hole of the carriage smoothly with a little clearance is considered to be the best.

(12) After finishing the installation of the carriage, loosen the screw which fixes the steel belt to the capstan temporarily.

(13) Confirm that the steel belt runs on the center of the belt spring in Fig.436.

(14) After moving the head carriage several times manually, tighten the fixing screw of the steel belt in item (12) carefully with the specified torque of 4.5Kg.cm. At this time, be careful that the belt is tensioned straightly. Pay attention not to damage the surface of the belt or the capstan.

Note: 5. Do not pinch the upper arm of the head carriage when move it manually. Pinch the rear side of the carriage.

(15) Move the head carriage to the middle of movable area and apply a drop of oil (FLOIL 946P) on three points of guide shafts' surface near the shaft holes of the carriage. This item shall be omitted, if the oil has been already applied.

Notes: 6. A small drop of oil shall be applied to each point. For example, dip the tip of a narrow object such as wire or a pair of tweezers with oil.

7. If the head carriage or the head piece is smeared with oil, wipe it out completely by such a cotton swab dipped with alcohol.

(16) Make the head carriage move manually several times to spread the oil to all over the moving area.

(17) Referring Figs.436 and 437, apply a drop of locking paint to four points between the steel belt and the carriage (locking paint 1 through 4).

(18) In the reverse order of items (1) and (2), install the set arm and the head cable. Refer to item 4-2-3 as to the head cable treatment.

(19) Adjust the set arm position according to item 4-4-1.

(20) Model with head load solenoid:
Check and adjust the arm lifter according to item 4-4-3.

CSS model:
Check the CSS Ass'y according to item 4-4-4.

(21) Make the head move continuously between the track 00 and the innermost track and confirm that the steel belt does not meander nor undulate. When the SKA is used, key in "C6" for this check and key in "F" for stop.

Note: 8. If the steel belt is replaced with a new one, continue the head seek operation in item (21) for 3 minutes, approx.

(22) Check the head touch according to item 4-4-8.

(23) Adjust the asymmetry according to item 4-4-9.

(24) Adjust the track alignment according to item 4-4-12.

(25) Adjust the track 00 sensor position according to item 4-4-13.

(26) Check the track 00 stopper according to item 4-4-14.

(27) Check or adjust the index burst timing according to item 4-4-15.

(28) Check the read level according to item 4-4-10.

(29) Check the resolution according to item 4-4-11.

(30) If is recommended to connect the FDD to the system for overall test.
     (Refer to items 4-2-5 (7) for window margin test).

Stepping motor capstan

Head carriage Ass'y

Guide shafts
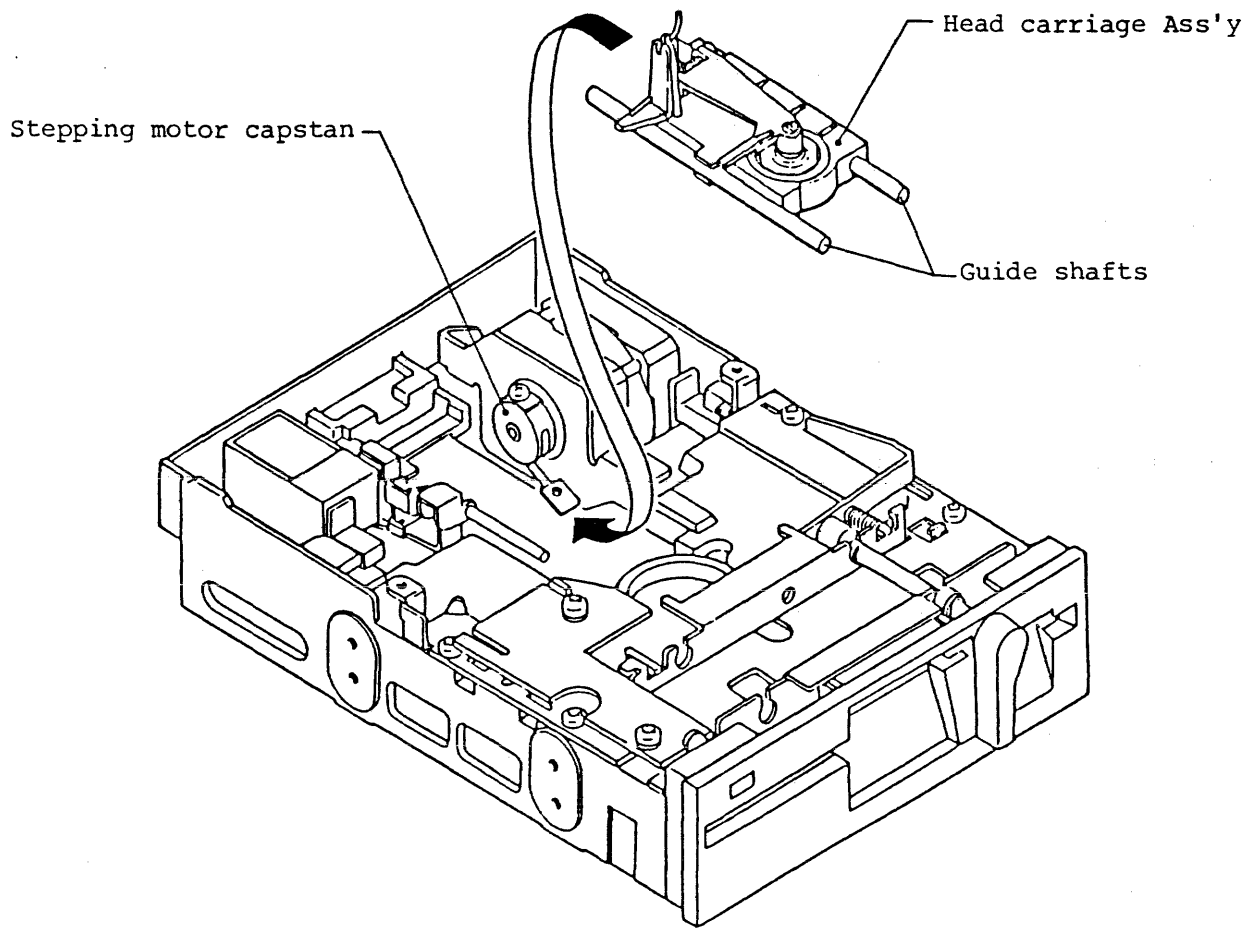
(Fig.438) Replacement of head carriage Ass'y

4-5-1-2. Replacement of L-type carriage

(A) Equipment

(1) Cross point screwdriver, M3

(2) Common screwdriver, small size

(3) A pair of tweezers

(4) Alcohol and gauze

(5) Oil (FLOIL 946P)

(6) SKA or user's system

(7) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect the head connector (J9) and remove the head cable from the cable guide (Fig.505, No.11).

(2) Remove the set arm sub Ass'y (Fig.505, No.3) by removing the two fixing screws (Fig.505, S8).

(3) Remove two fixing screws connecting the head carriage (Table 504, No.22a) and the steel belt A (Table 504, No.22c) and remove the steel belt and the belt spring (Table 504, No.22d) from the carriage.

(4) Remove three screws (Fig.505, S1) to remove the spring guides A and B (Fig.505, Nos.24 & 25) which fix two guide shafts (Fig.505, No.23d).

(5) Remove the head carriage Ass'y with the guide shafts (see Fig.438).

(6) Remove the screw (Fig.505, S1) on the capstan of the stepping motor Ass'y and remove the steel belt and the plate washer (Fig.505, No.26).

(7) Fix a new steel belt (accessory of L-type carriage) temporarily to the capstan with the plate washer and the screw in item (6) as they were.

Notes: 1. Fundamentally, the steel belt and the belt spring should be replaced with the head carriage. However, if there is no inferior points for these belt and spring, they may be used after cleaning the surface carefully with alcohol and gauze.

2. Steel belt and belt spring are different for V-type carriage and L-type carriage. When a carriage is replaced with another type, be sure to replace the steel belt and belt spring together.

3. Pay attention not to damage the surface of the steel belt or the capstan.

(8) Install a new head carriage Ass'y with two guide shafts in the reverse order of items (3) through (5). Two fixing screws of the steel belt to the head carriage (refer to item (3)) should be tightened with looseness for temporarily fixing.

Note: 4. When replacing the head carriage Ass'y, replace the two guide shafts at the same time because of matching the respective hole diameter of the carriage with those of the guide shafts. Each guide shaft is to be designated in combination with corresponding hole of the head carriage Ass'y.
Guide shaft which goes through the hole of the carriage smoothly with a little clearance is considered to be the best.

(9) After finishing the installation of the carriage, loosen the three screws which fix the steel belt to the capstan temporarily.

(10) Confirm that the steel belt runs on the center of the belt spring when viewed from the bottom side.

(11) After moving the head carriage several times manually, tighten the fixing screw of the steel belt in item (9) carefully with the specified torque of 4.5Kg.cm. At this time, be careful that the belt

is tensioned straightly. Pay attention not to damage the surface of
the belt or the capstan.

Note: 5. Do not pinch the upper arm of the head carriage when move it
         manually. Pinch the rear side of the carriage.

(12) Move the head carriage to the middle of movable area and apply a drop
     of oil (FLOIL 946P) on three points of guide shafts' surface near the
     shaft holes of the carriage. This item shall be omitted, of the oil
     has been already applied.

Notes: 6. A small drop of oil shall be applied to each point. For example,
          dip the tip of a narrow object such as wire or a pair of
          tweezers with oil.

       7. If the head carriage or the head piece is smeared with oil,
          wipe it out completely by such a cotton swab dipped with alcohol.

(13) Make the head carriage move manually several times to spread the oil
     to all over the moving area.

(14) In the reverse order of items (1) and (2), install the set arm and
     the head cable. Refer to item 4-2-3 as to the head cable treatment.

(15) Adjust the set arm position according to item 4-4-1.

(16) Model with head load solenoid: Check and adjust the arm lifter
     according to item 4-4-3.

     CSS model: Check the CSS Ass'y according to item 4-4-4.

(17) Make the head move continuously between the track 00 and the innermost
     track and confirm that the steel belt does not meander nor undulate.
     When the SKA is used, key in "C6" for this check and key in "F" for

stop.

If there is some abnormal running of the steel belt, readjust the belt with three screws in item (9). After the adjustment tighten the screws carefully with the specified torque of 4.5Kg.cm.

Note: 8. If the steel belt is replaced with a new one, execute the continuous seek operation in item (17) for three minutes, approx.

(18) Check the head touch according to item 4-4-8.

(19) Adjust the asymmetry according to item 4-4-9.

(20) Adjust the track alignment according to item 4-4-12.

(21) Loosen the fixing screw (Table 504, S10) of the track 00 stopper (Table 504, No.22e) to shift the stopper toward the rear side of the FDD.

(22) Adjust the track 00 sensor position according to item 4-4-13.

(23) Check the track 00 stopper according to item 4-4-14.

(24) Check or adjust the index burst timing according to item 4-4-15.

(25) Check the read level according to item 4-4-10.

(26) Check the resolution according to item 4-4-11.

(27) It is recommended to connect the FDD to the system for overall test. (Refer to item 4-2-5 (7) for window margin test).

4-5-2. Replacement of Stepping Motor Ass'y

(A) Tools

(1) Cross point screwdriver, M3

(2) A pair of tweezers

(3) Alcohol and gauze

(4) Locking paint

(5) SKA or user's system

(6) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect the stepping motor connector (J6).

(2) Remove the stepping motor cable form the cable hooks of the frame
    (Fig.505, No.1) to make the cable be free.

(3) Removal of steel belt and belt spring

    (a) V-type carriage (refer to Table 505):
        Remove the steel belt (Table 505, No.23c) and the belt spring (Table
        505, No.23d) according to item 4-5-1-1 (3) through (6).

    (b) L-type carriage (refer to Table 504):
        Remove two screws (Table 504, S4) fixing the head carriage (Table 504,
        No.22a) and the steel belt A (Table 504, No.22c), and remove the steel
        belt and the belt spring (Table 504, No.22d) from the carriage.

(4) Remove the two fixing screws (Fig.505, S9) of the stepping motor Ass'y
    (Fig.505, No.27) and remove the stepping motor with the steel belt.

(5) Remove screw (Fig.505, S1) on the capstan of the stepping motor and
    remove the steel belt and the plate washer (Fig.505, No.26).

(6) Confirm that there is no inferior nor defective point for the steel
belt and belt spring. Then carefully clean the surface of the steel
belt, belt spring and capstan with alcohol and gauze.
If an inferior or defective point is found, replace the steel belt or
the belt spring with a new one.

Note: 1. Steel belt and belt spring are different for V-type carriage
and L-type carriage. Designate the appropriate parts number
for the mounted carriage referring to Table 510-6 (or Tables
504, 505).

(7) Fix the steel belt temporarily to the capstan of a new stepping motor
with the plate washer and the screw as they were.

Note: 2. Never remove the plate of the stepping motor Ass'y since they
are combined each other.

(8) Install the stepping motor in item (7) according to the reverse order
of items (1) through (4).

Note: 3. For a V-type carriage, install the belt spring at the bottom side
first and hook the steel belt to the belt hook 1 (see Fig.436).
Then place the FDD with the top side up. Pull the belt in the
direction of arrow mark in Fig.437 using a pair of tweezers and
hook it to the belt hook 2.

For a L-type carriage, be careful to tension the steel belt
straightly and tighten the two screws temporarily.

(9) Loosen the screw which fixes the steel belt to the capstan.
If the L-type carriage is mounted, loosen another two screws which fix
the steel belt to the carriage.

(10) Confirm that the steel belt runs on the center of the belt spring when

viewed from the bottom side.

(11) After moving the head carriage several times manually, tighten the fixing screw of the steel belt in item (9) carefully with the specified torque of 4.5Kg.cm. At this time, be careful so that the belt is tensioned straightly. Pay attention not to damage the surface of the belt or the capstan.

Note: 4. Do not pinch the upper arm of the head carriage when move it manually. Pinch the rear side of the carriage.

(12) Make the head move continuously between the track 00 and the innermost track and confirm that the steel belt does not meander nor undulate. When the SKA is used, key in "C6" for this check and key in "F" for stop. If there is some abnormal running of the steel belt, readjust the belt with screws in item (9). After the adjustment tighten the screws carefully with the specified torque of 4.5Kg.cm.

Note: 5. If the steel belt is replaced, execute the continuous seek operation in item (12) for three minutes, approx.

(13) Adjust the track alignment according to item 4-4-12.

(14) This item is applied only for the L-type carriage:
Loosen the fixing screw (Table 504, S10) of the track 00 stopper (Table 504, No.22e) to shift the stopper toward the rear side of the FDD.

(15) Adjust the track 00 sensor position according to item 4-4-13.

(16) Check the track 00 stopper according to item 4-4-14.

4-5-3. Replacement of DD motor Ass'y (Spindle Motor)

(A) Tools

 (1) Cross point screwdriver, M3

 (2) Common screwdriver, small size

 (3) A pair of tweezers

 (4) Locking paint

 (5) SKA or user's system

 (6) Required equipment for each referring item

(B) Replacement procedure

 (1) Disconnect the spindle motor connector (J7).

 (2) Remove three screws (Fig.505, S5) of the DD motor Ass'y from the upper
     side of the FDD and draw out the DD motor Ass'y from the rotor side
     (PCBA side).

 (3) Install a new DD motor Ass'y in the reverse order.

 Note: The spindle area of the DD motor (clamping cup of the disk) is
        precisely machined. For installing the motor to the frame,
        place the spindle in parallel to the frame and push into the frame
        slowly. Handle the spindle very carefully not to damage the spindle
        surface.

 (4) Arrange the DD motor cable according to Fig.439.
     If the cable hook of the frame is the left type in Fig.439 (hook A),
     cable shall be formed so that it is threaded outside of the hook A.
     Do not thread the cable through the hook which might cause cable be
     in contact with the disk.
     If the cable hook is the right type in Fig.439 (hook B), thread the
     cable through the hook B normally.

(5) Adjust the set arm position according to item 4-4-1.

(6) Check the file protect sensor according to item 4-4-5.

(7) Check the disk rotational speed according to item 4-4-6.

(8) Adjust the track alignment according to item 4-4-12.

(9) Check or adjust the track 00 sensor position according to item 4-4-13.

(10) Check the track 00 stopper according to item 4-4-14.

(11) Check or adjust the index burst timing according to item 4-4-15.

Hook A

Hook B
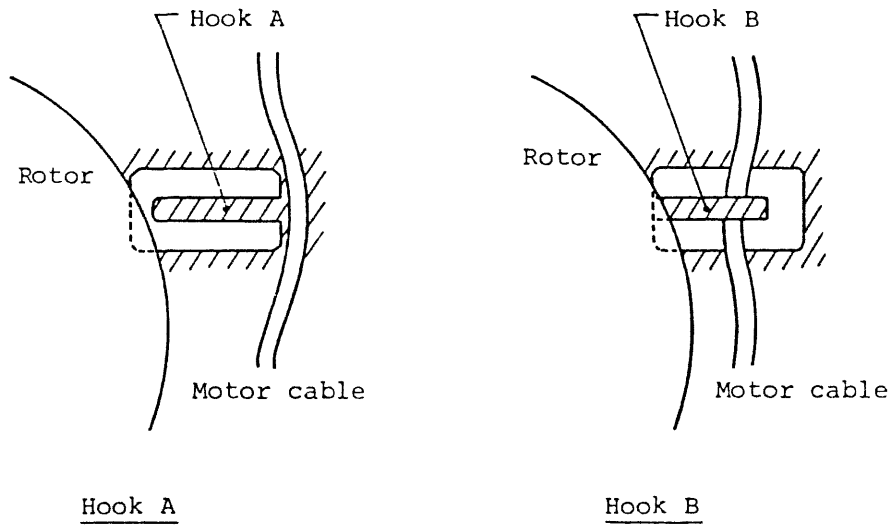
(Fig.439) Arrangement of spindle motor cable

4-5-4. Replacement of Collet Ass'y

(A) Equipment

(1) Cross point screwdriver, M3

(2) A pair of tweezers

(3) Round nose pliers

(4) Locking paint

(5) SKA or user's system

(6) Required equipment for each referring item

(B) Replacement procedure

(1) Remove the set arm (Fig.505, No.3) by removing the two fixing screws
    (Fig.505, S8).

(2) Remove the E-ring (Fig.505, S12) which fixes the collet Ass'y (Fig.505,
    No.9) to the set arm and remove the collet and the pressure spring
    (Fig.505, No.10).

(3) Install a new collet Ass'y in the reverse order. Pay attention to the
    orientation of the spring. The spring is conical. The smaller
    diameter side faces the collet side and the larger diameter side faces
    the set arm side.

(4) Adjust the set arm position according to item 4-4-1.

(5) Check (or adjust) the track alignment according to item 4-4-12.

4-5-5. Replacement of Head Load Solenoid

   This item applies only for the FDD with the head load solenoid.

(A) Tools

   (1) Cross point screwdriver, M3

   (2) Hexagon wrench key, 1.5mm

   (3) A pair of tweezers

   (4) Locking paint

   (5) SKA or user's system

   (6) Required equipment to each referring item

(B) Replacement procedure

   (1) Disconnect the head load solenoid and the track 00 connector (J4).

   (2) Pull out two solenoid pins (terminal Nos. 1 and 2) from the connector
       housing referring to item 4-2-2, (4).

   (3) Remove two fixing screws (Fig.505, S2) to remove the head load solenoid
       Ass'y (Fig.505, No.20).

   (4) Install a new head load solenoid Ass'y in the reverse order.

   Note: Arrange the wiring connection of the head load solenoid so that the
         white lead wire is connected to pin 1 and the red wire to pin 2.
         Refer to Fig.440.

   (5) Position the head load solenoid Ass'y so that the rod of ϕ2mm be in
       parallel with the set arm. Refer to Fig.441.
       The space between the head protector Ass'y and the arm lifter shall be
       more than 0.2mm. Then tighten the screws with the specified torque.

(6) Check and adjust the arm lifter according to item 4-4-3.

Yellow(pin 4)   Black(pin 6)

Solenoid lead wire   Grey(pin 5)
    Red(pin 2)

                                    Polarizing key position
                                              (pin 3)

Solenoid lead wire
    White(pin 1)

(Fig.440) Color identification of connector J4 wiring

Arm lifter

φ2mm,rod

                                        Head load solenoid Ass'y

                                        Head protector Ass'y

Set arm

0.2mm Min.
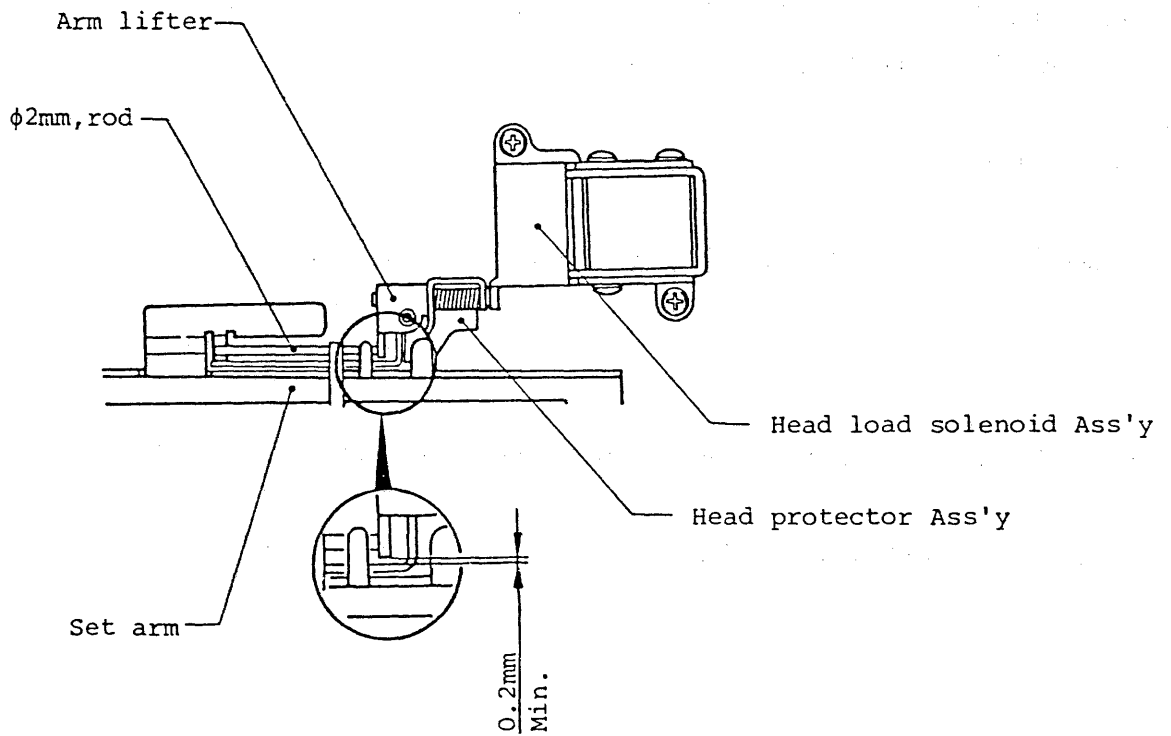
(Fig.441) Installation of the head load solenoid Ass'y

4-5-6. Replacement of PCBA Track 00 Sensor #H

(A) Tools

   (1) Cross point screwdriver, M3

   (2) A pair of tweezers

   (3) Locking paint

   (4) SKA or user's system
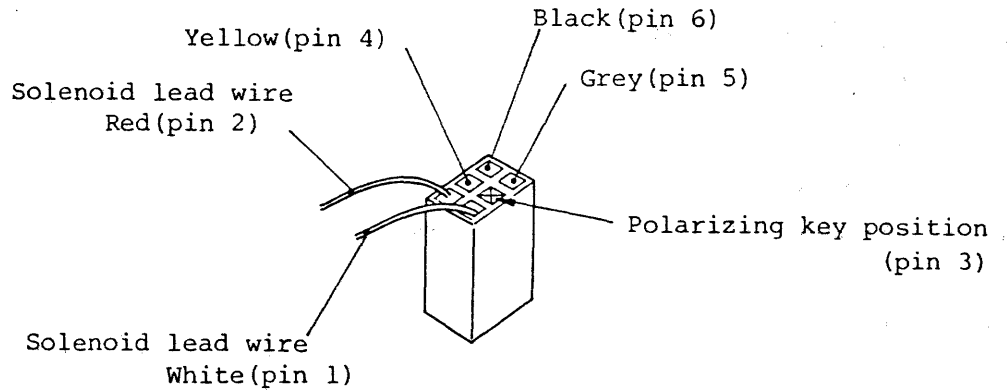
   (5) Required equipment for each referring item

(B) Replacement procedure

   (1) Disconnect the head load solenoid and the Track 00 connector (J4).

   (2) Pull out two solenoid pins (terminal Nos.1 and 2) from the connector
       housing referring to item 4-2-2, (4).

   (3) Remove the fixing screw (Fig.505, S6) to remove the PCBA T00 sensor #H
       (Fig.505, No.19).

   (4) Install a new PCBA T00 sensor in the reverse order.

   Note: Araange the wiring connection of the head load solenoid so that the
         white lead wire is connected to pin 1 and red wire to pin 2. (See
         Fig.440).

   (5) Adjust the track 00 sensor position according to item 4-4-12.

   (6) Check the track 00 stopper according to item 4-4-13.

4-5-7. Replacement of PCBA MFD Control #H

(A) Tools

(1) Cross point screwdriver, M3

(2) Common screwdriver, small size

(3) SKA or user's system

(4) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect all of the connectors connected to the PCBA MFD control #H
(Fig.505, No.29) referring to item 4-2-2.

(2) Remove the PCBA by removing the three fixing screws (Fig.505, S3).

(3) Install a new PCBA in the reverse order.

(4) Set the straps and terminator as they were on the old PCBA.

(5) Check the file protect sensor according to item 4-4-5.

(6) Check the erase gate delay according to item 4-4-7.

(7) Adjust the asymmetry according to item 4-4-9.

(8) Check the read level according to item 4-4-10.

(9) Check the resolution according to item 4-4-11.

(10) Check the track 00 sensor according to item 4-4-13.

(11) Check the index burst timing according to item 4-4-15.

(12) It is recommended to connect the FDD to the system for overall test. (Refer to items 4-2-5 (7) for window margin test).

4-5-8. Replacement of PCBA Front OPT #H

(A) Tools

(1) Cross point screwdriver, M3

(2) SKA or user's system

(3) Required equipment for each referring item

(B) Replacement procedure

(1) Disconnect PCBA front OPT #H connector (J5).

(2) Remove the two fixing screws (Fig.505, S7) to remove the PCBA.

(3) Install a new PCBA in the reverse order.

(4) Check the file protect sensor according to item 4-4-5.

(5) Adjust the index burst timing according to item 4-4-15.

(6) Check the performance of the front bezel indicator.

4-5-9. Replacement of Front Bezel Ass'y

(A) Tools

(1) Cross point screwdriver, M3

(2) Required equipment for each referring item

(B) Replacement procedure

(1) Draw out the front lever Ass'y (Fig.505, No.32).

(2) Remove the fixing screws (Fig.505, S8) of the front bezel Ass'y (Fig.505,
No.31) and draw the front bezel out.

(3) Install a new front bezel Ass'y in the reverse order. For the
installation of the front bezel, press the longitudinal ends of the
bezel against the frame and tighten the fixing screws with the
specified torque.

(4) Insert the front lever Ass'y fully against the lever shaft as it was.

4-5-10. Replacement of Front Lever Ass'y

(A) Tools

(1) Required equipment for each referring item

(B) Replacement procedure

(1) Draw out the front lever Ass'y (Fig.505, No.32).

(2) Insert a new front lever Ass'y fully against the lever shaft as it was.

(3) Check (or adjust) the holder position according to item 4-4-2.

4-5-11. Replacement of CSS Ass'y

This item applies only to the CSS model (without head load solenoid).

(A) Tools

(1) Cross point screwdriver, M3
(2) Required equipment for each referring item

(B) Replacement procedure

(1) Remove the fixing screw (Fig.505, S2) to remove the CSS Ass'y (Fig.505, No.21) from the frame.

(2) Install a new CSS Ass'y in the reverse order. Be careful to install the arm lifter area (ϕ2mm rod) to be in parallel to the set arm. The CSS Ass'y shall be fixed with no contact to the set arm. (Refer to Fig.442).

(3) Check the CSS Ass'y according to item 4-4-4.
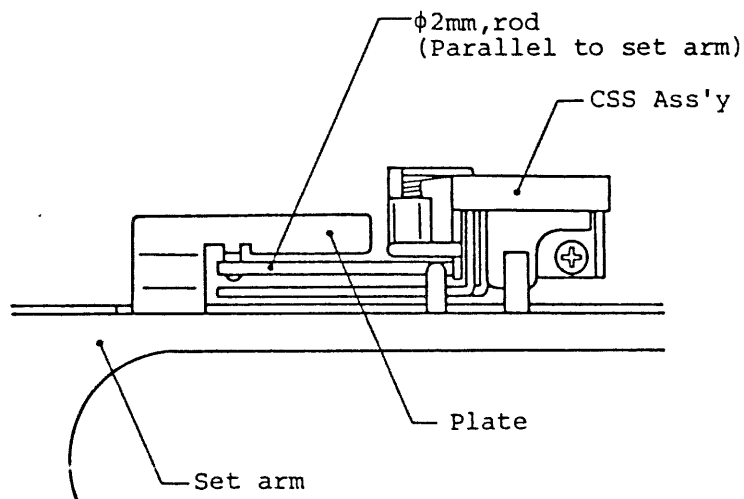
(Fig.442) CSS Ass'y and shift lever position

4-5-12. Replacement of Head Pad (single sided)

This item applies only to the single sided FDD.

(A) Equipment

(1) A pair of tweezers
(2) Required equipment for each referring item

(B) Replacement procedure

(1) Lift up the pad arm manually and peel the pad carefully with a pair
of tweezers. (See Fig.443).

(2) Apply a new pad to the original position. Do not press the pad
surface strongly.

(3) Check or clean the magnetic head surface according to item 4-3-2.

(4) Adjust the head pad position according to item 4-4-8.

(5) Check the read level according to item 4-4-10.

(6) Check the resolution according to item 4-4-11.
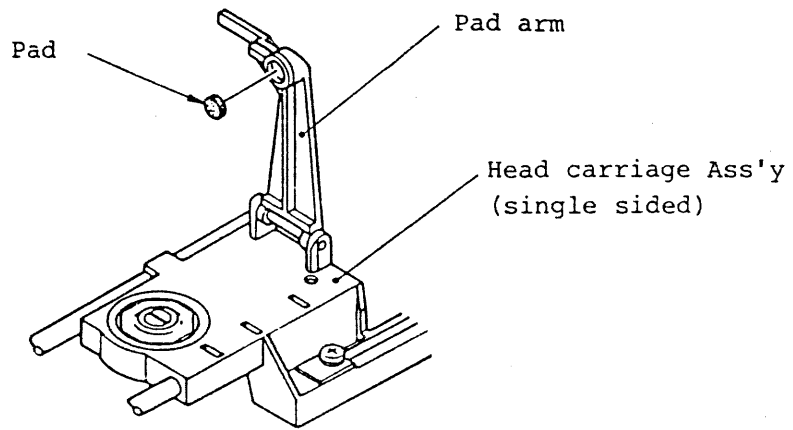
(Fig.443) Replacement of head pad

J1

X X RESERVED	2
IN USE/HEAD LOAD	4
DRIVE SELECT 3	6
INDEX/SECTOR	8
DRIVE SELECT 0	10
DRIVE SELECT 1	12
DRIVE SELECT 2	14
MOTOR ON	16
DIRECTION SELECT	18
STEP	20
WRITE DATA	22
WRITE GATE	24
TRACK 00	26
WRITE PROTECT	28
READ DATA	30
SIDE ONE SELECT	32
X X READY	34
SIGNAL GND	1
(ODD NOS.)	⁄
	33

PCBA
MFD CONTROL
15532060-XX

J2

+12V	1
0V	2
0V	3
+ 5V	4

FRAME GROUND
(FASTON TAB)

FRAME

J9

12	R/W START
2	R/W FINISH
10	COMMON
	ERASE
6	SHIELD
4	
11	R/W START
1	R/W FINISH
9	COMMON
	ERASE
7	SHIELD
3	

HEAD CARRIAGE ASS'Y
SIDE 0
HEAD

X SIDE 1
HEAD

J5

1	5V	
3	INDEX SENSOR	1
5	FRONT LED	2
	FPT SENSOR	3
	0V	4
		5

PCBA FRONT OPT
15532064-XX

XJ10
1
2

X1/1 FRONT
BEZEL ASS'Y

XJ11
1
2

X DOOR LOCK
SOLENOID
ASS'Y

J4

1	DRV
2	PWR
4	PWR
5	SEN
6	0V

X HEAD LOAD SOLENOID ASS'Y

PCBA TRACK 00
SENSOR
15532063-00

J6

1	PHASE A
2	PHASE B
3	PHASE NA
4	PHASE NB
5	COM A
6	COM B

STEPPING
MOTOR
ASS'Y

J7

1	12V
2	0V
3	MC
4	5V
5	X X HPSD

PCBA
DD MOTOR
SERVO

DD MOTOR ASS'Y
⟷ (M)

XJ8

1	5V
2	0V
3	SEN

150Ω1/4W

X PCBA DISK SENSOR
15532002-00

X DOOR CLOSE SW
ASS'Y

NOTES
2. SIGNALS WITH DOUBLE ASTERISKS(X X) ARE CHANGED IN SOME FDD VERSIONS. REFER TO VERSION TABLE. UNLISTED SIGNALS ARE NOT USED IN THAT VERSIONS.
1. PARTS WITH AN ASTERISK(X) ARE USED IN SOME FDD VERSIONS. REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

P/N 19307200-XX

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FD-55V

TOTAL DIAGRAM

B 61509 85·10·17

協井 85·6·7
小林 85·6·7
上原 85·2·27
菊池 85·6·7

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VERSIONS TABLE

FDD VERSIONS	MAIN SPEC	X PARTS	XX SIGNALS	PCBA VERSIONS MFD CONTROL	PCBA VERSIONS FRONT OPT
A -00	S. SIDE CSS		J1-34:READY	-00 OR -01	-00
B -01	D. SIDE CSS	S1 HEAD	J1-34:READY	-01	-00
E -02	S. SIDE CSS		J1-34:READY	-02 OR -03	-00
F -03	D. SIDE CSS	S1 HEAD	J1-34:READY	-03	-00
G -04	D. SIDE CSS	S1 HEAD	J1-34:READY	-04	-00
GF-05	D. SIDE CSS	S1 HEAD / D. SEN	J1- 2:HIGH/NORMAL DENSITY / J1-34:READY/DISK CHANGE / J7- 5:HSPD	-05	-00
B -06	D. SIDE CSS XT	S1 HEAD	J1-34:READY/OPEN	-08	-00
GF-07	D. SIDE CSS (AT)	S1 HEAD / D. SEN	J1- 2:HIGH/NORMAL DENSITY / J1-34:READY/DISK CHANGE / J7- 5:HSPD	-09	-00
A -08	S. SIDE CSS M ONLY				-00
B -09	D. SIDE CSS M ONLY	S1 HEAD			-00
A -10	S. SIDE HL	HL ASS'Y	J1-34:READY	-00 OR -01	-00
B -11	D. SIDE HL	HL ASS'Y / S1 HEAD	J1-34:READY	-01	-00
E -12	S. SIDE HL	HL ASS'Y	J1-34:READY	-02 OR -03	-00
F -13	D. SIDE HL	HL ASS'Y / S1 HEAD	J1-34:READY	-03	-00
G -14	D. SIDE HL	HL ASS'Y / S1 HEAD	J1-34:READY	-04	-00
GF-15	D. SIDE HL	HL ASS'Y / S1 HEAD / D. SEN	J1- 2:HIGH/NORMAL DENSITY / J1-34:READY/DISK CHANGE / J7- 5:HSPD	-05	-00
B -16	D. SIDE HL AT	HL ASS'Y / S1 HEAD	J1-34:READY/OPEN	-14	-00
GF-17	D. SIDE HL AT	HL ASS'Y / S1 HEAD / D. SEN	J1- 2:HIGH/NORMAL DENSITY / J1-34:READY/DISK CHANGE / J7- 5:HSPD	-09	-00
B -21	D. SIDE CSS T1K	S1 HEAD	J1-34:READY	-06	-00

FDD VERSIONS	MAIN SPEC	X PARTS	XX SIGNALS	PCBA VERSIONS MFD CONTROL	PCBA VERSIONS FRONT OPT
B -22	D. SIDE CSS T1K GREEN	S1 HEAD	J1-34:READY	-06	-01
B -23	D. SIDE CSS T1KD	S1 HEAD	J1-34:READY	-07	-00
B -24	D. SIDE CSS T1K GREEN	S1 HEAD	J1-34:READY	-07	-01
GF-25	D. SIDE HL AT GREEN	HL ASS'Y / S1 HEAD / D. SEN	J1- 2:HIGH/NORMAL DENSITY / J1-34:READY/DISK CHANGE / J7- 5:HSPD	-09	-01
F -30	D. SIDE CSS (XT)	S1 HEAD	J1-34:READY/OPEN	-10	-00
B -31	D. SIDE CSS GCR/XT	S1 HEAD	J1-34:READY/OPEN	-11	-00
F -32	D. SIDE CSS DC-00 Q EJ	DC SW ASS'Y-00 / S1 HEAD	J1-34:DOOR CLOSE	-12	-00
G -33	D. SIDE HL RE DL	HL ASS'Y / S1 HEAD / DL SOL	J1-34:READY	-13	-02
B -36	D. SIDE CSS (AT/XT)	S1 HEAD	J1-34:READY/OPEN	-15	-00

NOTE :   ABBREVIATED NAMES ARE AS FOLLOWS :
S SIDE : SINGLE SIDED   D SIDE : DOUBLE SIDED
HL : HEAD LOAD SOLENOID   DL SOL : DOOR LOCK SOLENOID
CSS : WITHOUT HL SOL   1/1 FB : 1/1 FRONT BEZEL (FULL HIGHT)
S1 HEAD : SIDE 1 HEAD   D. SEN : PCBA DISK SENSOR
DC SW : DOOR CLOSE SWITCH

P/N 19307200-XX

TEAC ティアック株式会社

FD-55V

TOTAL DIAGRAM

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FDD VERSIONS	MAIN SPEC	X PARTS	XX SIGNALS	PCBA VERSIONS	
				MFD CONTROL	FRONT OPT

FDD VERSIONS	MAIN SPEC	X PARTS	XX SIGNALS	PCBA VERSIONS	
				MFD CONTROL	FRONT OPT

VERSIONS TABLE

P/N 19307200-XX

TEAC ティアック株式会社

形式 FD-55V

品名 TOTAL DIAGRAM

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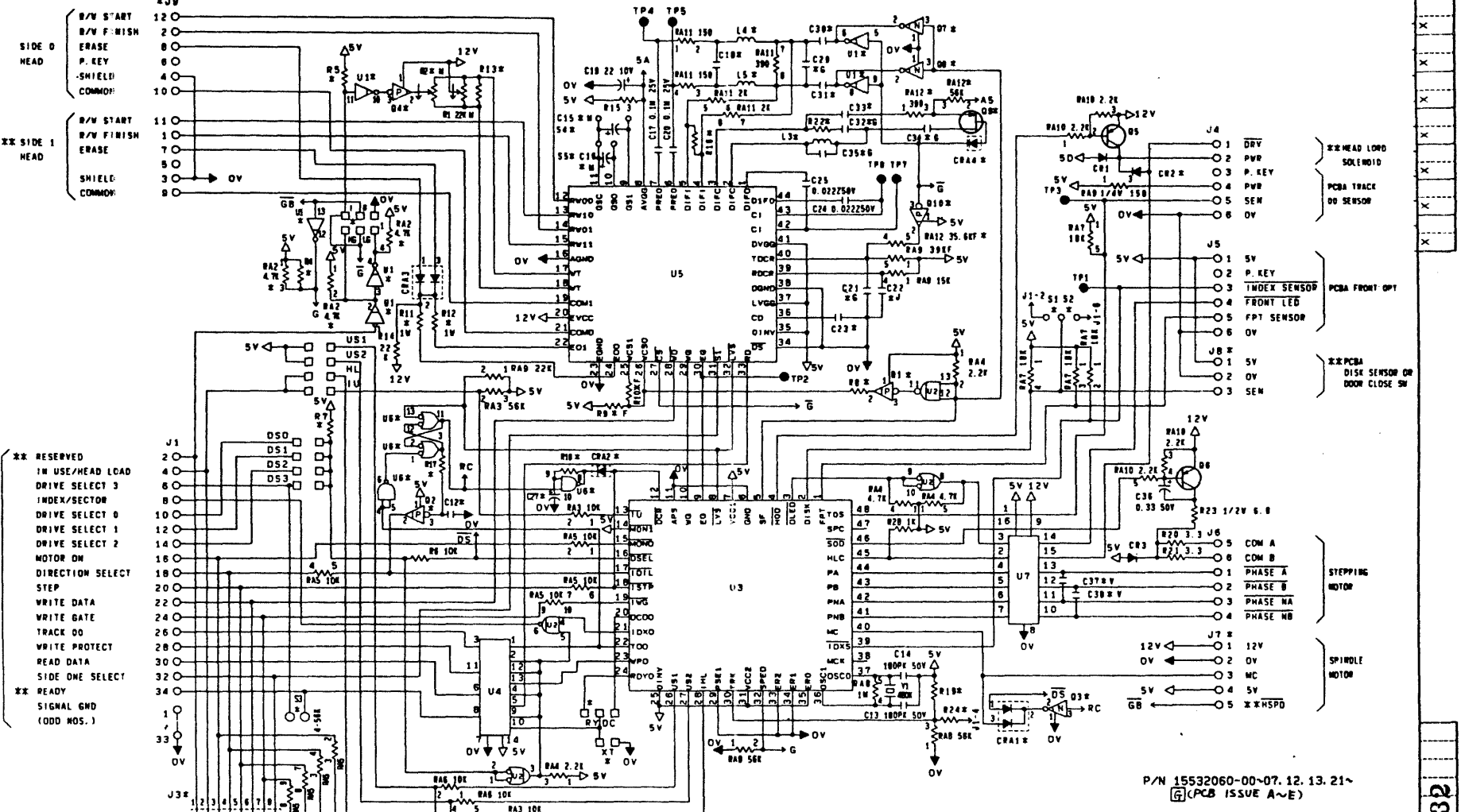
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Ⓖ(PCB ISSUE A~E)

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FD-55V

PCBA MFD CONTROL #H

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P/N 15532060-08~11.14~20
[G](PCB ISSUE A~E)

TEAC ティアック株式会社

FD-55V

PCBA MFD CONTROL #H

SCHEMATIC

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D-203A

DC POWER — schematic diagram (J2: +12V 1, 0V 2, 0V 3, +5V 4; L1 39μHK, L2 39μHK; C1 10 25V, C2 22 25V, C9.C28 0.022Z50V, C5 100 10V, C7 22 10V, C4.C6.C10.C26 0.022Z50V; outputs 12V, 0V, 5V, 05V; FASTON FRAME GROUND, FG, TP6)

VERSION TABLE

PCBA VERSIONS	MAIN SPEC.	¤ PARTS
-00	48 tPI S.SIDE A-STD	J9(56P). THE OTHERS ARE THE SAME AS - 01.
-01	48 tPI S.SIDE A-STD	RA1(7-330). R5(4.7K). R7(330). R9(2.67K). R11(120). R13(2.2K). R16(8.2K). R22(200). C18(2200P). C21(100P). C22(100P). C23(180P). C29(2200P). C32(1500P). C37(6.8.25V).
	48 tPI D.SIDE B-STD	C38(6.8.25V). J3(14P). J7(4P). J9(W12P). RY. S5. L3(330μH). L4(330μH). L5(330μH).
-02	96 tPI S.SIDE E-STD	J9(56P). THE OTHERS ARE THE SAME AS - 03.
-03	96 tPI S.SIDE E-STD	Q1. RA1(7-330). R5(4.7K). R7(330). R8(20K). R9(4.02K). R11(240). R13(4.7K). R19(10). R22(237). C18(2200P). C21(100P). C22(100P). C23(180P). C29(2200P). C32(1500P).
	96 tPI D.SIDE F-STD	C37(4.7.25V). C38(4.7.25V). J3(14P). J7(4P). J9(W12P). RY. S5. L3(330μH). L4(330μH). L5(330μH)
-04	96 tPI D.SIDE G-STD	Q1. Q7. Q8. RA1(7-330). R4(4.7K). R5(4.7K). R7(330). R8(12K). R9(1.78K). R11(130). R13(3.3K). R19(10). R22(464). C18(1000P). C21(27P). C22(27P). C23(100P). C29(1000P). C30(0.0022.25V). C31(0.0022.25V). C32(560P). C35(100P). C37(4.7.25V). C38(4.7.25V). J3(14P). J7(4P). J9(W12P). RY. S4. L3(180μH). L4(150μH). L5(150μH)
-05	96 tPI D.SIDE GF-STD	U1. Q1. Q4. Q7. Q8. Q9. Q10(PNP). CRA4. RA1(8-330). RA2. RA12(T-7615-01). R2(22K). R7(330). R8(12K). R9(2.74K). R10(4.42K). R11(240). R12(130). R13(3.9K). R16(10K). R19(10). R22(432). C18(1000P). C21(75P). C22(27P). C23(100P). C29(1000P). C30(0.0022.25V). C31(0.0022.25V). C32(680P). C33(0.022.25V). C34(1500P). C35(100P). C37(4.7.25V). C38(4.7.25V). J3(16P). J7(5P). J8(3P). J9(W12P). HG/LG/I/8(W6P). DC/RY(S3P). L3(180μH). L4(150μH). L5(150μH). S4

6. SIGNALS WITH DOUBLE ASTERISKS(¤¤) ARE USED OR CHANGED IN SOME FDD VERSIONS.
REFER TO FD-55V TOTAL DIAGRAM AND IT'S VERSION TABLE.

5. POLARIZING KEY POSITIONS FOR CONNECTOR(J) ARE:
J1: BETWEEN PIN4 AND PIN5. J4: PIN3. J5: PIN2. J9: PIN6

4. TOLERANCE SYMBOLS FOR R.RA.C AND L ARE:
F:±1%. G:±2%. J:±5%. K:±10%. M:±20%. V:+20~-10%. Z:+80~-20%

3. CAPACITOR(C) VALUES ARE IN MICRO FARADS. 10V OR HIGHER. ±10%(K). UNLESS OTHERWISE SPECIFIDE.

2. RESISTOR(R) AND RESISTOR ARRAY(RA) VALUES ARE IN OHMS. 1/8V OR GREATER. ±5%(J). UNLESS OTHERWISE SPECIFIED.

NOTES: 1. PARTS WITH AN ASTERISK(¤) ARE DIFFERENT IN EACH PCBA VERSION.
REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

P/N 15532060-XX
G (PCB ISSUE A~E)

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FD-55V
PCBA MFD CONTROL #H
SCHEMATIC

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PCBA VERSIONS	MAIN SPEC.	X PARTS
-06	48tPI D. SIDE B	RA1(7-1K), R7(1K). THE OTHERS ARE THE SAME AS - 01.
-07	48tPI D. SIDE B	RA1(8-1K), R7(1K), DELETE J3 THE OTHERS ARE THE SAME AS - 01.
-08 REV. A	48tPI D. SIDE B	CR4 WITH JUMPER. RY(S2P), XT(S2P) PATTERN:P2, P4, P9, P10 OPEN:P1, P3, P5, P6 ~ P8 THE OTHERS ARE THE SAME AS - 01.
-08 REV. B	48tPI D. SIDE B	Q10(NPN), S17, RY(S2P), XT(S2P), DELETE R11, R12(120) PATTERN:P9, P10 JUMPER:P1, P3, P5 CUT:P2, P4 OPEN:P6 ~ P8 THE OTHERS ARE THE SAME AS - 01.
-08 REV. C	48tPI D. SIDE B	Q10(NPN), S17, RY(S2P), XT(S2P), DELETE R11, R12(120) PATTERN:P1, P5, P9, P10 JUMPER:P3 OPEN:P2, P4, P6 ~ P8 (PCB ISSUE E IS USED.) THE OTHERS ARE THE SAME AS - 01.
-09	96tPI D. SIDE GF	U6(74LS08), Q10(PNP), CR4(DIP SIDE) PATTERN:P2, P4 JUMPER:P6 ~ P8 CUT:P9, P10 OPEN:P1, P3, P5 THE OTHERS ARE THE SAME AS - 05.
-10	96tPI D. SIDE F	Q10(NPN), S17, RY(S2P), XT(S2P), DELETE R11, R12(240) PATTERN:P1, P5, P9, P10 JUMPER:P3 OPEN:P2, P4, P6 ~ P8 (PCB ISSUE E IS USED.) THE OTHERS ARE THE SAME AS - 03.
-11 REV A	48tPI D. SIDE B	R16(18K), R22(453) THE OTHERS ARE THE SAME AS - 08. REV. A.
-11 REV. B	48tPI D. SIDE B	R16(18K), R22(453) (PCB ISSUE E IS USED.) THE OTHERS ARE THE SAME AS - 08. REV. C.
-12	96tPI D. SIDE F	DELETE RY. JUMPER(J8-3 ~ U4-10) THE OTHERS ARE THE SAME AS - 03.
-13	96tPI D. SIDE G	U6(74LS132), Q2, Q3, CRA1, CRA2, R17(100), R18(680), C12(0.022Z, 50V), C27(4.7, 50V) THE OTHERS ARE THE SAME AS - 04.
-14	48tPI D. SIDE B	U6(74LS08), CR4(DIP SIDE), RY(S2P), XT(S2P). PATTERN:P2, P4 JUMPER:P6 ~ P8 CUT:P9, P10 OPEN:P1, P3, P5 THE OTHERS ARE THE SAME AS - 01.
-15 REV. A	48tPI D. SIDE B	U6(74LS08), Q10(NPN), S17, RY(S2P), XT(S2P), DELETE R11, R12(120) JUMPER:P1, P3, P5 ~ P8 CUT:P2, P4, P9, P10 THE OTHERS ARE THE SAME AS - 01
-15 REV. B	48tPI D. SIDE B	U6(74LS08), Q10(NPN), S17, RY(S2P), XT(S2P), DELETE R11, R12(120) PATTERN:P1, P5 JUMPER:P3, P6 ~ P8 CUT:P9, P10 OPEN:P2, P4 (PCB ISSUE E IS USED.) THE OTHERS ARE THE SAME AS - 01

VERSION TABLE   P/N 15532060-XX
G(PCB ISSUE A~E)

TEAC ティアック株式会社

FD-55V

PCBA MFD CONTROL #H

SCHEMATIC

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P/N 15532060-XX
(PCB ISSUE F ~)

TEAC ティアック株式会社

FD-55V

PCBA MFD CONTROL #H

SCHEMATIC

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DC POWER

J2
+12V 1
0V 2
0V 3
+5V 4

L1 39μHK
L2 39μHK

C1 10 25V
C5 100 10V
C2 22 26V
C7 22 10V
C9.C28 0.022 250V
C4.C6.C10.C28 0.022 250V

12V
0V
5V
D5V

FASTON
FRAME GROUND

F8
S2P
R3 100K *
C3 0.01Z 500V *

TP6

VERSION TABLE

PCBA VERSIONS	MAIN SPEC.	* PARTS
-01 / REV. D	48 tPI S.SIDE A-STD / 48 tPI D.SIDE B-STD	Q5, CR1, CRA1, CRA2, RA1(7-330), RA9(T-7613, 1-4:15K), RA13, R5, R7(330), R9(2.67K), R11(120), R13(2.2K), R16(8.2K), R22(200), C18(2200P), C21(100P), C22(100P), C23(180P), C29(2200P), C32(1500P), C37(6.8,25V), C38(6.8,25V), L3(330μH), L4(330μH), L5(330μH), J3(14P), J5(56P), J7(4P), S4(JV25) STRAP POST PINS:DS0~DS3(V8P), U1~1U(V8P), RY(S2P), XT(S2P), ML/RE(S4P), E0(S2P), E2(S2P) SHORT BAR :E0
-03 / REV. D	96 tPI S.SIDE E-STD / 96 tPI D.SIDE F-STD	Q1, Q2, Q5, CRA1, CRA2, RA1(7-330), RA9(T-7613,1-4:15K), RA13, R5, R7(330), R8(20K), R9(4.02K), R11(240), R13(4.7K), R19A, R22(237), C18(2200P), C21(100P), C22(100P), C23(180P), C29(2200P), C32(1500P), C37(4.7,25V), C38(4.7,25V), L3(330μH), L4(330μH), L5(330μH), J3(14P), J5(56P), J7(4P), S4(JV25) STRAP POST PINS:DS0~DS3(V8P), U1~1U(V8P), RY(S2P), XT(S2P), ML/RE(S4P), E0(S2P), E2(S2P) SHORT BAR :E0
-04 / REV. D	96 tPI D.SIDE G-STD	Q1, Q2, Q5, Q7, Q8, CR1, CRA1, CRA2, RA1(7-330), RA9(T-7613,1-4:15K), RA13, R4, R5, R7(330), R8(12K), R9(1.78K), R11(130), R13(3.3K), R19A, R22(464), C18(1000P), C21(27P), C22(27P), C23(100P), C29(1000P), C30, C31, C32(560P), C35, C37(4.7,25V), C38(4.7,25V), L3(180μH), L4(150μH), L5(150μH), J3(14P), J5(56P), J7(4P), RY(JV25), S5(JV25) STRAP POST PINS:DS0~DS3(V8P), U1~1U(V8P), ML/RE(S4P), E0(S2P), E1(S2P) SHORT BAR :E0
-05 / REV. E	96 tPI D.SIDE GF-STD	U1, Q1, Q2, Q4, Q5, Q7, Q8, Q9, Q10, CR1, CRA1, CRA2, CRA4, RA1(8-330), RA2, RA9(T-7613,1-4:15K), RA12(T-7615-01), RA13, R2, R7(330), R8(12K), R9(2.74K), R10(4.42K), R11(240), R12(130), R13(3.9K), R16(10K), R19A, R22(432), C18(1000P), C21(75P), C22(27P), C23(100P), C29(1000P), C30, C31, C32(680P), C33, C34, C35, C37(4.7,25V), C38(4.7,25V), L3(180μH), L4(150μH), L5(150μH), J3(16P), J5(56P), J7(5P), J8(3P), S5(JV25), S12(JV25) STRAP POST PINS:DS0~DS3(V8P), U1~1U(V8P), HG/LG/1/H(V6P), RY/DC/RE/ML(S7P), E0(S2P), E2(S2P) SHORT BAR :E0

8. SIGNALS WITH DOUBLE ASTERISKS(**) ARE USED OR CHANGED IN SOME FDD VERSIONS. REFER TO FD-55V TOTAL DIAGRAM AND IT'S VERSION TABLE.

5. POLARIZING KEY POSITIONS FOR CONNECTOR(J) ARE:
J1: BETWEEN PIN4 AND PIN6, J4: PIN3, J5: PIN2, J8: PIN6

4. TOLERANCE SYMBOLS FOR R, RA, C AND L ARE:
F:±1%, G:±2%, J:±5%, K:±10%, M:±20%, V:+20~-10%, Z:+80~-20%

3. CAPACITOR(C) VALUES ARE IN MICRO FARADS. 10V OR HIGHER, ±10%(K), UNLESS OTHERWISE SPECIFIDE.

2. RESISTOR(R) AND RESISTOR ARRAY(RA) VALUES ARE IN OHMS, 1/8V OR GREATER, ±5%(J), UNLESS OTHERWISE SPECIFIED.

NOTES: 1. PARTS WITH AN ASTERISK(*) ARE DIFFERENT IN EACH PCBA VERSION. REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

P/N 15532060-XX (PCB ISSUE F~)

TEAC ティアック株式会社

形式	FD-55V
品名	PCBA MFD CONTROL 部H
図名	SCHEMATIC
図番	1041 0601

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PCBA VERSIONS	MAIN SPEC.	X PARTS
-00 REV. D	48tpi D. SIDE B	RA1(T-1K), R7(1K), RY(JV25), EO(JV20) DELETE:CRA1, CRA2, RA13, RY(S2P), XT(S2P), ML/RE(S4P), EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.
-07 REV. D	48tpi D. SIDE B	RA1(8-1K), R7(1K), RY(JV25), EO(JV20) DELETE:CRA1, CRA2, RA13, J3(14P), RY(S2P), XT(S2P), ML/RE(S4P), EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.
-00 REV. D	48tpi D. SIDE B	SHORT BAR:E2 DELETE:SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.
-00 REV. D	96tpi D. SIDE GF	U6(74LS74A, CUT PIN 10), B11, CR4, C39(1000P), S13(JV25), E1(JV20), E2(JV20) JUMPER:P4~RA13-2, P3~E1 CUT :P5 DELETE:EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 05.
-10 REV. D	96tpi D. SIDE F	SHORT BAR:E2 DELETE:SHORT BAR EO THE OTHERS ARE THE SAME AS - 03.
-11 REV. D	48tpi D. SIDE B	R16(18K), R22(453) SHORT BAR:E2 DELETE:05, CR1, SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.
-12 REV. D	96tpi D. SIDE F	J8(3P), EO(JV20) STRAP POST PINS:DC3(S2P) SHORT BAR :DC3 DELETE:05, CR1, CRA1, CRA2, RA13, XT(S2P), ML/RE(S4P), EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 03.
-14 REV. C -15 REV. D	48tpi D. SIDE B	SHORT BAR:E2 DELETE:SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.
-16 REV. A	96tpi D. SIDE GF	RA1(8-1K), R19B, R22(536), R20, J5(S7P), DSO(JV25), HG(JV25), I(JV25), RY(JV25), EO(JV20), S0(JV25), JUMPER:P2~S9 DELETE:CRA1, CRA2, RA13, R19A, J3(16P), J8(3P), DS0~DS3(V8P), U1~1U(V6P), HG/LG/1/E(V6P), RY/DC/RE/ML(STP), EO(S2P), E2(S2P), S12(JV25), SHORT BAR EO THE OTHERS ARE THE SAME AS - 05.
-18 REV. A	96tpi D. SIDE GF	RA1(8-1K), R7(1K), R19B, HG(JV25), I(JV25), RY(JV25), RE(JV20), EO(JV20) JUMPER:P2~S9 DELETE:05, CR1, CRA1, CRA2, RA13, R19A, J3(16P), J8(3P), U1~1U(V8P), HG/LG/1/E(V6P), RY/DC/RE/ML(STP), EO(S2P), E2(S2P), S12(JV25), SHORT BAR EO THE OTHERS ARE THE SAME AS - 05.
-19 REV. A	96tpi D. SIDE GF	RA1(8-1K), RA9(T-7613-01, 1-4:5.1K), R7(1K), C22(10P), LG(JV25), I(JV25), RY(JV25), S15(JV25), EO(JV20) DELETE:05, CR1, CRA1, CRA2, RA13, J3(16P), J8(3P), S12(JV25), HG/LG/1/E(V6P), RY/DC/RE/ML(STP), EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 05.
-20 REV. A	96tpi D. SIDE F	U6(74LS74A), J8(3P), EO(JV20), S11(JV25), S14(JV25), S16(JV25), STRAP POST PINS:DC1/DC2(S3P), DC3/DC4(S3P) SHOR BAR :DC2, DC4 DELETE:CRA1, CRA2, RA13, RE/ML(S4P), RY(S2P), XT(S2P), EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 03.
-21 REV. A	96tpi D. SIDE GF	U6(74LS74A), EO(JV20), S11(JV25), S14(JV25), S16(JV25), STRAP POST PINS:DC1/DC2(S3P), DC3/DC4(S3P) SHORT BAR :DC2, DC4 DELETE:CRA1, CRA2, RA13, RY/DC/RE/ML(STP), EO(S2P), E2(S2P), S12(JV25), SHORT BAR EO THE OTHERS ARE THE SAME AS - 05.

PCBA VERSIONS	MAIN SPEC.	X PARTS
-22 REV. A	48tpi D. SIDE B	U6(74LS74A), RA1(T-1.5K), R7(1.5K), S11(JV25), S14(JV25), S16(JV25), EO(JV20) STRAP POST PINS:DC1/DC2(S3P), DC3/DC4(S3P) SHORT BAR :DC3 DELETE:CRA1, CRA2, RA13, RE/ML(S4P), RY(S2P), XT(S2P), EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.
-23 REV. A	96tpi D. SIDE F	RA1(8-1K), RA9(T-7613-01, 1-4:5.1K), R7(1K), C22(10P), S15(JV25) DELETE:05, CR1, J3(14P) THE OTHERS ARE THE SAME AS - 03.
-24 REV. A	96tpi D. SIDE GF	RA1(8-1K), RY(1K) THE OTHERS ARE THE SAME AS - 05.
-25 REV. A	96tpi D. SIDE GF	EO(JV20) STRAP POST PINS:DC3(S2P), RY(S2P) SHORT BAR :DC3 DELETE:05, CR1, CRA1, CRA2, RA13, RY/DC/RE/ML(STP), EO(S2P), E2(S2P), S12(JV25) SHORT BAR EO THE OTHERS ARE THE SAME AS - 05.
-26 REV. A	96tpi D. SIDE G	J8(3P), S12(JV25) THE OTHERS ARE THE SAME AS - 04.
-27 REV. A	48tpi D. SIDE B	RA1(8-1K), RY(JV25), FG(JV25), IB(JV25), 06(1-2, JV25), L1(JV20), L2(JV20), EO(JV20) STRAP POST PINS:DSO/DS1(V4P) DELETE:05, 06, CRA1, CRA2, CR1, CR3, RA10, RA13, R7, C1(10μF), C7(22μF), C30(0.33μF), L1(39μH), L2(39μH), J3(14P), U1~1U(V6P), RY(S2P), XT(S2P), ML/RE(S4P), EO(S2P), E2(S2P), FG(JV25), SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.
-28 REV. A	96tpi D. SIDE GF	RA1(8-1K), R19B, R22(536), R20, C34(1200P), J5(S7P), I/B(S3P), DSO(JV25), RY(JV25), EO(JV20), S0(JV25) JUMPER:P2~S9 DELETE:CRA1, CRA2, RA13, R7, R19A, C34, J3(16P), J8(3P), DS0~DS3(V8P), U1~1U(V6P), HG/LG/1/E(V6P), RY/DC/RE/ML(STP), EO(S2P), E2(S2P), S12(JV25), SHORT BAR EO THE OTHERS ARE THE SAME AS - 05.
-29 REV. A	48tpi D. SIDE B	U6(74LS74A), S11(JV25), S14(JV25), S16(JV25), EO(JV20) STRAP POST PINS:DC1/DC2(S3P), DC3/DC4(S3P) SHORT BAR :DC2, DC4 DELETE:CRA1, CRA2, RA13, RE/ML(S4P), RY(S2P), XT(S2P), EO(S2P), E2(S2P), SHORT BAR EO THE OTHERS ARE THE SAME AS - 01.

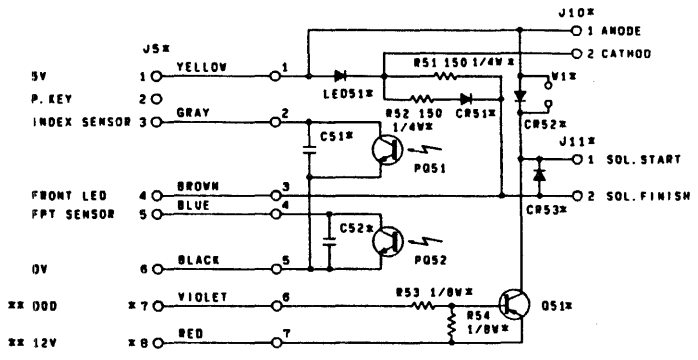VERSION TABLE   P/N 15532060-XX (PCB ISSUE F~)

TEAC ティアック株式会社

型式 FD-55V

品名 PCBA MFD CONTROL SH

図名 SCHEMATIC

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VERSION TABLE

PCBA VERSIONS	MAIN SPEC.	* PARTS
-00	RED	LED51(RED), R51, J5(S6P)
-01	GREEN	LED51(GREEN), R51, J5(S6P)
-02	DOOR LOCK RED	LED51(RED), R51, CR53, W1, J11(2P)
-03	DOOR LOCK GREEN	LED51(GREEN), R51, CR53, W1, J11(2P)

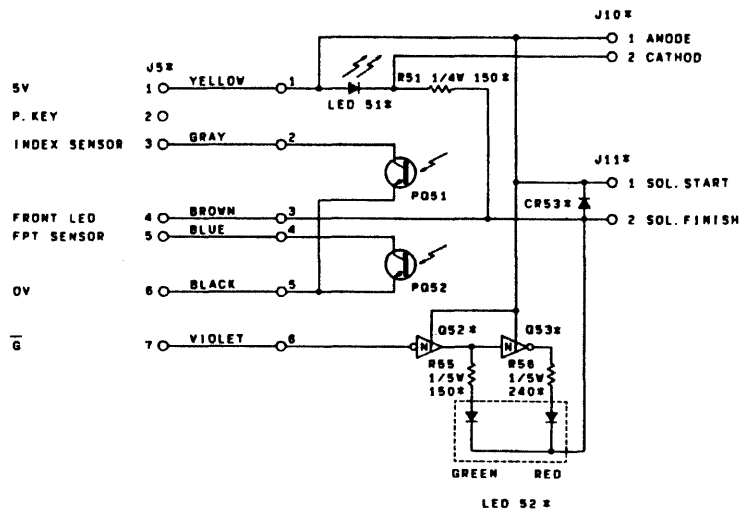VERSION TABLE   P/N 15532064-XX

NOTES: 1. PARTS WITH AN ASTERISK(*) ARE DIFFERENT IN EACH PCBA VERSION.
        REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

2. RESISTOR(R) VALUES ARE IN OHMS. 1/8W OR GREATER. ±5%(J). UNLESS OTHERWISE
   SPECIFIED.

3. CAPACTOR(C) VALUES ARE IN MICRO FARADS. 25V OR HIGHER. ±5%(J). UNLESS
   OTHERWISE SPECIFIED.

4. POLARIZING KEY POSITION FOR CONNECTOR J5 IS 2.

5. SIGNALS WITH DOUBLE ASTERISKS(**) ARE USED IN SOME OPTIONAL FDD VERSIONS.
   REFER TO FD-55V TOTAL DIAGRAM AND IT'S VERSION TABLE.

J5*
5V   1 YELLOW
P.KEY   2 GRAY
INDEX SENSOR 3
FRONT LED   4 BROWN
FPT SENSOR 5 BLUE
0V   6 BLACK
** OOD   *7 VIOLET
** 12V   *8 RED

J10*
1 ANODE
2 CATHOD
R51 150 1/4W*
LED51* R52 150 1/4W* CR51*
W1*
CR52*
C51* PQ51
J11*
1 SOL.START
2 SOL.FINISH
CR53*
C52* PQ52
R53 1/8W*
R54 1/8W* Q51*

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3. POLARIZING KEY POSITION FOR CONNECTOR J5 IS 2.

2. RESISTOR(R) VALUES ARE IN OHMS. 1/4W OR GREATER. ±5%(J). UNLESS OTHERWISE
   SPECIFIED.

NOTES: 1. PARTS WITH AN ASTERISK(*) ARE DIFFERENT IN EACH PCBA VERSION.
       REFER TO VERSION TABLE. UNLISTED PARTS ARE NOT USED IN THAT VERSION.

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PCBA VERSIONS	MAIN SPEC.	* PARTS
-10	RED/ GREEN	LED52(RED/GREEN), Q52, Q53, R55, R56, J5(STP)

VERSION TABLE

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