SUPER-10
TURBO XT MAINBOARD
USER'S MANUAL

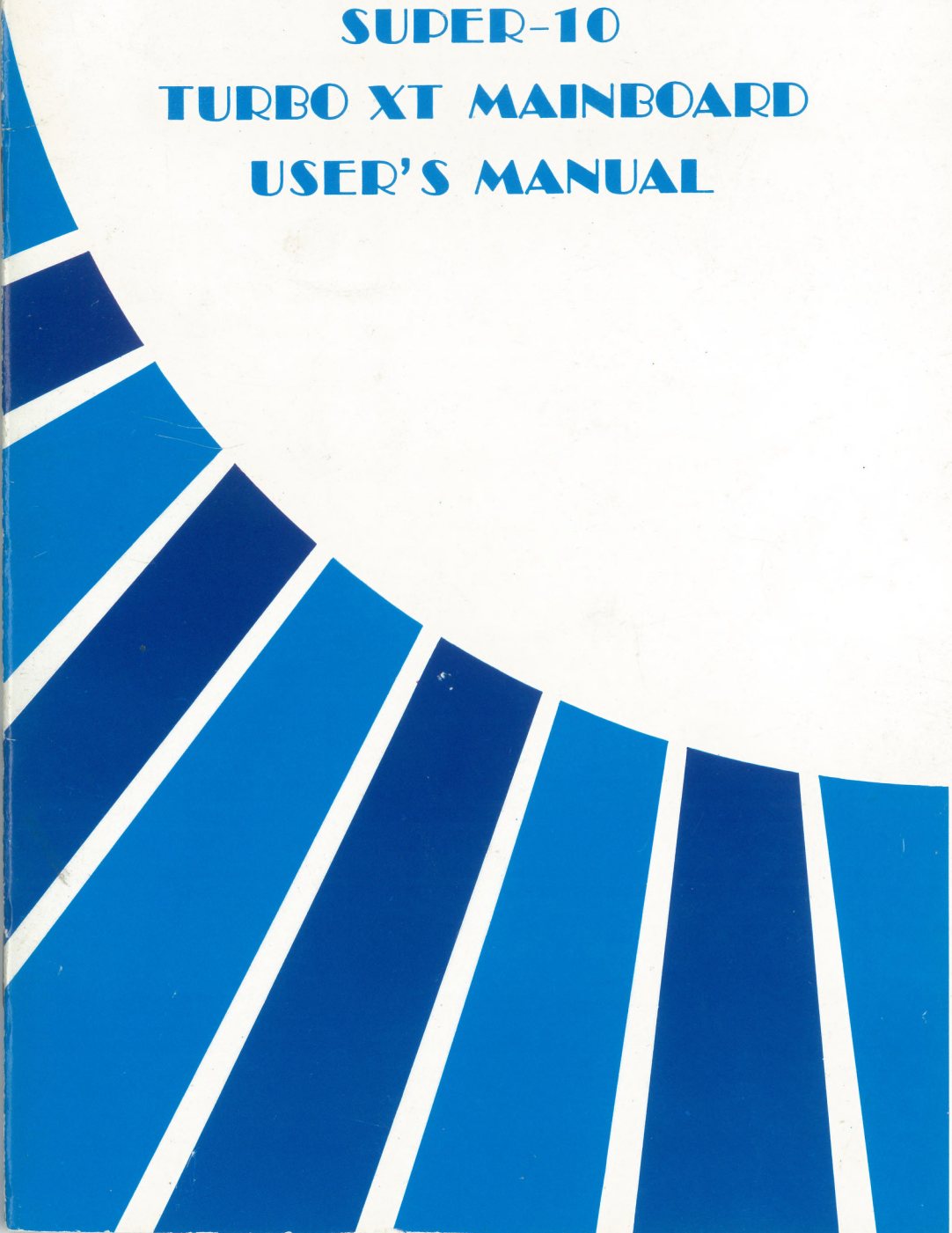


TABLE OF CONTENTS

CHAPTER 1
THE SYSTEM BOARD

1.1 Introduction

The SUPER 10 is 8 or 10MHZ TURBO XT MAINBOARD. The 8 or 10MHZ TURBO system board fits horizontally in the base of the system unit and is approximately 8½x12 inches. It is a double sided P.C.B.; DC power and a signal from the power supply enter the board through two six-pin connectors. Other connectors on the board are for attaching the keyboard and speaker. Eight 62-pin card edge-sockets are also mounted on the board. The I/O channel is bussed across these eight I/O slots.

A "Dual-in Line Package (DIP) switch (SW1) (one eight-switch pack)" is mounted on the board and can be read under program control. The DIP switch provides the system software with information about the installed options, how much storage the system board has, what type of the display adapter is installed what operation modes are desired when power is switched on (color or black-and-white, 80- or 40-character lines), and the number of diskette drive attached.

The system board consists of five function area: the processor subsystem and its support elements, the Read-Only Memory (ROM) subsystem, the Read/Write (R/W) Memory subsystem, integrated I/O adapters, and the I/O channel. All are desired in this section.

The hear of the 8 or 10MHZ Turbo system board is the INTEL 8088-1 or NEC D70108-8/10(V-20)microprocessor. This processor is an 8-bit external bus version of INTEL'S 16 bit 8086 processor, and it's software compatible with the 8086. Thus, the 8088 supports 16 bit operations, including multiply and divide, and supports 20 bits addressing (1 megabyte of storage).

It also operates in a maximum mode, so a coprocessor can be added as a feature. The processor operates in two mode, which can be switched, called Normal mode and Turbo mode. When the processor operating at 4.77MHZ called Normal mode, the frequency, which is derived from a 14.318MHZ crystal, is divided by 3 for the processor clock, and by 4 to obtain the 3.58MHZ color burts signal required for color television. When processor operating at 8 or 10MHZ called Turbo mode, the frequency is derived from 30MHZ.

– KEYBOARD –

The system board contains the adapter circuits for attaching the serial interface to the keyboard. These circuits generate an interrupt on the the processor, when a complete scan code is received. The interface can request execution of a diagnostic test in the keyboard.

The keyboard interface, a 5-pin DIN connector on the system board, extends through the rear panel of the system unit.

– SPEAKER –

The system unit has a 2¼ inch audio speaker. The speaker s control circuits and driver are on the system board. The speaker connects through a 2-wire interface that attaches to a 4-pin connector on the system board.

The speaker drive circuit could be capable of providing approximately ½ watt of power. The control circuits allow the speaker to be driven three different ways: 1) a direct program control register bit may be toggled to generate a pulse train ; 2) the output from Channel 2 of the timer counter, may be programed to generate a wave form to the speaker; 3) the clock input to the timer counter, can be modulated with a program to control I/O register bit. All three methods may be performed simultaneously.

– DMA –

Three of the four DMA channels are available on the I/O bus and support high speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programing a channel of the timer-counter device to periodically request a dummy DMA transfer. This action creates a memory read cycle available to refresh dynamic storage on the system board and in the system expansion slots. All DMA data transfers, except the refresh channel, take five processor clocks of 210 ns, or 1.05 μs if the processor ready line is not deactivated. Refresh DMA cycles take four clocks or 840 ns.

– MEMORY –

The system board supports both ROM/EPROM and R/W memory. It has space for 32kx1 & 8kx1 of ROM or EPROM. This ROM contains the power-on self-test, I/O drivers, dot patterns for 128 characters in graphics mode, and a diskette.

The system board also has from 256k to 640k of R/W memory. A minimum system would have 256K of memory.

– TIMER –

The three programmable timer/counters are used by the system as follows: Channel 0 is used as a general purpose timer, providing a constant time base for implementing a time-of-day clock; Channel 1 requests refresh cycles from the DMA channel; anc Channel 2 is used to spports the tone generation for the audio speaker. Each channel has a minimum timing resolution of 1.05 μs.

– INTERRUPT –

Of the eight prioritized levels of interrupts, six are bussed to the system expansion slots for features cards. Two levels are used on the system board. Level 0, the highest priority, is attached to Channel 0 of the timer/counter and provides a periodic interrupt for the time-of-day clock. Level 1 is attached to the keyboard adapter circuits and receives an interrupt for each scan code sent by the key-board. The Non-Maskable Interrupt (NMI) of the 8088 is used to report memory parity errors.

1.2 Expansion I/O Channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered, and enhanced by the addition of interrupts and Direct Memory Access (DMA) functions.

The I/O channel contains an 8 bit, bidirectional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines, a channel check line, and power and ground for the adapters. Four voltage levels are provided for I/O card: +5Vdc, −5Vdc, +12Vdc, and −12Vdc.

A "ready" lines is available on the I/O channel, to allow operation with slow I/O or memory devices. If the channel's ready line is not activated by an addressed device, all processor-generated memory read and write cycles take four 210 ns clock or 840 ns/byte. All processor-generated I/O read and write cycles require five clocks for a cycle time of 1.05 μs/byte. Refresh cycles occur once every 72 clocks (approximately 15 μs) and require four clocks or approximately 7% of the bus handwidth.

I/O devices are addressed through I/O mapped address space. The channel is designed so that 768 I/O device addressed are available to the I/O channel cards.

A channel check line reports error conditions to the processor. Activating this line results in a Non-Maskable Interrupt (NMI) to the 8088 processor. Memory expansion options use this line to report parity errors.

The I/O channel is repowered, to provide sufficient drive, to power all eight (J1 through J8) expansion slots. Assuming two Low-Power Schorttky (LS) loads per slot, the I/O adapters typically use only one load.

1.3 I/O Channel Description

The following is a description of the PC/XT I/O Channel. All lines are TTL-compatible.

Signal I/O Description

OSC, Oscillator:

High speed clock with a 70-ns period (14.31818 MHz) has a 50% duty cycle.

CLK, System Clock:

It is divide-by-three of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.

RESET:

This line resets or initializes system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.

A0-A19, Address Bits 0 to 19:

These lines address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the Least Significant Bit (LSB) and A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.

D0-D7, I/O Data Bits 0 to 7:

These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices. D0 is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These lines are active high.

ALE, Address Latch Enable:

This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the failing edge of ALE.

I/O CH CK, I/O Channel Check:

This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error would indicate.

I/O CH RDY, I/O Channel Ready:

This line, normally high (ready), can be pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This lines should never be held low, longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles.

IRQ2-IRQ7, Interrupt Request 2 to 7:

These lines are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high, until it was acknowledged by the processor (interrupt service routine).

IOR, I/O Read Command:

This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor on the DMA controller. This signal is active low.

IOW, I/O Write Command:

This command line instructs an I/O device, to read the data from the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMR, Memory Read Command:

This command line instructs the memory to drive its data into the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMW, Memory Write Command:

This command line instructs the memory to store the data of the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

DRQ1–DRQ3, DMA Request 1 to 3:

These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK line goes active.

DACK0-3–DAM Acknowledge 0 to 3:

These lines are DACK3 used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active low.

AEN, Address Enable:

This line degates the processor and other devices from the I/O channel to allow DMA transfers. When this line is active (high), the DMA controller controls the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).

T/C, Terminal Count:

This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

The following voltages are available on the system board I/O channel:

+5 Vdc + – 5%, located on 2 connector pins
–5 Vdc + –10%, located on 1 connector pin
+12 Vdc + – 5%, located on 1 connector pin
–12 Vdc + –10%, located on 1 connector pin
GND (Ground), located on 3 connector pins

1.4 Speaker Interface

The sound system has a small, permanent-magnet, 2¼ inch speaker. The speaker can be driven from one or two sources:

* An 8255A-5 PPI output bit. The address and bit are defined in the "I/O Address Map"

* A timer clock channel, the output of which is programmable within the functions of the 8253-5 timer when using a 1.19-MHz clock input. The timer gate also is controlled by an 8355A-5 PPI output-port bit. Address and bit assignment are in the "I/O Address Map".

The speaker connection is a 4-pin berg connector, See System Board Component Diagram", earlier in this section, for speaker connection or placement.

CHAPTER 2

THE NORMAL/TURBO MODE OPERATION

2.1 Adventages of the 8 or 10MHZ Turbo

The difference between super 10 and other PC/XT main boards is 8 or 10 MHZ main board allows an increase at about 110% in speed of program execution. As the 8088-1 or NEC D70108-8/10 (V20) processor operates at a quicker speed at 8 or 10 MHZ. In other PC/XT main board, the clock speed is only 4.77 MHZ.

The SUPER 10 consists of dual clock system, in Normal mode; the clock speed is only 4.77 MHZ cycle. In Turbo mode, the clock speed increases to 8 or 10MHZ cycle.

Note No. 1: Please do not make use of RAM memory on interface card. Because its original design may be not compatible with 10 MHZ high speed CPU at access time. *Please use memory on mainboard and use 4164 and 41256 and 4464 access time within 120 ns.

For Example:

	4164	41256
NEC	D4164C	D41256C
HITACHI	HM4846	HM50256
MITSUBISHI	MSK4164	MSM4256P
PANASONIC	MN4164	MN41256

2.2 To Obtain Turbo Mode at 8 or 10MHZ

The system board supports both software switch as well as hardware switch to allow transaction from Normal mode (4.77 MHZ) to Turbo mode (8 or 10 MHZ) and software switch. Hardware switch can be used at the same time to select each of them by jumper.

A) Hardware Switch Setting:

SW1:

1 = OFF	Normal Speed of 4.77MHZ
1 = ON	Turbo Speed of 8 or 10MHZ

B) Software Switch Setting: (Award BIOS only)

1) On hard switch turbo mode:
   press CTRL + ALT + '+' then skip to 4.77MHZ.
   press CTRL + ALT + '—' will Return to the source mode.
2) On hard switch 4.77 mode:
   press CTRL + ALT + '+', then skip to turbo 8 or 10MHZ.
   press CTRL + ALT + '—' will Return to the source mode.

C) Software Switch Setting (Phoenix and AMI BIOS)

On hard switch mode, pressing CTRL + ALT + '+' can continuously and uninterruptedly skip from Low Speed Mode to High Speed Mode, and return to Low Speed Mode.

CHAPTER 3

CONNECTORS AND SWITCH SETTING

3.1 Connectors

The system board has the following connectors:

One power-supply connector (CN1)
One keyboard connector

- Keylock connector (JP1)
- Reset connector (JP2)
- Speaker and power LED connector (JP3)
- Turbo LED connector (JP4)
- Turbo speed SWITCH (JP5) – simulation DIP PIN 1

A) Power Supply Connector (CN1)

Pin	Assignments	Connector
1	Power good	CN1
2	Not used	
3	+ 12 Vdc	
4	–12 Vdc	
5	Ground	
6	Ground	
7	Ground	
8	Ground	
9	–5 Vdc	
10	+5 Vdc	
11	+5 Vdc	
12	+5 Vdc	

B) Keyboard Connector

The keyboard connector is a 5-pin, 90-degree Printed Circuit Board (PCB) mounting, DIN connector. The pin assignments as follows:

Pin	Assignments
1	Keyboard clock
2	Keyboard data
3	Keyboard reset
4	Ground
5	+5 Vdc

C) Keylock Connector (JP1)

There are two types of keylock connector (keylock 1, keylock 2) supported to user, in order to suit for different keylock on case.

(1) Series: keylock 1 see in fig. 3. 1. 1

(2) Parallel: keylock 2 see in fig. 3. 1. 1 (when keylock 2 is used, lock 1 must be shorten)

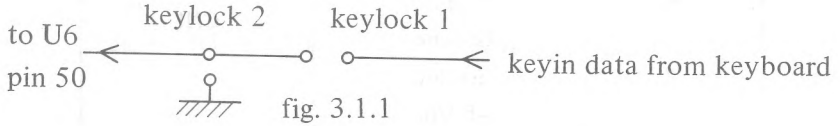


fig. 3.1.1

D) Reset Connector (JP2)

The reset connector is a 2-pin, keyed, bergstrip. When this connector (JP2) is open, system is in regular operation. When this connector (JP2) is shorted for a while system restarts.

E) Speaker and Power LED Connectors (JP3)

The speaker and power LED connectors is a 4-pin berg strip. It's pin assignments as follows:

Pin	Assignments
1	Speaker
2	+5 Vdc
3	Ground
4	+5 Vdc

- Pin 1 & Pin 2 to speaker.
- Pin 3 & Pin 4 to power LED.

F) Turbo LED Connector (JP4)

The turbo LED connector is a 2-pin, keyed, berg strip.

G) Tubro speed SWITCH (JP5) – Simulation DIP PIN 1.

1. When you select Turbo speed SWITCH (JP5) to change the speed of system board. Please first note the following two points:
   (1) First, set DIP PIN 1 "OFF".
   (2) JP5 is only available during reset action.
2. Turn power on
   (1) If Turbo light is on, it means on "Hard SWITCH TURBO MODE". Please refer to section 2.2 to change the speed.
   (2) If Turbo light is off, it means on "Hard SWITCH 4.77 MODE". Please refer to section 2.2 to change the speed.

3.2 The System Board Switch Setting

The DIP Switch (SWI) is used to set the system configuration and specify the amount of memory installed on the system board.

Position

1	Mode of speed
2	Use for 8087-2 co-processor
3-4	Amount of memory on system board
5-6	Type of display adapter
7-8	Number of 5¼ inch disketted rivos.

Switch (SW1):

1 = ON	Turbo Speed of 8 or 10MHZ
1 = OFF	NORMAL Speed of 4.77 MHZ
2 = ON	W/O 8087-2 co-processor
2 = OFF	W 8087-2 co-processor

Memory Switch Settings:

3 = OFF	4 = ON	640K MEMORY INSTALLED
3 = ON	4 = OFF	512K MEMORY INSTALLED
3 = OFF	4 = OFF	256K MEMORY INSTALLED

Display Adapter Switch Settings:

5 = ON	6 = ON	NO DISPLAY ADAPTER
5 = OFF	6 = ON	COLOR/GRAPHICS (40x20 Mode)
5 = ON	6 = OFF	COLOR/GRAPHICS (80x25 Mode)
5 = OFF	6 = OFF	MONOCHROME DISPLAY ADAPTER OR BOTH

Display Drive Switch Setting:

7 = ON	8 = ON	1 DRIVE INSTALLED
7 = OFF	8 = ON	2 DRIVES INSTALLED
7 = ON	8 = OFF	3 DRIVES INSTALLED
7 = OFF	8 = OFF	4 DRIVES INSTALLED

CHAPTER 4

MEMORY RAM/ROM CHIPS INSTALLATION

4.1 RAM chips Installation

The 8 or 10MHZ Turbo mainboard provides 4 banks of memory.

BANK 0 is made up of 9 pieces of 41256 in U33 through U41.
BANK 1 is made up of 9 pieces of 41256 in U42 through U50.
BANK 2 is made up of 2 pieces of 4464 in U27, U29 and one pieces of 4164 in U31.
BANK 3 is made up of 2 pieces of 4464 in U28, U30 and one pieces of 4164K in U32.

4 potions of memory configuration can be installed on board. Follow the instructions below for proper installation:

Note:

Option	RAM chips on Bank 0	RAM chips on Bank 1	RAM chips on Bank 2	RAM chips on Bank 3
256K RAM	41256x9	No chip	No chip	No chip
512K RAM	41256x9	41256x9	No chip	No chip
576K RAM	41256x9	41256x9	4464x2 +4164x1	No chip
640K RAM	41256x9	41256x9	4464x2 4164x1	4464x2 +4164x1

4.2 ROM chips Installation

The 8 or 10MHZ Turbo Main board provides 2 ROM chips space for system.

U22 must be installed 2764 for ROM BIOS.
U23 must be installed 27256 for ROM BASIC.

APPENDIX

The SUPER 10 System board is used a customer specific IC designed. This customer chip is called M1101.

M1101

SPECIFICATION

1. General Description

The M1101 is a customer specific IC designed as the peripheral controller of 8088 microprocessor to perform the PC/XT function. It was implemented with 2μ CMOS technology and packaged with 100 pins plastic flat package.

2. Features

Fully IBM-PC/XT compatible

82C84 Clock generator with 2 clock inputs to generate the CPU. They are 14.318MHz and 24MHz which will support 4.77 MHz and 8MHz CPU clock with 1/3 duty cycle. Up to 30MHz (10MHz CPU speed) can be achieved with careful system design and PCB layout skill.

82C88 Bus controller.

82C37 4 channels DMA controller, channel 0 is used for DRAM refresh.

82C59 8 channels interrupt controller, level 0 is used for system time base, and level 1 for keyboard input.

82C53 3 channels timer, channel 0 is used for system time base, channel 1 for DRAM refresh, and channel 2 for speaker audio.

82C55 Peripheral I/O, used for keyboard interface and system configuration switch (same as the PC/XT).

74322 Keyboard interface, supported PC/XT type keyboard.

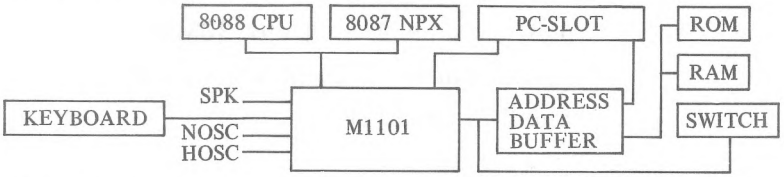
74280 Parity check and generator.

74670 4 bit page register for DMA.

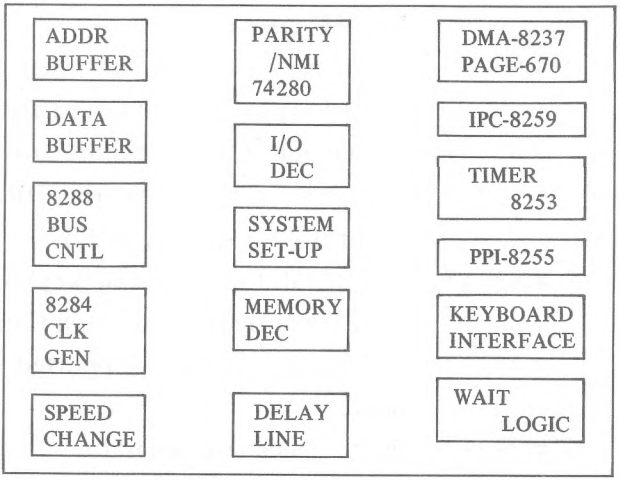
Wait state logic.
NMI control logic.
ROM decoder for one 2764 and one 27256.
RAM decoder for 4164 or 41256 DRAM.
H/W and S/W CPU speed change and indicator.
Build-in delay line for RAS, CAS, and MUX.
Low power comsumption: less than 300mW in 8MHz CPU speed.
Small PCB size: 100 pin Plastic Flat Package.

3. System Configuration

The PC/XT system with M1101 is shown as following:



4. Chip Block



5. Inserted wait state:

	Low	High
Onboard Memory	0	0
Onboard I/O	1	4
Slot Memory	0	2
Slot I/O	1	4

6. Internal I/O Address Map

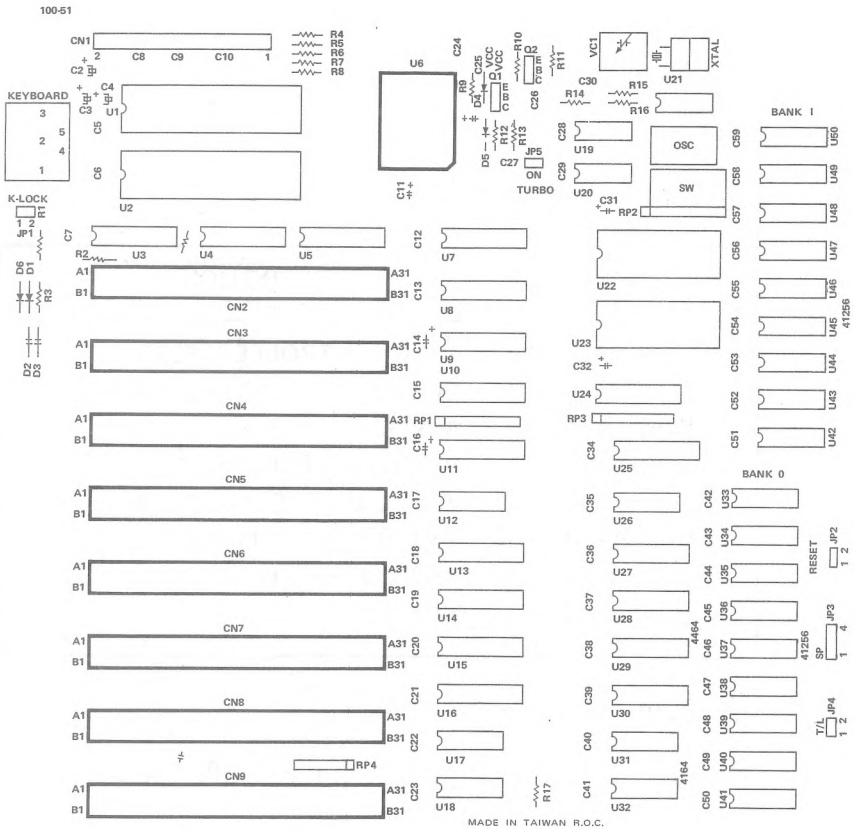
ADDRESS	DEFINITION
000H-01FH	DMA CONTROLLER (8237)
020H-03FH	INTERRUPT CONTROLLER (8259)
040H-05FH	SYSTEM TIMER (8253)
060H-07FH	PARALLEL PORT (8255)
080H-09FH	DMA PAGE REGISTER (74670)
0A0H-0BFH	NMI MASK REGISTER
0C0H-0C3H	CHANGE SPEED
0E0H-0E3H	STATUS

7. Port 0C0H: Write only.

A write command to this port will toggle CPU speed.

8. Port 0E0H: Status Read only.

DIP SW:


100-51
CN1
KEYBOARD
K-LOCK
JP1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
CN2
CN3
CN4
CN5
CN6
CN7
CN8
CN9
RP1
RP2
RP3
RP4
JP5
TURBO
ON
OSC
SW
VC1
XTAL
BANK I
BANK 0
RESET
JP2
JP3
JP4
T/L
SP
41256
4464
4164
MADE IN TAIWAN R.O.C.